NB7VPQ16M

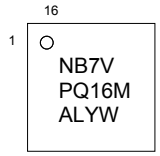
1.8V / 2.5V CML 12.5 Gbps Programmable Pre-Emphasis Copper/Cable Driver with Selectable Equalizer Receiver

Multi-Level Inputs w/ Internal Termination

ON Semiconductor®
http://onsemi.com

1
QFN−16
MN SUFFIX
CASE 485G

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

Description

The NB7VPQ16M is a high performance single channel programmable Pre-Emphasis CML Driver with an Equalizer Receiver (signal enhancer) that operates up to 12.5Gbps with a 1.8V or 2.5V power supply. When placed in series with a Data/Clock path, the NB7VPQ16M inputs will compensate the degraded signal transmitted across a FR4 PCB backplane or cable interconnect. Therefore, the serial data rate is increased by reducing Inter-Symbol Interference (ISI) caused by losses in copper interconnect or long cables.

The Pre-Emphasis buffer is controlled using a serial bus via the SDIN (Serial Data In) and SCLKIN (Serial Clock In) control inputs and contains circuitry which provides sixteen programmable Pre-Emphasis settings to select the optimal output compensation level. These selectable output levels will handle various backplane lengths and cable lines. The first four SDIN bits (D3:D0) will digitally select 0 dB through 12 dB typical of de-emphasis (see Table 1).
For cascaded applications, the shifted SDIN and SCLKIN signals are presented at the SDOUT and SCLKOUT pins.
The 5th-bit (LSB) of the serial data bits allows for enabling the equalization function of the receiver.

The differential Data / Clock inputs incorporate a pair of internal 50-Ω termination resistors, in a 100- Ω center-tapped configuration, via the VT pin and will accept LVPECL, CML or LVDS logic levels. This feature provides transmission line termination on-chip, at the receiver end, eliminating external components.

The NB7VPQ16M is a member of the GigaComm™ family of high performance Data/Clock products with Pre-Emphasis/Equalization (PEEQ).

Features

- Maximum Input Data Rate > 12.5Gbps
- Maximum Input Clock Frequency > 8GHz
- Drives Up To 18-inches of FR4
- (16) Programmable Output De-emphasis Levels; 0dB through 12dB
- 100ps typical Propagation Delay
- Differential CML Outputs, 400mV peak-to-peak, typical (PE = 0dB)
- Operating Range: V_{CC} = 1.71V to 2.625V, GND = 0V
- Internal Output Termination Resistors, 50-Ω
- QFN-16 Package, 3mm x 3mm, Pb-free
- -40ºC to +85ºC Ambient Operating Temperature

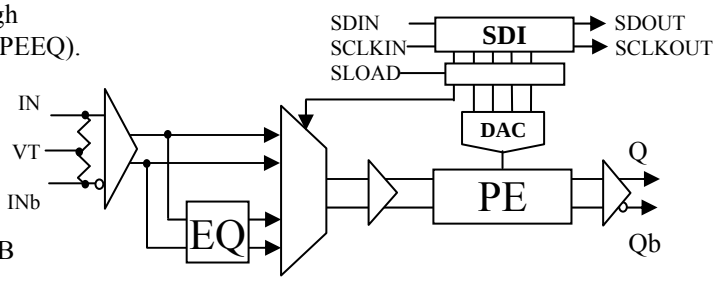


Figure 1. Simplified Logic Diagram

Rev. 9-29-08

Publication Order Number:
NB7VPQ16M/D

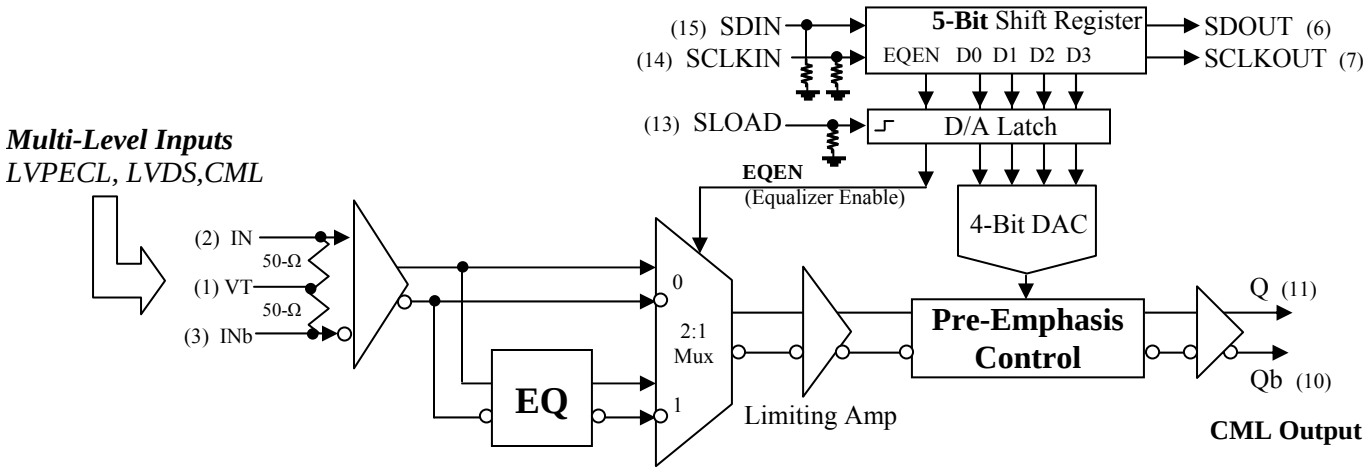


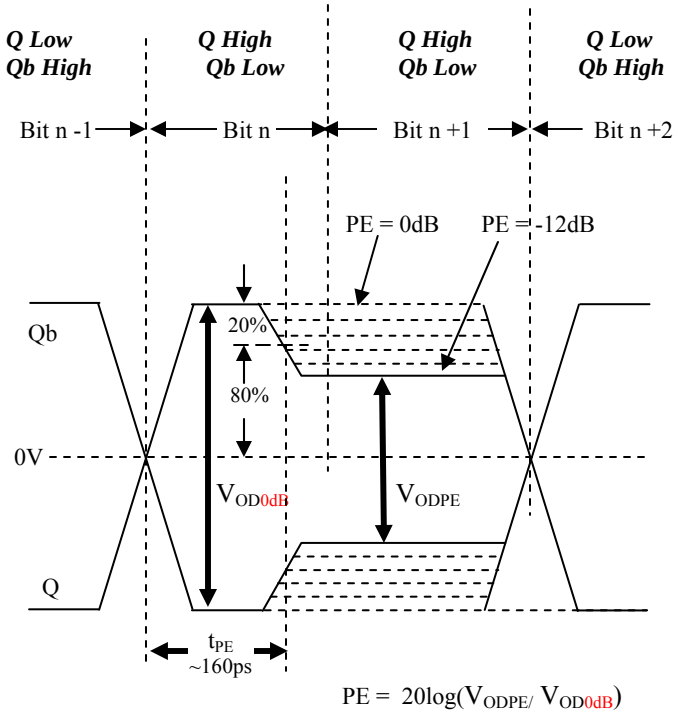
Figure 2. Detailed Block Diagram of NB7VPQ16M

Table 1. Typical Pre-Emphasis Control Table, EQ=0, 25°C, VCC = 1.8V

Decimal	4-bit PE MSB LSB D3 D2 D1 D0	PE Output Compensation in dB Approximate @ 1GHz	VODPE (mV) typical
00	0 0 0 0	0 dB (Default)	435
01	0 0 0 1	-1.0 dB	390
02	0 0 1 0	-1.5 dB	365
03	0 0 1 1	-2.0 dB	345
04	0 1 0 0	-2.5 dB	325
05	0 1 0 1	-3.0 dB	310
06	0 1 1 0	-3.5 dB	290
07	0 1 1 1	-4.0 dB	275
08	1 0 0 0	-4.5 dB	260
09	1 0 0 1	-5.0 dB	245
10	1 0 1 0	-6.0 dB	220
11	1 0 1 1	-7.0 dB	195
12	1 1 0 0	-8.0 dB	175
13	1 1 0 1	-9.0 dB	155
14	1 1 1 0	-10.0 dB	135
15	1 1 1 1	-12.0 dB	110

Table 2. Equalizer Enable Function

EQEN	Function
0	IN / INb Inputs By-pass the Equalizer section
1	Inputs flow through the Equalizer



V_{OD0dB} – Differential Output Voltage without Pre-Emphasis
V_{ODPE} – Differential Output Voltage with Pre-Emphasis

Figure 3. Illustration of Output Waveform Definition

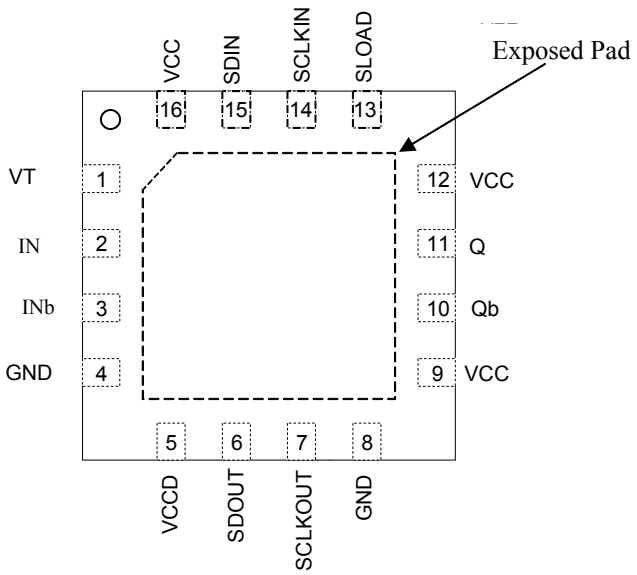


Figure 4. NB7VPQ16M Pinout: QFN-16 (Top View)

Table3. Pin Description

Pin	Name	I/O	Description
1	VT		Internal 50-Ω Termination Pin for IN and INb
2	IN	LVPECL, CML, LVDS Input	Non-inverted Differential Clock/Data Input. Note 1
3	INb	LVPECL, CML, LVDS Input	Inverted Differential Clock/Data Input. Note 1
4	GND	-	Negative Supply Voltage; Note 2
5	VCCD	-	Positive Supply Voltage for Serial Bus Logic and 5-Bit DAC; Note 2
6	SDOUT	LVCMOS Output	Serial Data Out
7	SCLKOUT	LVCMOS Output	Serial Clock Out
8	GND	-	Negative Supply Voltage; Note 2
9	VCC	-	Positive Supply Voltage for the analog circuitry and CML Output buffer; Note 2
10	Qb	CML	Inverted Differential Output. Note 1.
11	Q	CML	Non-inverted Differential Output. Note 1
12	VCC	-	Positive Supply Voltage for the analog circuitry and CML Output buffer; Note 2
13	SLOAD	LVCMOS Input	When the SLOAD pin is LOW or left open (has internal pull-down resistor), the output of the shift register will input the 4-bit DAC and set the EQEN bit. When HIGH, the input to the 4-bit DAC is locked to the state prior to when SLOAD went HIGH.
14	SCLKIN	LVCMOS Input	Serial Clock In; pin will default LOW when left open (has internal pull-down resistor)
15	SDIN	LVCMOS Input	Serial Data In; pin will default LOW when left open (has internal pull-down resistor)
16	VCC	-	Positive Supply Voltage for the analog circuitry and CML Output buffer; Note 2
EP			The Exposed Pad (EP) on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is also electrically connected to the die, and is recommended to be electrically and thermally connected to GND on the PC board.

1. In the differential configuration when the input termination pin (V_T) is connected to a common termination voltage or left open, and if no input signal is applied on IN/INb input, then the device will be susceptible to self-oscillation. Q/Qb outputs have internal 50-ohm source termination resistor.
2. All V_{CC}, V_{CCD} and GND pins must be externally connected to external power supply voltage to guarantee proper device operation.

Table 4. Attributes

Characteristic		Value
ESD Protection	Human Body Model Machine Model	> 4kV > 200 V
Internal Input Pull-down Resistor		75kΩ
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 3)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		416
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1		Rating	Unit
V_{CC}/V_{CCD}	Positive Power Supply	GND = 0 V		3.0	V
V_{IN}	Positive Input Voltage	GND = 0 V		-0.5 to V_{CC} +0.5	V
V_{INPP}	Differential Input Voltage |IN - INb|			1.89	V
I_{out}	Output Current	Continuous Surge		34 40	mA mA
I_{IN}	Input Current Through R_T (50-Ω Resistor)			+/-40	mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 4) TGSD 51-6 (2S2P Multilayer Test Board) with Filled Thermal Vias	0 LFPM 500 LFPM	QFN-16 QFN-16	42 35	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	QFN-16	4	°C/W
T_{sol}	Wave Solder Pb-Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board - 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 6. DC CHARACTERISTICS POSITIVE CML OUTPUT V_{CC} = V_{CCD} = 1.71V to 2.625V; GND = 0V; TA = -40°C to 85°C (Note 5)

Symbol	Characteristic		Min	Typ	Max	Unit
Power Supply Current						
I_{CC}	Power Supply Current, (Inputs and Outputs Open) PE = 0dB	VCC = 2.5V VCC = 1.8V		95 80	120 100	mA
I_{CCD}	Power Supply Current for Serial Bus and DAC (Inputs and Outputs Open)	PE = 0000 PE = 1111		0 10	 20	mA
CML Outputs PE = 0dB (Note 6, Figure 18)						
V_{OH}	Output HIGH Voltage		V_{CC} – 30	V_{CC} – 10	V_{CC}	mV
		VCC = 2.5V	2470	2490	2500	
		VCC = 1.8V	1770	1790	1800	
V_{OL}	Output LOW Voltage		V_{CC} – 600	V_{CC} – 500	V_{CC} – 400	mV
		VCC = 2.5V	1900	2000	2100	
			V_{CC} – 550	V_{CC} – 450	V_{CC} –350	
		VCC = 1.8V	1250	1350	1450	
Data / Clock Inputs (IN, INb) (Note 7)(Figures 7 & 8)						
V_{IHD}	Differential Input HIGH Voltage		1100		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage		GND		V_{CC} - 100	mV
V_{ID}	Differential Input Voltage (V_{IHD} - V_{ILD}) (Note 10)		100		1200	mV
I_{IH}	Input HIGH Current		-150	20	150	uA
I_{IL}	Input LOW Current		-150	5	150	uA
Control Inputs (SDIN, SCLKIN, SLOAD)						
V_{IH}	Input HIGH Voltage for Control Pins		V_{CCD} x 0.65		V_{CCD}	mV
V_{IL}	Input LOW Voltage for Control Pins		GND		V_{CCD} x 0.35	mV
I_{IH}	Input HIGH Current		-150	20	150	uA
I_{IL}	Input LOW Current		-150	5	150	uA
Control Inputs (SDOUT, SCLKOUT)						
V_{OH}	Output HIGH Voltage		VCC - 200		VCC	mV
V_{OL}	Output LOW Voltage		GND		200	mV
Termination Resistors						
R_{TIN}	Internal Input Termination Resistor		45	50	55	Ω
R_{TOUT}	Internal Output Termination Resistor		45	50	55	Ω

NOTE: This device is designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

5. Input and output parameters vary 1:1 with V_{CC}.
6. All output loading with external 50 Ω to V_{CC}.
7. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.

Table 7. AC CHARACTERISTICS V_{CC} = V_{CCD} = 1.71V to 2.625V; GND = 0V; TA = -40°C to 85°C (Note 9)

Symbol	Characteristic		Min	Typ	Max	Unit
$f_{DATAMAX}$	Maximum Input Data Rate		12.5	14		Gbps
f_{MAX}	Maximum Input Clock Frequency (Note 10)	VOUTPP ≥ 200mV	8			GHz
f_{SCLKIN}	Serial Clock Input Frequency				20	MHz
VOD_{0dB}	Output Voltage Amplitude (see Table 1) (@ $V_{INPPmin}$) (See Figure 3, Note 10)	f_{in} ≤ 6.0GHz f_{in} ≤ 8.0GHz	300 200	400 300		mV
t_{PE}	PreEmphasis Width, tested at -12dB PreEmphasis			130		ps
V_{CMR}	Input Common Mode Range (Differential Configuration, Note 11) Fig. 9		1050		V_{CC}	mV
t_{PLH}, t_{PHL}	Propagation Delay to Differential Outputs, 1GHz, measured at differential cross-point	IN/INb to Q/Qb SCLKIN to SCLKOUT		200 5	250 10	ps ns
t_{DC}	Output Clock Duty Cycle (Reference Duty Cycle = 50%)	f_{in} ≤ 5.0GHz	45	50	55	%
t_{s1} t_{s2} t_{s3}	Setup Time @ 50MHz (Figs. 10 & 11)	SDIN to SCLKIN SCLKIN to SLOAD SLOAD to IN/INb	5 TBD TBD			ps
t_{h1} t_{h2} t_{h3}	Hold Time @ 50MHz (Figs. 10 & 11)	SDIN to SCLKIN SCLKIN to SLOAD SLOAD to IN/INb	1 TBD TBD			ps
t_{PW_SLOAD}	SLOAD Minimum Pulse Width (Figure 11)		6			ns
t_{JITTER}	RJ – Output Random Jitter (Note 12) DJ - Residual Output Deterministic Jitter (Note 13) FR4 ≤ 3” FR4 = 12”	f_{in} ≤ 8.0GHz f ≤ 12.5Gbps f ≤ 6.5Gbps		0.1	0.8 10 10	ps rms ps rms ps pk-pk ps pk-pk
V_{INPP}	Input Voltage Swing (Differential Configuration) (Note 10)		100		1200	mV
t_r, t_f	Output Rise/Fall Times @ 1 GHz (20% - 80%), Q, Qb			35	50	ps

9. Measured using a 400 mV source, 50% duty cycle clock source. All output loading with external 50-Ω to V_{CC}. Input edge rates 40 ps (20% - 80%); PE = 0dB, EQEN = 0
10. Input / Output voltage swing is a single-ended measurement operating in differential mode.
11. V_{CMR} min varies 1:1 with V_{EE}, V_{CMR} max varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.
12. Additive RMS jitter with 50% duty cycle Clock signal.
13. Peak-to-Peak jitter with input NRZ data at PRBS23.

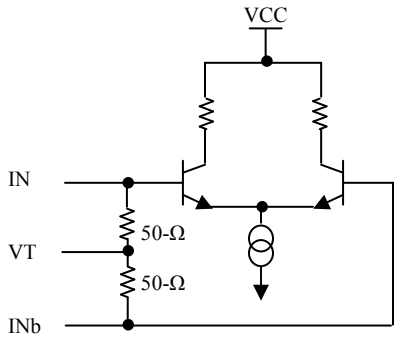


Figure 5. Input Structure

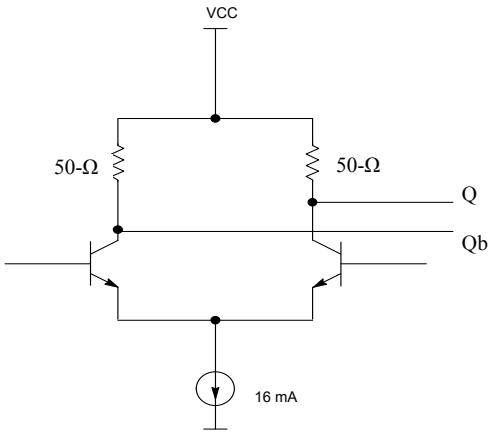


Figure 6. CML Output Structure

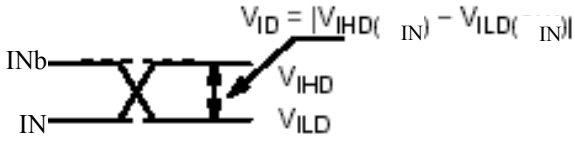


Figure 7. VID - Differential Inputs Driven Differentially

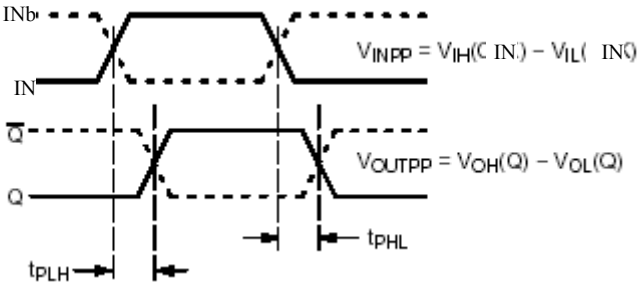


Figure 8. AC Reference Measurement

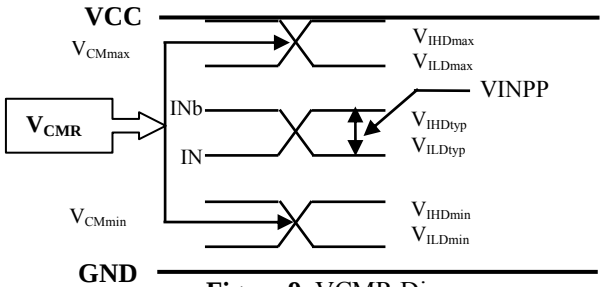


Figure 9. VCMR Diagram

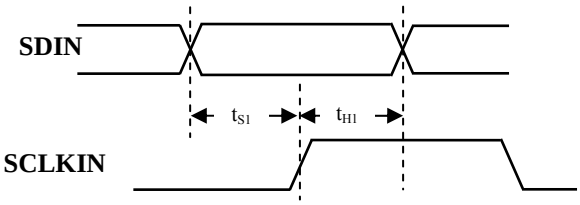


Figure 10. SLOAD Set-Up and Hold and t_{pw} min

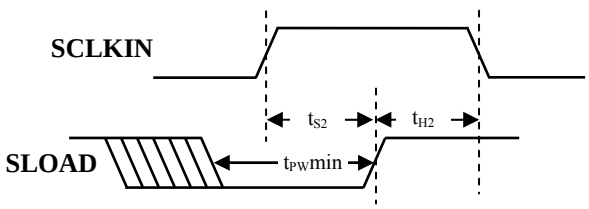


Figure 11. SLOAD Set-Up and Hold and t_{pw} min

Application Information

Data Inputs

The differential IN/INb inputs of the NB7VPQ16M can accept LVPECL, CML, and LVDS signal levels. The limitations for a differential input signal (LVDS, LVPECL, or CML) is a minimum input swing of 100 mV (single-ended measurement). Within this condition, the input HIGH voltage, VIH, can range from V_{CC} down to 1.1 V. Example interfaces are illustrated in Figure 18.

Serial Data Interface

The Serial Data Interface (SDI) logic is implemented with a 5-bit shift register scheme. The register shifts once per rising edge of the SCLKIN input. The serial data input SDIN must meet setup and hold timing as specified in the AC table. The configuration latches will capture the value of the shift register on the Low-to-High edge of the SLOAD input. The most significant bit (MSB) is loaded first. See the programming timing diagram for more information.

SDIN / SCLKIN

SDIN is the Serial Data input pin; SCLKIN is the Serial Clock input pin.

SLOAD

The SLOAD pin performs the DAC latch function. When LOW or left open, the DAC latch will pass the shift register outputs to the input of the DAC and the EQualizer ENable bit (EQEN). On the Low-to-HIGH transition of SLOAD, the input to the 4-bit DAC is locked to the state prior to when SLOAD went HIGH, and will set the EQualizer ENable bit. The DAC does not get programmed until SLOAD goes HIGH. The SLOAD pin must remain in a HIGH state to maintain the DAC Pre-Emphasis and the EQEN settings. A LOW or open state resets the DAC to 0db Pre-Emphasis setting and disables the EQEN bit, regardless of SDIN and SCLKIN values. The SLOAD function is asynchronous.

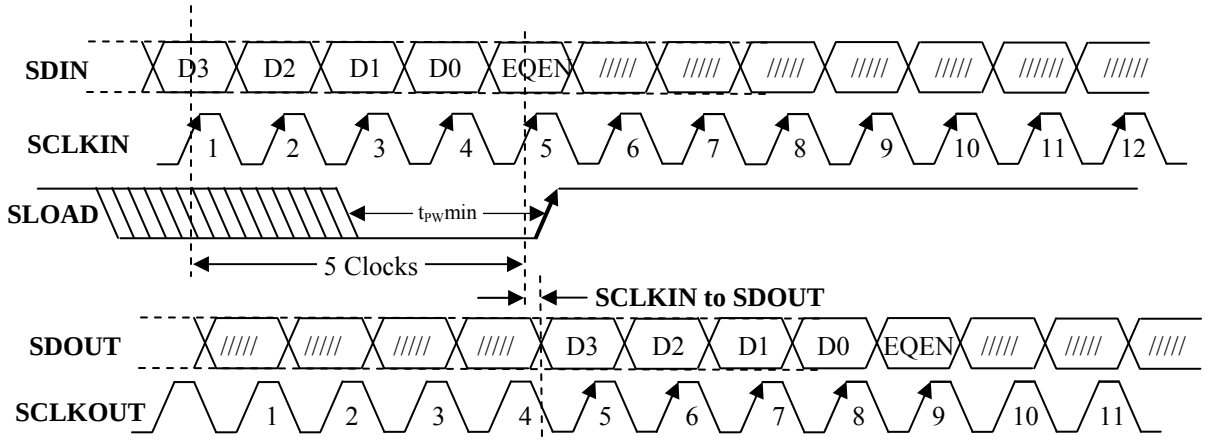


Figure 12. Timing Diagram for Single Channel

Pre-Emphasis Selection

The Pre-Emphasis buffer is controlled using a serial bus via the SDIN (Serial Data In) and SCLKIN (Serial Clock In) control inputs and contains circuitry which provides sixteen programmable pre-emphasis levels to control the output compensation. The 4-bits (D3:D0) digitally select 0 dB through 12 dB of Pre-Emphasis compensation (see Table 1). The default state at start-up is PE = 0dB.

EQualization ENable (EQEN)

The EQualizer ENable (EQEN) allows for enabling the Equalizer function. The control of the Equalizer function is realized by setting the 5th bit, EQEN, of the 5-bit serial data. When EQEN is set Low (or open), the IN/INb inputs bypass the Equalizer. When EQEN is set High, the IN/INb inputs flow through the Equalizer. The default state at start-up is EQEN = LOW.

Q / Qb Outputs

The differential output buffers of the NB7VPQ16M, Q and Qb, utilize Common Mode Logic (CML) architecture. The outputs are designed to drive differential transmission lines with nominal 50-Ω characteristic impedance. External termination with a 50-ohm resistor to VCC is required. See Figure 19 for output termination scheme.

Power Supply Bypass information

A clean power supply will optimize the performance of the NB7VPQ16M. The device provides VCC power supply pins for the digital circuitry and CML outputs. Placing a 0.01uF to 0.1uF bypass capacitor on each VCC pin to ground will help ensure a noise free VCC power supply. The purpose of this design technique is to isolate the CMOS digital switching noise from the high speed input/output path.

Cascade Application

SDOUT / SCLKOUT

SDOUT is the Serial Data output pin; SCLKOUT is the Serial Clock output pin. These pins are the outputs of the 5-bit shift register and will produce the SDIN / SCLKIN signals after five serial clock cycles, see Figure 13. The purpose of SDOUT and SCLKOUT is for use in cascade applications, described below.

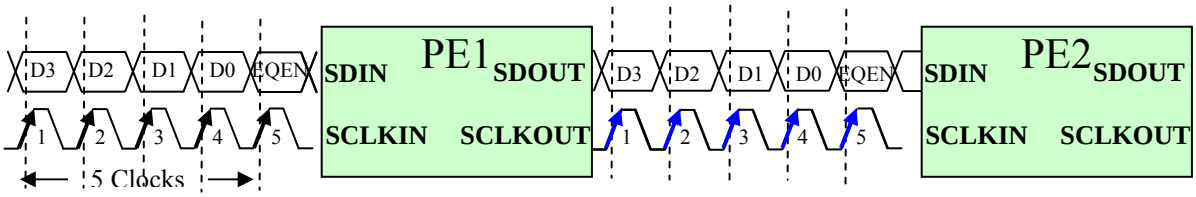


Figure 13. Simplified Cascaded Serial Data/Clock Timing Diagram

Cascaded Applications

The NB7VPQ16M can be cascaded with multiple NB7VPQ16Ms in series for various Equalizer / Pre-Emphasis applications, as shown in Figure 14.

Serial Data In, SDIN1, is clocked with SCLKIN1 into the cascaded chain of the Pre-Emphasis shift registers, (PE1, PE2 & PE3), 5-bits per register. Upon the rising edge of the 5th clock of SCLKIN1, the first valid data bit (D3) and 5th clock will exit PE1 from SDOUT1 and SCLKOUT1 and enter SDIN2 and SCLKIN2 of PE2….and so on with PE3.

When SLOAD is brought LOW, the PE shift registers of all devices are enabled and data is written into the NB7VPQ16Ms with the contents of the PE shift registers. When the data transfer is complete, SLOAD is brought HIGH and all NB7VPQ16Ms are updated simultaneously. After the PE control bits are clocked into their appropriate registers, the Low-to-High transition of SLOAD will latch the data bits for the Pre-Emphasis DACs.

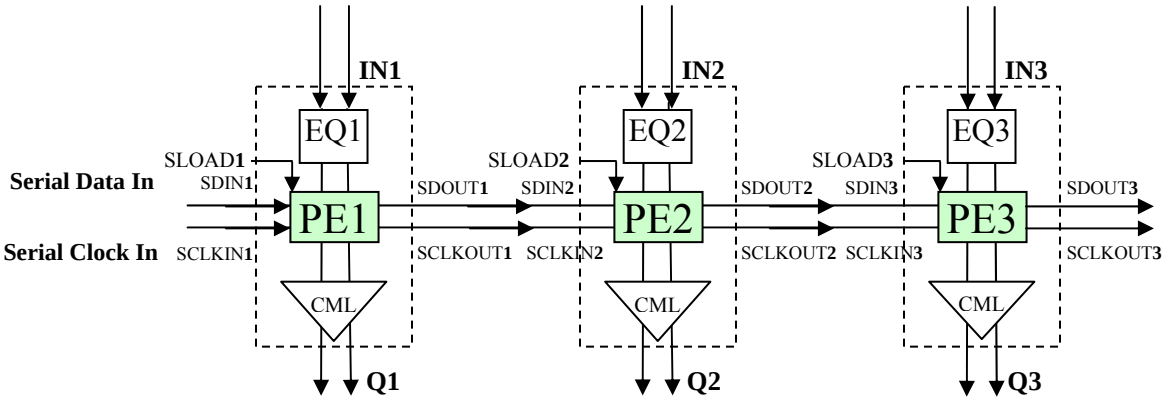


Figure 14. Simplified Cascaded Logic Diagram

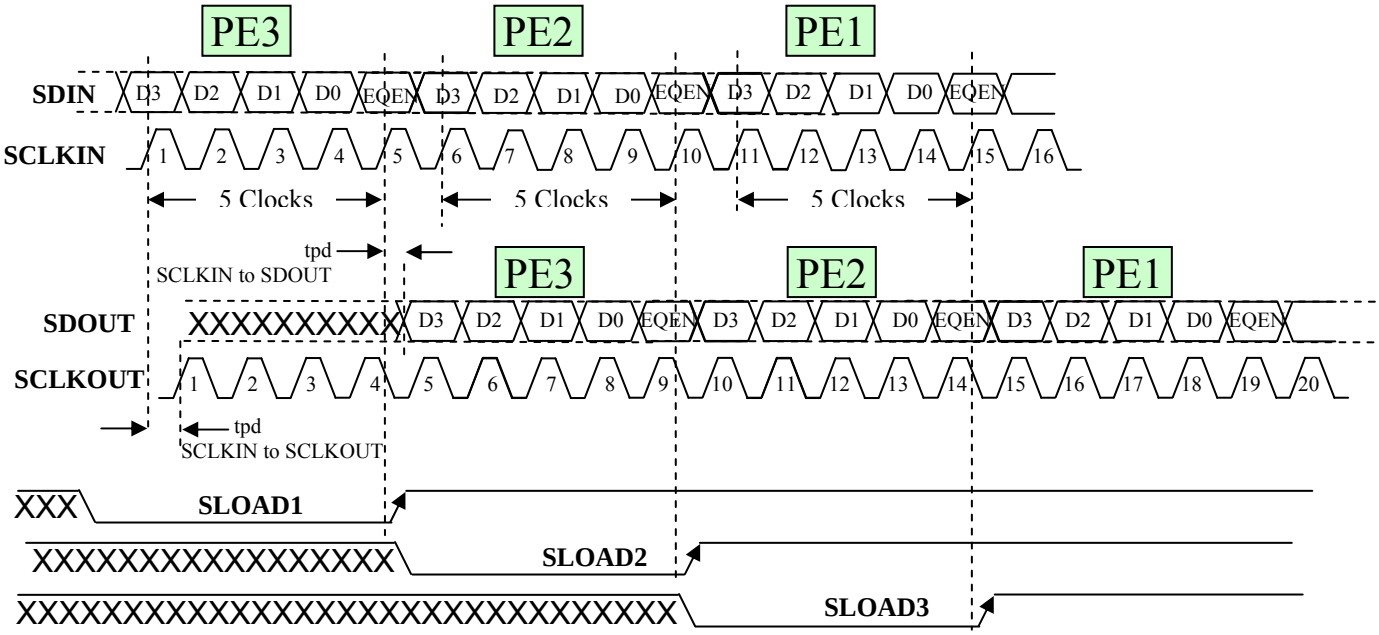


Figure 15. Simplified Cascaded Serial Data/Clock Timing Diagram

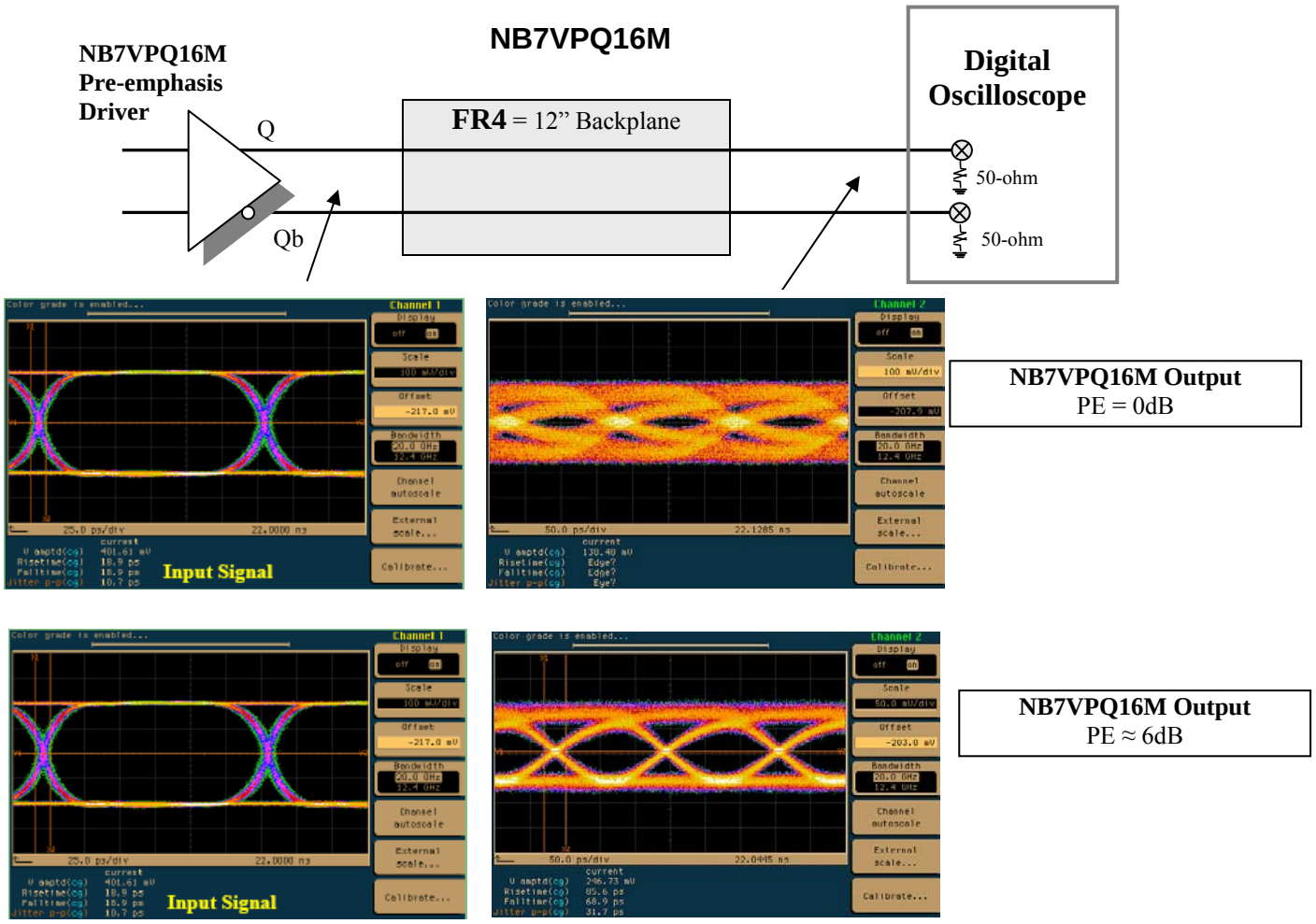


Figure 16. Typical NB7VPQ16M **PreEmphasis Application** at 6.5Gbps - Jitter Measurement Points, without and with pre-emphasis.

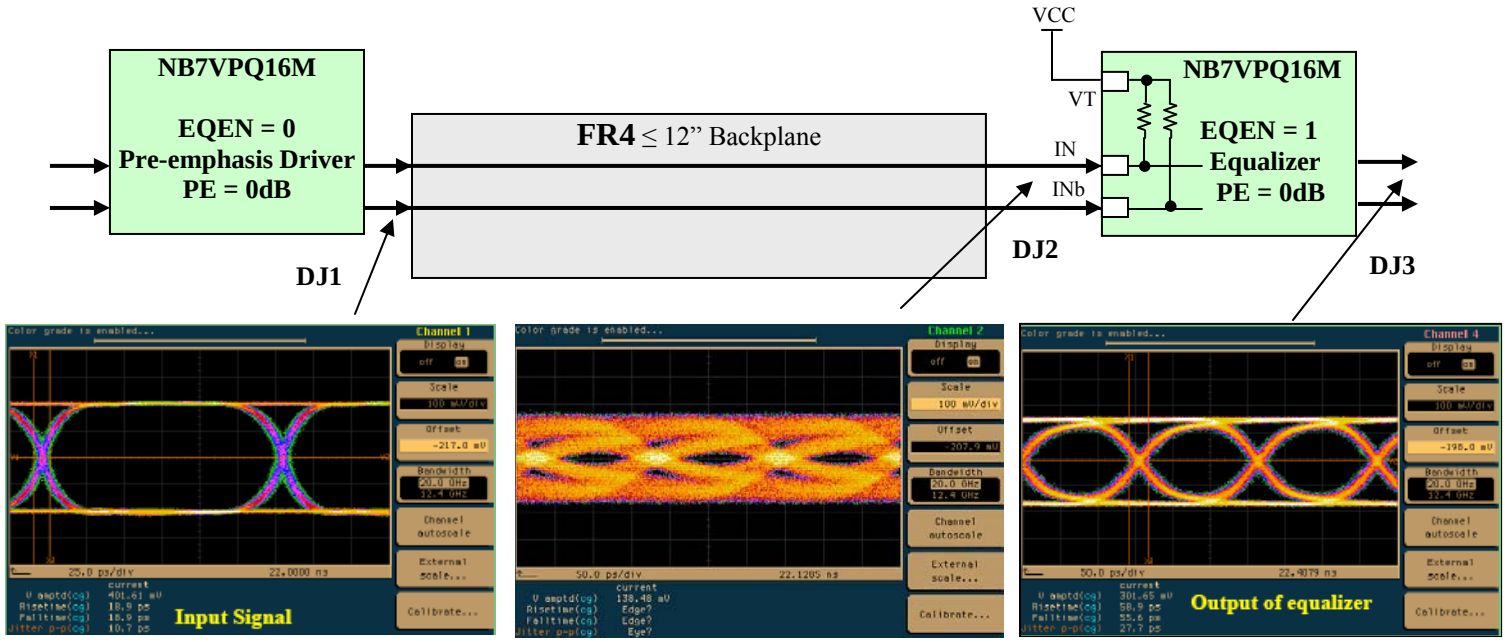


Figure 17. Typical NB7VPQ16M **Equalizer Application** and Interconnect with the NB7VPQ16M; PRBS23 pattern at 6.5Gbps

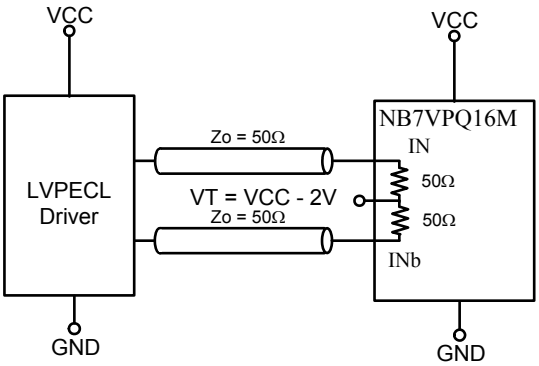


Figure __. LVPECL Interface

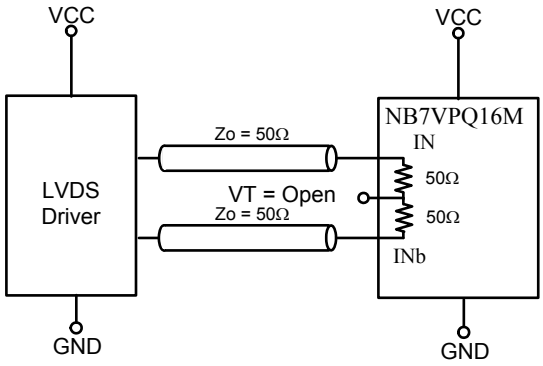


Figure __. LVDS Interface

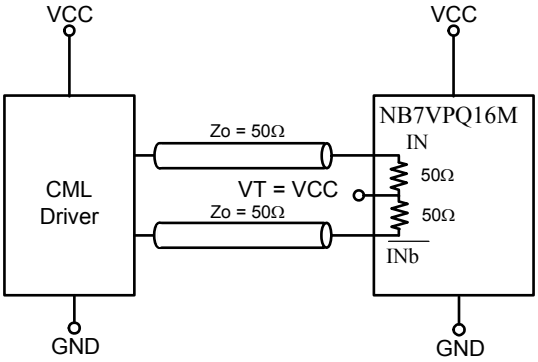


Figure __. Standard 50Ω Load CML Interface

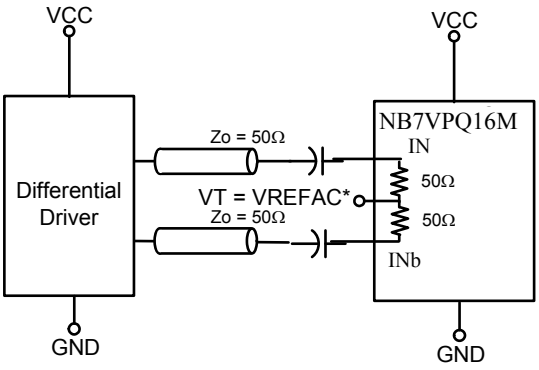


Figure __. Capacitor-Coupled Differential Interface (VT connected to external VREFAC)

* VREFAC bypassed to ground with a 0.01uF capacitor

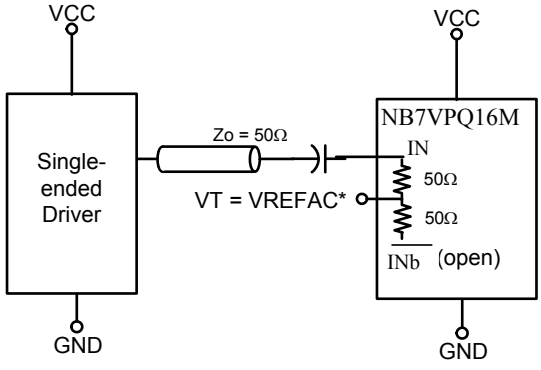


Figure __. Capacitor-Coupled Single-Ended Interface (VT connected to external VREFAC)

Figure 18. Input Interface

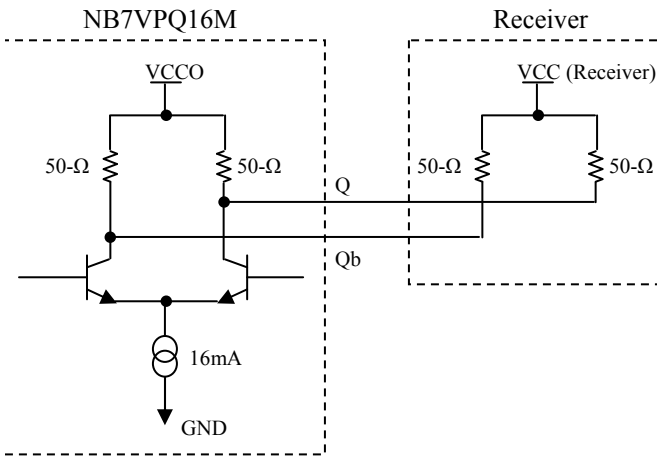


Figure 19. Typical CML Output Structure and Termination

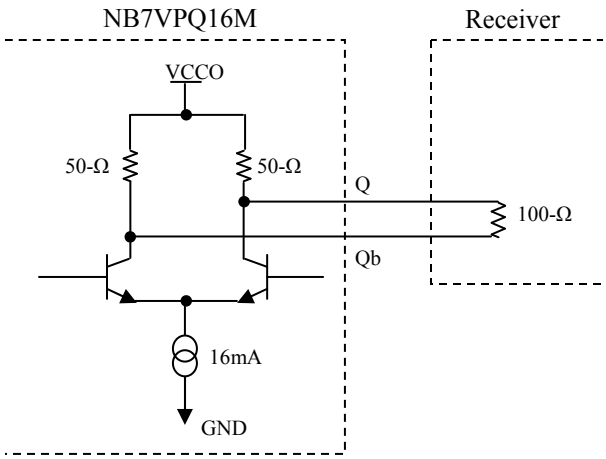


Figure 20. Alternative Output Termination

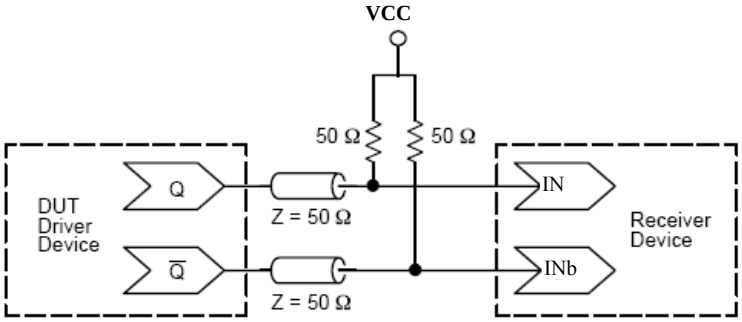


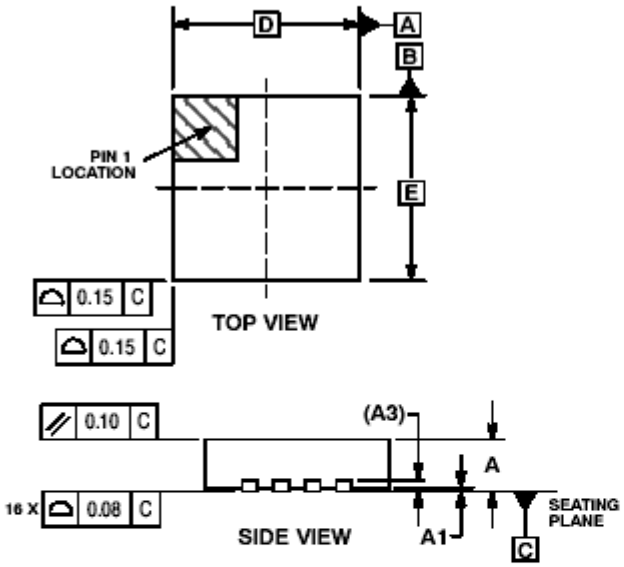
Figure 21. Typical Termination for Output Driver and Device Evaluation

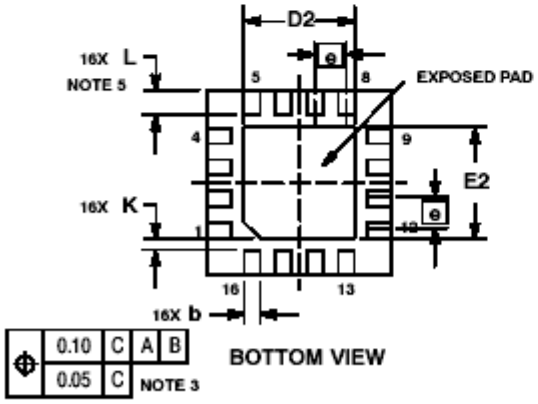
ORDERING INFORMATION

Device	Package	Shipping
NB7VPQ16MMNG	QFN-16 (Pb-free)	123 Units / (Rail)
NB7VPQ16MMNTXG	QFN-16 (Pb-free)	3000 / Tape & Reel

PACKAGE DIMENSIONS

16 PIN QFN
CASE 485G−01
ISSUE B

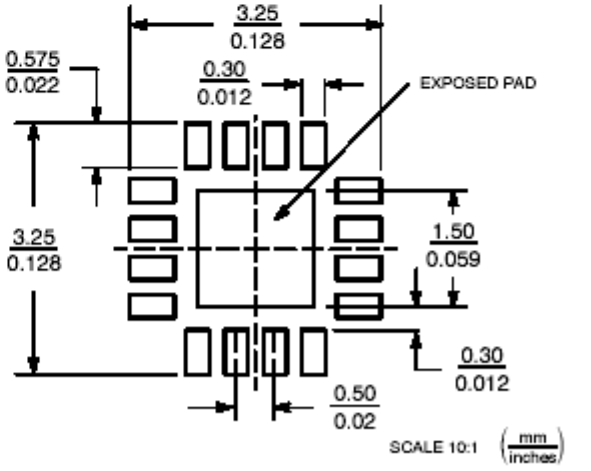




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

DIM	MILLIMETERS MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.