19-3315; Rev 0; 7/04

EVALUATION KIT AVAILABLE

Programmable Audio Clock Generator

General Description

The MAX9485 programmable multiple-output clock generator provides a cost-efficient solution for MPEG-2 audio systems such as DVD players, DVD drives for multimedia PCs, digital HDTV systems, home entertainment centers, and set-top boxes.

The MAX9485 accepts an input reference frequency of 27MHz from a crystal or system reference clock. The device provides two buffered clock outputs of 256, 384, or 768 times the chosen sampling frequency (f_S) selected through an I²C™ interface or hardwired inputs. Sampling frequencies of 12kHz, 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, or 96kHz are available. The MAX9485 also offers a buffered 27MHz output and an integrated voltage-controlled oscillator (VCXO) that is tuned by a DC voltage generated from the MPEG processor. The use of VCXO allows the audio system clock to lock with the overall system clock.

The MAX9485 features the lowest jitter in its class, guaranteeing excellent dynamic performance with audio ADCs and DACs in an MPEG-2 audio system. The device operates with a 3.3V supply and is specified over the -40°C to +85°C extended temperature range. The MAX9485 is offered in 6.5mm x 4.4mm 20-pin TSSOP and 4mm x 4mm 20-pin thin QFN packages.

Applications

Digital TVs

Set-Top Boxes

Home Entertainment Centers

DVD Players

HDTVs

Features

- **27MHz Crystal with ±30ppm Frequency Reference**
- **Two Buffered Output Ports with Multiple Audio Clocks: 256, 384, or 768 Times f_S**
- **Supports Standard and Double Sampling Rates (12kHz, 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2 kHz, and 96kHz)**
- **I²C Interface or Hardwired Output Clock Selection**
- **Separate Output Clock Enable**
- **Low Jitter Typical 21ps (RMS at 73.728MHz)**
- **No External Components for PLL**
- **Integrated VCXO with ±200ppm Tuning Range**
- **Small Footprint, Thin QFN Package, 4mm x 4mm**

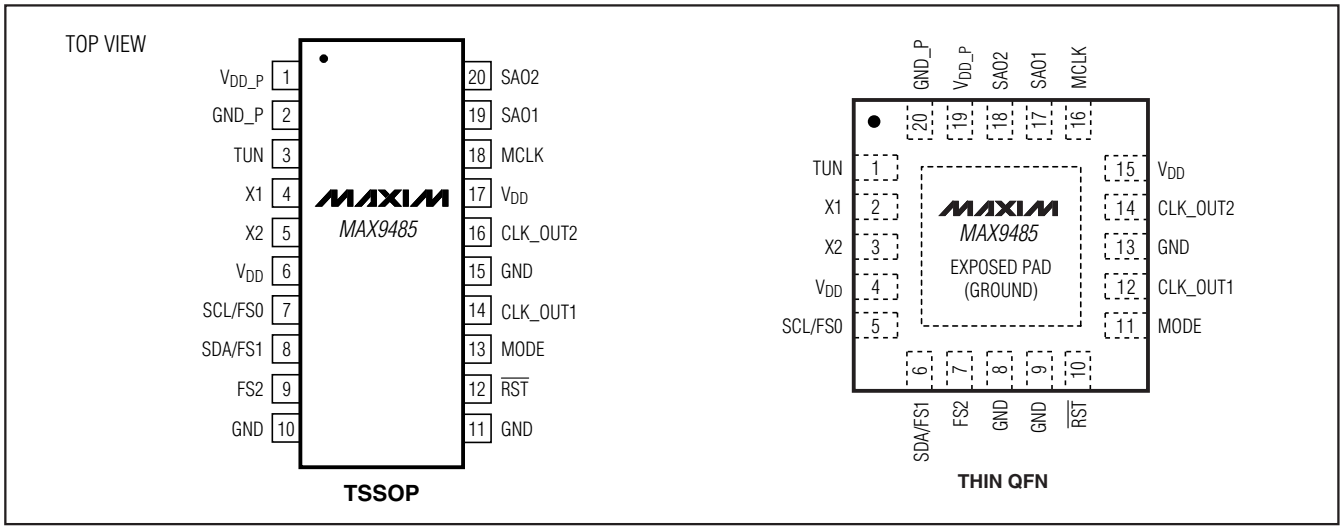
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9485ETP	-40°C to +85°C	20 Thin QFN-EP*
MAX9485EUP	-40°C to +85°C	20 TSSOP

*EP = Exposed pad.

I²C is a trademark of Philips Corp.
Purchase of I²C components of Maxim Integrated Products, Inc., or one of its sublicensed Associated Companies, conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Pin Configurations



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

V_{DD}, V_{DD_P} to GND .....-0.3V to +4.0V
GND_P to GND .....±0.3V
All Inputs and Outputs to GND.....-0.3V to (V_{DD} + 0.3V)
Short-Circuit Duration of Outputs to GND.....Continuous
Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP (derate 11mW/°C above +70°C) 879mW
20-Lead Thin QFN (derate 16.9mW/°C above +70°C).....1349mW
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
ESD Protection
Human Body Model (R_D = 1.5kΩ, C_S = 100pF).....> ±2kV
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{DD_P} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{DD} = V_{DD_P} = 3.3V.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVCMOS/LVTTL INPUTS (MODE, $\overline{RST}$, X1) (Note 2)						
High Level-Input Voltage	V_{IH1}		2.0		V_{DD}	V
Low Level-Input Voltage	V_{IL1}		0.0		0.8	V
Input Current	I_{IL1}	Input voltage = 0 or V_{DD}	-20		+20	µA
THREE-LEVEL INPUTS (FS0, FS1, FS2, SAO1, SAO2)						
High Level-Input Voltage	V_{IH2}		2.5		V_{DD}	V
Low Level-Input Voltage	V_{IL2}		0.0		0.8	V
Input Open Level	V_{IO2}	Input open	1.3		2.0	V
Input Current	I_{IN}	Input voltage = 0 or V_{DD}	-10		+10	µA
LVCMOS/LVTTL OUTPUTS (CLK_OUT1, CLK_OUT2, MCLK)						
Output High Level	V_{OH1}	I_{OH1} = -4mA	V_{DD} - 0.6			V
Output Low Level	V_{OL1}	I_{OL1} = 4mA			0.4	V
I^2C INTERFACE INPUT AND OUTPUT (SCL, SDA)						
Input High Level	V_{IH3}		0.7 x V_{DD}		V_{DD}	V
Input Low Level	V_{IL3}		0		0.3 x V_{DD}	V
Input Current	I_{IN}	Input voltage = 0 or V_{DD}	-1		+1	µA
Low-Level Output	V_{OL3}	I_{OL3} = 4mA			0.4	V
Input Capacitance	C_{IN}			8.4		pF
POWER SUPPLY (V_{DD}, V_{DD_P})						
Power-Supply Ranges	V_{DD}, V_{DD_P}		3.0	3.3	3.6	V
Power-Supply Current	I_{DD}+I_{DD_P}	CLK_OUT1, CLK_OUT2 at 73.728MHz, no load, V_{TUN} = 3.0V		12		mA

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{DD_P} = 3.0V to 3.6V, T_A = -40°C to +85°C, output frequency is 73.728MHz, C_L = 20pF, unless otherwise noted. Typical values are at T_A = +25°C, V_{DD} = V_{DD_P} = 3.3V.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VCXO (MCLK)							
Crystal Frequency	f_{XTL}	Nominal frequency			27		MHz
Crystal Accuracy					±30		ppm
Tuning Voltage Range	V_{TUN}			0		3.0V	V
VCXO Tuning Range		V_{TUN} = 0 to 3.0V		-200		+200	ppm
TUN Input Impedance	R_{TUN}				94		kΩ
Output Clock Frequency	f_{MCLK}	V_{TUN} = 1.75V			27		MHz
Output Clock Accuracy		V_{TUN} = 1.75V (Note 4)			±50		ppm
Output Duty Cycle				45	55	65	%
Output Jitter	t_{MJ}	RMS			28		ps
Output Rise Time	t_{MR}	Figure 8			2		ns
Output Fall Time	t_{MF}	Figure 8			2		ns
Tuning Response Time	t_{TUN}	Figure 9			10		µs
Power-On Settling Time	T_{PO1}	Figure 9			5		ms
CLOCK OUTPUTS (CLK_OUT1, CLK_OUT2)							
Frequency Range (Note 5)	f_{out}	256 x f_S		8.192		24.576	MHz
		384 x f_S		12.288		36.864	
		768 x f_S		24.576		73.728	
Clock Rise Time	t_{R1}	Figure 8			2		ns
Clock Fall Time	t_{F1}	Figure 8			2		ns
Duty Cycle				45	50	55	%
Output Clock Period Jitter	t_{RJ}	RMS	CLK_OUT1, 2 at 73.728MHz (Note 6)		21		ps
			CLK_OUT1, 2 at 36.864MHz		37		
Frequency Settling Time	t_{FST}	Figure 1			10		ms
Power-On Time	T_{PO2}	Figure 9			15		ms

I²C TIMING CHARACTERISTICS

(V_{DD} = V_{DD_P} = 3.0V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, V_{DD} = V_{DD_P} = 3.3V; Figure 7.) (Note 1)

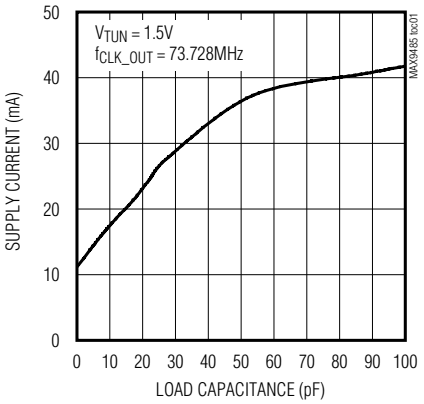
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock	f_{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD, STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU, STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU, STO}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$	(Note 7)	0.05		0.9	µs
Data Setup Time	$t_{SU,DAT}$		100			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.6			µs
Rise Time of SDA and SCL, Receiving	t_R	(Notes 3, 8)	20 + 0.1Cb		300	ns
Fall Time of SDA and SCL, Receiving	t_F	(Notes 3, 8)	20 + 0.1Cb		300	ns
Fall Time of SDA, Transmitting	t_F	(Notes 8, 9)	20 + 0.1Cb		250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Notes 3, 10)	0		50	ns
Capacitive Load for Each Bus Line	C_b				400	pF

Note 1: All parameters tested at T_A = +25°C. Specifications over temperature are guaranteed by design and characterization.
Note 2: When X1 is used as an external reference.
Note 3: Guaranteed by design and characterization; limits are set at ±6 sigma.
Note 4: Includes crystal accuracy.
Note 5: F_{XTL} = 27MHz. Nominal frequency.
Note 6: See frequency selection paragraph in the *Applications Information* section.
Note 7: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
Note 8: C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.3 V_{DD} and 0.7 V_{DD}.
Note 9: Bus sink current is less than 6mA. C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.3 V_{DD} and 0.7 V_{DD}.
Note 10: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

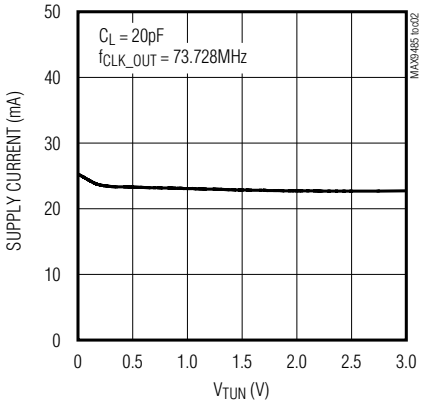
Typical Operating Characteristics

(V_{DD} = V_{DD_P} = 3.3V, T_A = +25°C.)

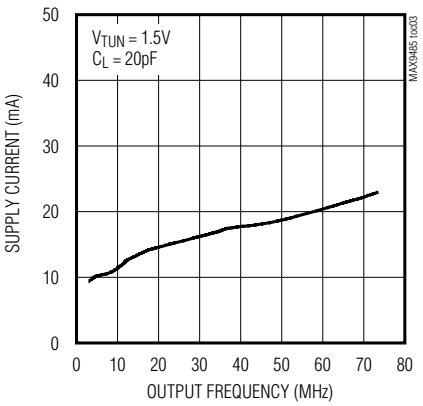
SUPPLY CURRENT vs. LOAD CAPACITANCE



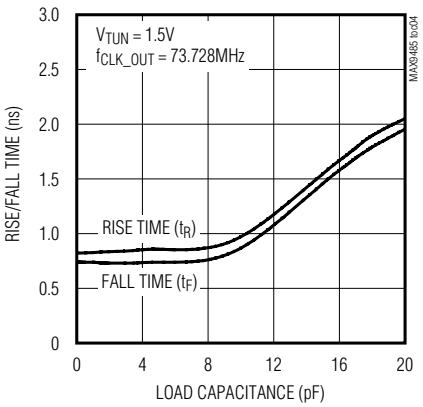
SUPPLY CURRENT vs. V_{TUN}



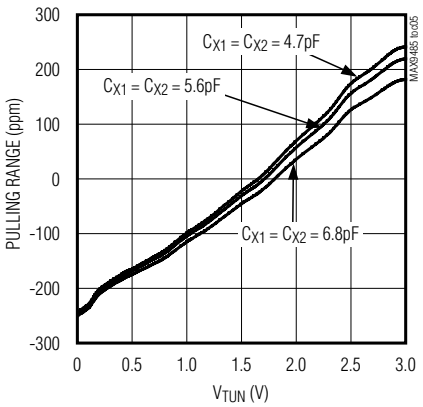
SUPPLY CURRENT vs. OUTPUT FREQUENCY



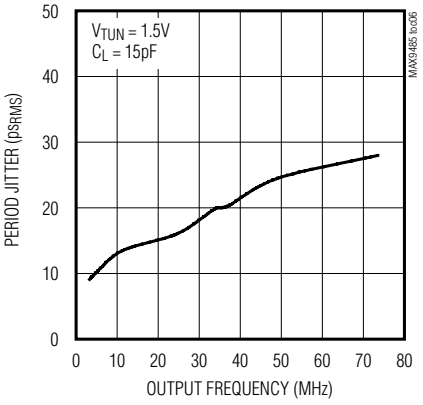
OUTPUT CLOCK RISE/FALL TIME vs. LOAD CAPACITANCE



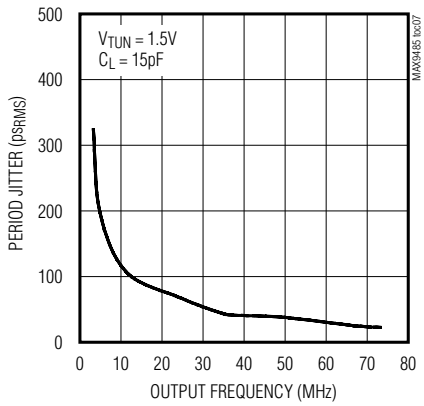
MCLK PULLING RANGE vs. V_{TUN}



MCLK PERIOD JITTER vs. OUTPUT FREQUENCY



CLK_OUT PERIOD JITTER vs. OUTPUT FREQUENCY

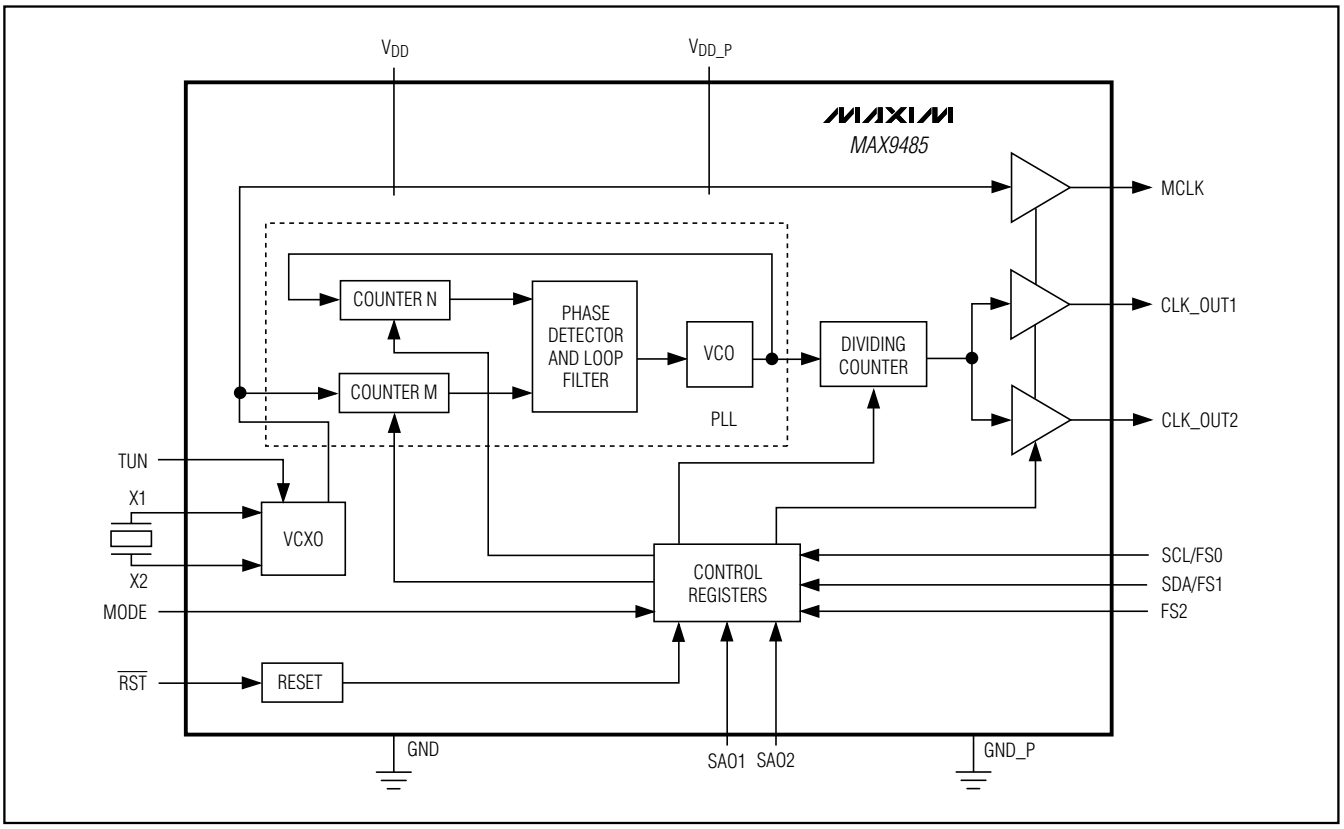


Programmable Audio Clock Generator

Pin Description

PIN		NAME	FUNCTION
TSSOP	TQFN		
1	19	V_{DD_P}	PLL Power Supply. Bypass V_{DD_P} with a 0.1µF and 0.001µF capacitor to GND_P.
2	20	GND_P	PLL Ground
3	1	TUN	VCXO Tuning Voltage Input. Apply 0 to 3V at TUN to adjust the VCXO frequency. Connect TUN to V_{DD} when driving X1 directly with a 27MHz input reference clock.
4	2	X1	Crystal Connection 1. Connect a fundamental mode crystal between X1 and X2 for use as a VCXO, or drive X1 directly with a 27MHz input reference clock.
5	3	X2	Crystal Connection 2. Connect a fundamental mode crystal between X1 and X2 for use as a VCXO, or leave X2 unconnected when driving X1 with a 27MHz system reference clock.
6, 17	4, 15	V_{DD}	Digital Power Supply. Bypass V_{DD} with a 0.1µF and 0.001µF capacitor to GND.
7	5	SCL/FS0	Serial Clock/Function Selection Input 0. When MODE = low, SCL/FS0 functions as the I^2C serial clock input. When MODE = high, SCL/FS0 functions as a three-level input to select sampling frequency.
8	6	SDA/FS1	Serial Data I/O/Function Selection Input 1. When MODE = low, SDA/FS1 functions as the I^2C serial data input/output. When MODE = high, SDA/FS1 functions as a three-level input to select output frequency scaling factor.
9	7	FS2	Function Selection Input 2. When MODE = high, FS2 functions as a three-level input to select sampling rate. When MODE = low, voltage levels at FS2 do not affect device operation.
10, 11, 15	8, 9, 13	GND	Ground
12	10	$\overline{RST}$	Reset Input. Drive $\overline{RST}$ low resets the I^2C register to its default state. $\overline{RST}$ is internally pulled to V_{DD}.
13	11	MODE	Mode Control Input. When MODE = low, the I^2C interface is active. When MODE = high, the hardwired interface is active, and function selection is programmed by SCL/FS0, SDA/FS1, and FS2. Mode is internally pulled to GND.
14	12	CLK_OUT1	Output Clock Port 1. CLK_OUT1 operates at 256/384/768f_S, depending on the function selection. CLK_OUT1 is pulled low when disabled.
16	14	CLK_OUT2	Output Clock Port 2. CLK_OUT2 operates at 256/384/768f_S, depending on the function selection. CLK_OUT2 is pulled low when disabled.
18	16	MCLK	Master System Clock Buffered Output. MCLK outputs the 27MHz clock generated by the internal VCXO. MCLK is pulled low when disabled.
19	17	SAO1	I^2C Device Address Selection Input 1 or MCLK Output Enable Control Input. When MODE = low, SAO1 is a three-level I^2C device address programming input. When MODE = high, SAO1 controls MCLK enable/disable.
20	18	SAO2	I^2C Device Address Selection Input 2 or CLK_OUT Output Enable Control Input. When MODE = low, SAO2 is a three-level I^2C device address programming input. When MODE = high, SAO2 controls CLK_OUT1 and CLK_OUT2 enable/disable.
—	Exposed Pad	EP	Exposed Pad. Connect EP to ground.

Functional Diagram



Detailed Description

The MAX9485 uses an input reference frequency of 27MHz from a crystal or system reference clock. The device provides two buffered clock outputs of 256, 384, or 768 times the chosen sampling frequency (f_S) selected through an I^2C interface or hardwired inputs. Sampling frequencies of 12kHz, 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, or 96kHz are available. The MAX9485 offers a buffered 27MHz output and an integrated VCXO tuned by a DC voltage generated from the MPEG system. The device operates with a 3.3V supply.

Reference and Output Clock

The MAX9485 uses the 27MHz crystal or reference clock (master clock) from the audio system and generates an output of 256, 384, or 768 times the audio system sampling frequency (f_S). Connect a fundamental mode crystal between X1 and X2 or drive X1 with a 27MHz system clock. The choices of sampling frequencies are 12kHz, 32kHz, 44.1kHz, 48kHz, 64kHz, 88.2kHz, and 96kHz. The MAX9485 offers two identical outputs: CLK_OUT1 and CLK_OUT2. In the following, the CLK_OUT is used to refer to both outputs. Table 1 shows the relations of f_S and the output frequency. Select the output frequency by programming the I^2C register or hardwiring inputs FS0, FS1, and FS2. CLK_OUT settling is typically 15ms from power-on or from applying the clock to X1. Delay time from sampling frequency change to CLK_OUT settling is 10ms (typ). Figure 1 illustrates CLK_OUT transient timing in the I^2C programmed case. The I^2C register is set through a master-write data transfer. The frequency settling time t_{FST} is counted from the end of the next ACK pulse of the written byte in SDA until the CLK_OUT is settled.

Table 1. Sampling Frequency and Output Clock

SAMPLING FREQUENCY	CLK_OUT			SAMPLING RATE
f_S (kHz)	256 x f_S (MHz)	384 x f_S (MHz)	768 x f_S (MHz)	
12	3.072	4.608	9.126	Standard
32	8.1920	12.2880	24.5760	Standard
44.1	11.2896	16.9344	33.8688	Standard
48	12.2880	18.4320	36.8640	Standard
64	16.3840	24.5760	49.1520	Double
88.2	22.5792	33.8688	67.7376	Double
96	24.5760	36.8640	73.7280	Double

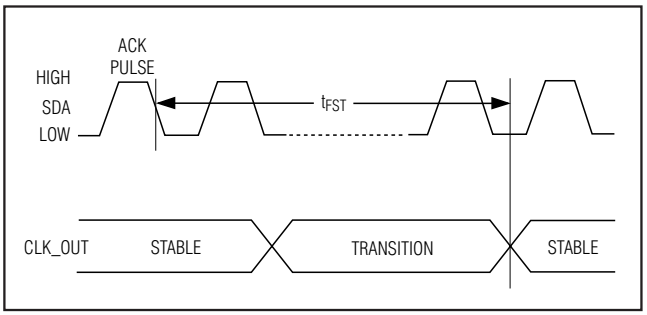


Figure 1. CLK_OUT Transient Timing

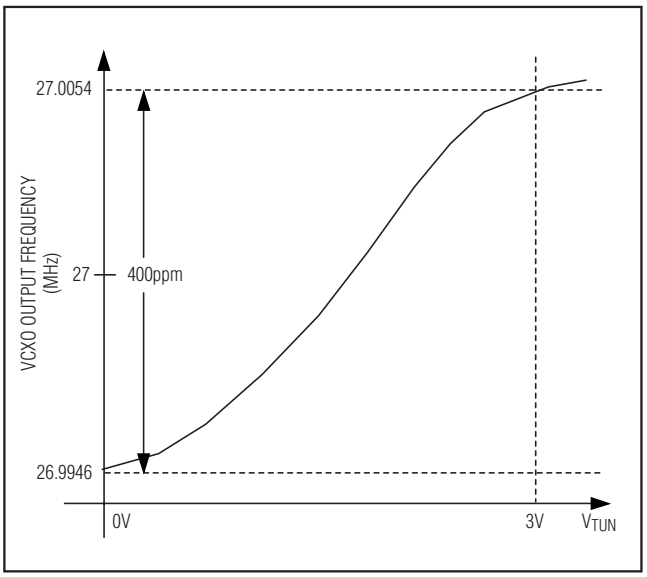


Figure 2. VCXO Tuning Range

Voltage-Controlled Crystal Oscillator (VCXO)

The MAX9485 internal VCXO produces a 27MHz reference clock for the PLL used to generate CLK_OUT1 and CLK_OUT2. The oscillator uses a 27MHz crystal as the base frequency reference and has a voltage-controlled tuning input for micro adjustment in a range of ±200ppm. The tuning voltage V_{TUN} can vary from 0 to 3V as shown in Figure 2. Use an AT-cut crystal that oscillates at 27MHz on its fundamental mode with ±30ppm. Use a crystal shunt capacitor less than 12pF, including board parasitic capacitance. Choose an oscillator with a load capacitance less than 14pF to achieve ±200ppm pullability. VCXO, a free-run oscillator, and the buffered output MCLK are not affected by power-on reset and external reset. VCXO has a 5ms settling time at power-on and 10µs at a change of the V_{TUN} voltage.

The MAX9485 can be used as a synthesizer with a 27MHz input reference clock. For this mode, connect the 27MHz input clock to X1. Connect TUN to V_{DD} and leave X2 open. This configuration is for applications where the micro tuning is not needed and there is a 27MHz system master clock available.

Chip Reset Function

The MAX9485 has an internal reset function. The device resets at power-up or can be externally reset by driving $\overline{RST}$ low. The reset function sets the registers to default values. MODE sets the device's programming mode at power-up. When MODE = low, the device is set to software-programmable mode. Set MODE = high for hardwired mode. If MODE = low, the reset sets default values for CLK_OUT1 and CLK_OUT2 to 256 x f_S with f_S = 32kHz. If MODE = high, the reset sets CLK_OUT1 and CLK_OUT2, according to the values of the hardwired inputs.

The internal power-on reset completes after 1024 cycles of the reference clock starting when V_{DD} is greater than 2.2V with a tolerance of ±0.4V. When using the internal power-on reset, $\overline{RST}$ must be high. Figure 3 shows power-on reset timing. The internal reset function also accepts an external forced reset by driving $\overline{RST}$ = low. The reset is triggered when $\overline{RST}$ = low and completes after 1024 reference clock cycles. When a reset is initiated, any pulses on $\overline{RST}$ during the 1024 reference clock cycles are ignored. If $\overline{RST}$ is held low at the end of a reset cycle, reset does not initiate until a high-to-low transition is detected at $\overline{RST}$. Figure 4 shows external reset timing.

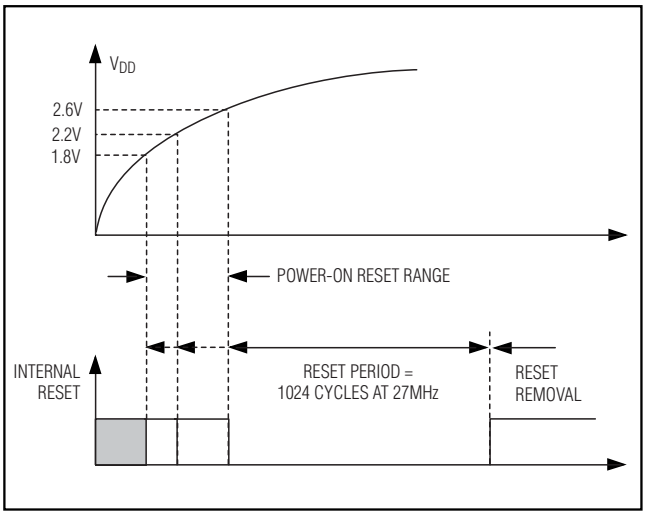


Figure 3. Power-On Reset Timing

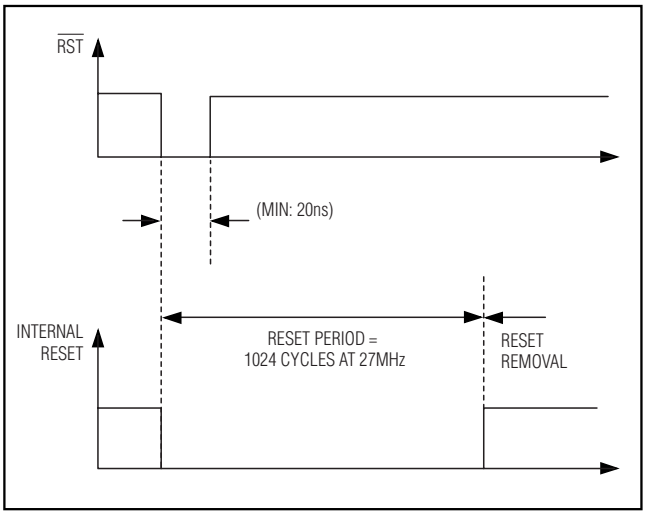


Figure 4. External Reset Timing

Software and Hardwire Control Modes

The MAX9485 sampling frequency, sampling rate, and clock outputs can be programmed through the I^2C 2-wire interface (software mode, MODE = low), or hardwired directly through three-level inputs (hardwire mode, MODE = high). The offered functions for each mode are shown in Table 2. CLK_OUT and MCLK are pulled low when disabled.

Hardwire Mode Programming (MODE = High)

In hardwire mode, FS2 selects the sampling rate (Table 3). With FS2 = low, the sampling rate is standard. With FS2 = high, the sampling rate is doubled. When FS2 = open, the 12kHz standard rate is selected, overriding the setting of FS0. FS1 selects the scaling factors: 256, 384, and 768 (Table 4). FS0 selects the sample frequencies: 32kHz, 44.1kHz, and 48kHz (Table 5).

When MODE = high, inputs SAO1 and SAO2 enable or disable the clock outputs (Tables 6 and 7). CLK_OUT and MCLK are pulled low when disabled.

Table 2. Selectable Functions

FUNCTIONS	HARDWIRE MODE MODE = HIGH	SOFTWARE MODE MODE = LOW
Standard sampling frequencies: 12kHz, 32kHz, 44.1kHz, 48kHz	✓	✓
Double sampling frequencies: 64kHz, 88.2kHz, 96kHz	✓	✓
CLK_OUT1, CLK_OUT2, MCLK: enable/disable	✓	✓

Table 3. Sampling Rate Selection

FS2	SAMPLING RATE
Low	Standard (32kHz, 44.1kHz, 48kHz)
High	Doubled (64kHz, 88.2kHz, 96kHz)
Open	Standard (12kHz)

Table 4. Frequency Scaling Factors

FS1	OUTPUT SCALING FACTOR
Low	256
High	384
Open	768

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Table 5. Selection of Sampling Frequency

FS0	SAMPLING FREQUENCY (kHz)
Low	32
High	44.1
Open	48

Table 6. MCLK Enable/Disable Control

SAO1	MCLK
Low	Disabled
High	Enabled
Open	Reserved

Table 7. CLK_OUT Enable/Disable Control

SAO1	SAO2	CLK_OUT1	CLK_OUT2
High/low	Open	Enabled	Enabled
High/low	Low	Enabled	Disabled
High/low	High	Disabled	Enabled

Software Mode Programming (MODE = Low)

In software mode, the I²C interface writes or reads an 8-bit control register in the MAX9485. The control register controls the rate settings and the clock outputs. Since there is only one register in the MAX9485, no address is assigned to this register. The device has a programmable 7-bit address for the I²C bus, selected by SAO1 and SAO2 (Table 8). At power-up with MODE = low, the MAX9485 reads the state of SAO1 and SAO2, then latches the I²C device address. Table 9 shows the control register bit mapping. Bit C7 enables the MCLK output. Bits C5 and C6 enable the clock outputs CLK_OUT1 and CLK_OUT2, respectively. Bit C4 selects the sampling rates. Bits C3 and C2 choose the output frequency-scaling factor. Bits C1 and C0 determine the sampling frequency. The details are shown in Tables 10–14.

Serial Interface

The MAX9485 control interface uses a 2-wire I²C serial interface. The device operates as a slave that sends and receives data through clock line SCL and data line SDA to achieve bidirectional communication with the master. A master (typically a microcontroller) initiates all data transfers to and from the MAX9485, and generates the SCL clock that synchronizes the data transfer. The

Table 8. Register Address Selection

SAO1	SAO2	I²C DEVICE ADDRESS
Open	Open	110 0000
Low	Open	110 0011
High	Open	110 0010
Open	Low	110 0100
Low	Low	110 1000
High	Low	111 0000
Open	High	111 0001
Low	High	111 0010
High	High	111 0100

Table 9. Control Register Bit Mapping

BIT	FUNCTION
C7	MCLK enable/disable
C6, C5	CLK_OUT2, CLK_OUT1 enable/disable
C4	Sampling-rate selection
C3, C2	Frequency-scaling factors
C1, C0	Sampling-frequency selection

Table 10. MCLK Enable/Disable Control

C7	MCLK
0	Disabled
1	Enabled

Table 11. CLK_OUT1, 2 Enable/Disable Control

C6	C5	CLK_OUT2	CLK_OUT1
1	1	Enabled	Enabled
1	0	Enabled	Disabled
0	1	Disabled	Enabled
0	0	Disabled	Disabled

Table 12. Sampling Rate Selection

C4	SAMPLING RATE
0	Standard
1	Doubled

Table 13. Frequency Scaling Factors

C3	C2	OUTPUT SCALING FACTOR
0	0	256
0	1	384
1	0	768
1	1	Reserved

Table 14. Sampling Frequency Selection

C1	C0	SAMPLING FREQUENCY (kHz)
0	0	12
0	1	32
1	0	44.1
1	1	48

Note: *(C1, C0) = (0, 0) and C4 = 1 (double) is not a proper selection. However, when set, it selects 12kHz sampling frequency.*

SDA line operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDA. The SCL line operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the 2-wire bus, or if the master in a single-master system has an open-drain SCL output.

Start and Stop Conditions

Both SCL and SDA remain high when the interface is idle. The active master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. After communication, the MAX9485 issues a STOP (P) condition by transitioning SDA from low to high while SCL is high, freeing the bus for another transmission (Figure 5). If a START or STOP occurs while a bus transaction is in progress, then it terminates the transaction.

Data Transfer and Acknowledge

Following the START condition, each SCL clock pulse transfers 1 bit. For the MAX9485 interface, between a START and a STOP, 18 bits are transferred on the 2-wire bus. The first 7 bits are for the device address. Bit 8 indicates the writing (low) or reading (high) operation (R/$\overline{W}$). Bit 9 is the ACK for the address and operation type. Bits 10 though 17 form the data byte. Bit 18 is the ACK for the data byte. The master always transfers

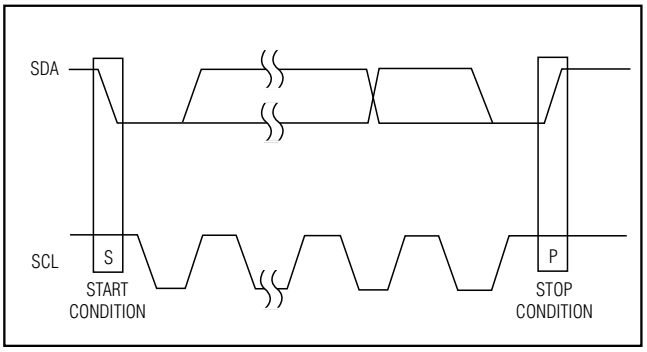


Figure 5. Start and Stop Conditions

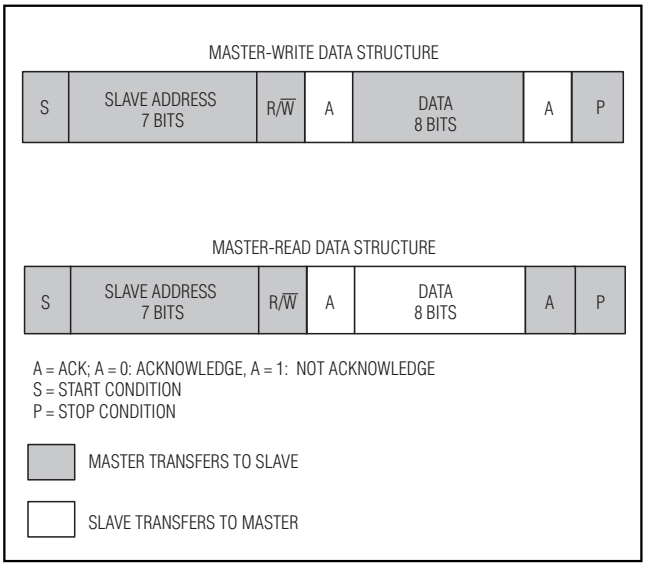


Figure 6. Serial Interface Data Structure

the first 8 bits (address + R/$\overline{W}$). The slave (MAX9485) can receive the data byte from the bus or transfer it to the bus from the internal register. The ACK bits are transmitted by the address or data recipient. A low ACK bit indicates a successful transfer (Acknowledge), a high ACK bit indicates an unsuccessful transfer (Not Acknowledge). Figure 6 shows the structure of the data transfer. During a write operation, if more synchronous data is transferred, it overwrites the data in the register. During a read operation, if more clocks are reset on SCL, the SDA continues to respond to the register data.

Programmable Audio Clock Generator

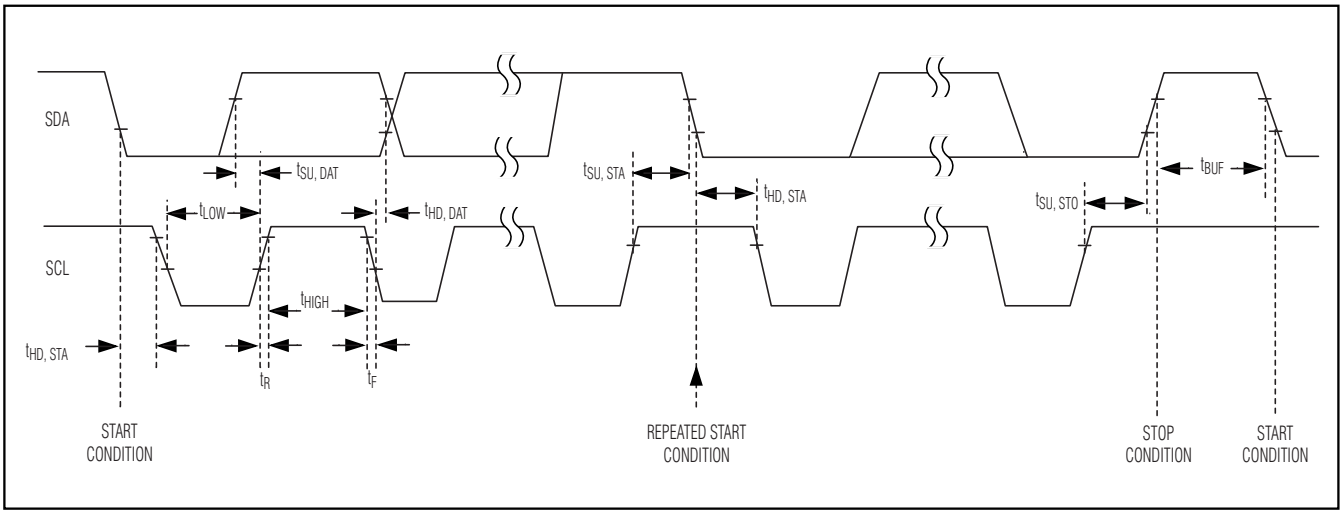


Figure 7. 2-Wire Serial Interface

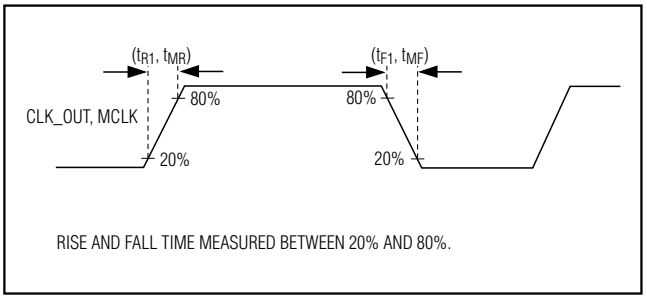


Figure 8. CLK_OUT, MCLK Rise and Fall Time

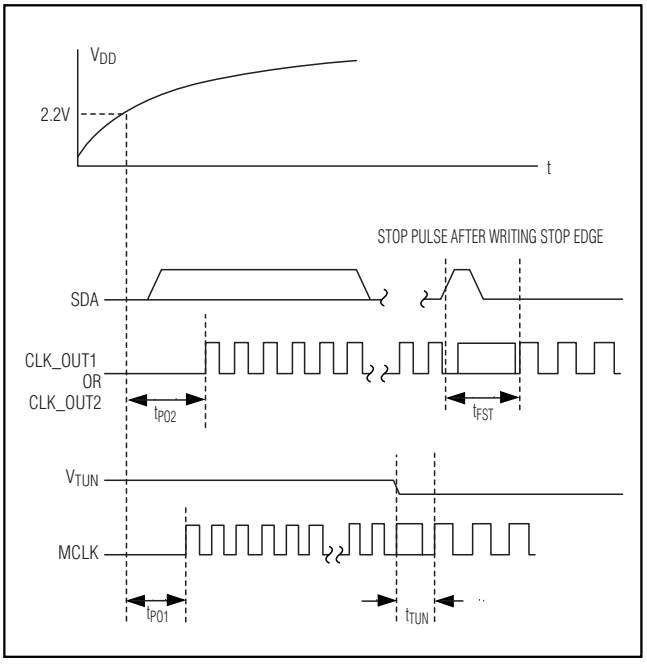


Figure 9. VCXO and PLL Settling Time

Applications Information

Crystal Selection

When using the MAX9485's internal VCXO with an external crystal, connect the crystal to X1 and X2. Choose an AT-cut crystal that oscillates at 27MHz on its fundamental mode with ±30ppm. Use a crystal shunt capacitance less than 12pF, including board parasitic capacitance. Choose an oscillator with a load capacitance less than 14pF to achieve ±200ppm pullability. **Note:** Pulling range may vary depending on the crystal used. Refer to the MAX9485 Evaluation Kit for details.

Output CLK Frequency Setting with Low Jitter

A specific frequency could be achieved through multiple settings (Table 1) such as different sampling rate and multiplication factors (256, 384, and 768). However, due to the difference of internal structure, the CLK outputs jitter may be different for each setting. Table 15 lists CLK output frequencies and jitter for the various settings. For best performance, the user should choose the setting that gives the lowest jitter at a specific frequency.

Power-Supply Bypassing and Ground Management

The MAX9485's high oscillator frequency makes proper layout important to ensure stability. For best performance, place components as close as possible to the device.

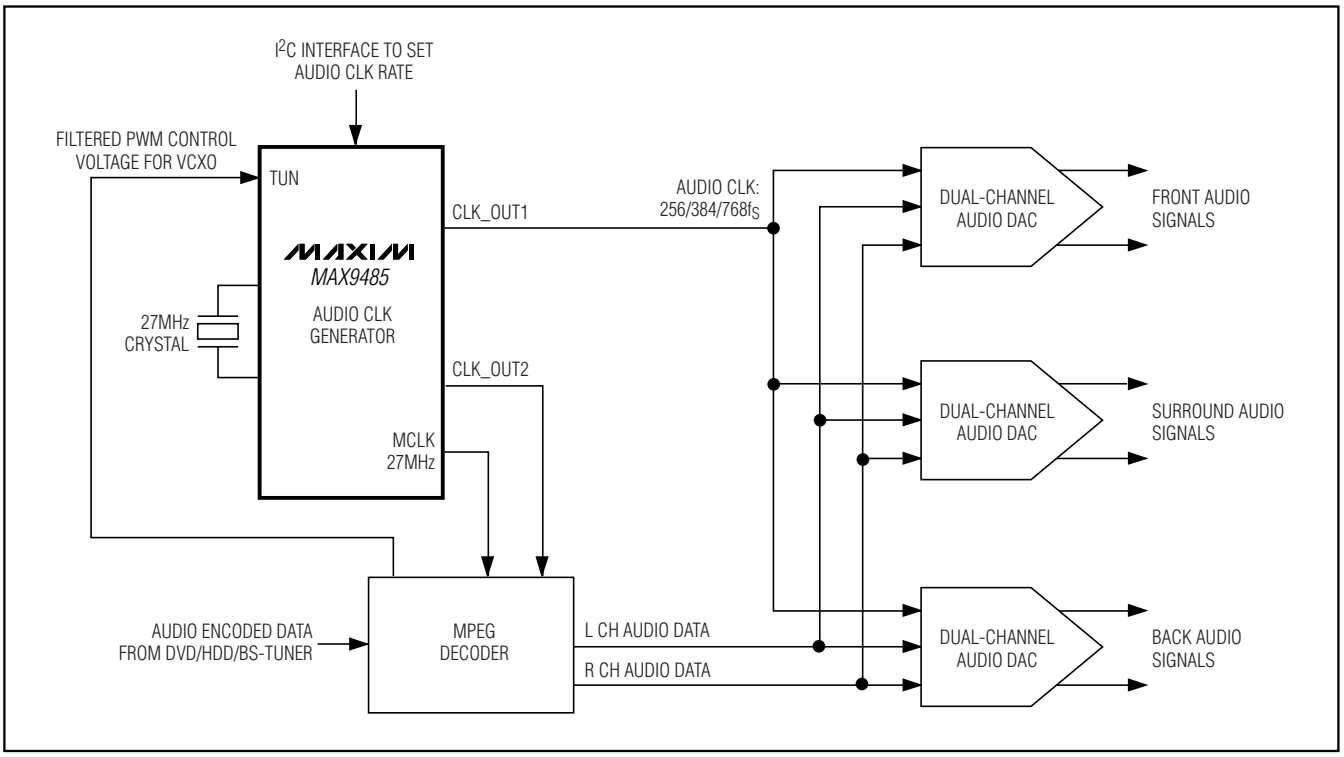
Digital or AC transient signals on GND can create noise at the clock output. Return GND to the highest-quality ground available. Bypass V_{DD} and V_{DD_P} with 0.1µF and 0.001µF capacitors, placed as close to the device as possible. Careful PC board ground layout minimizes crosstalk between the outputs and digital inputs.

Table 15. Jitter Measurements of Output CLKs

FOUT (MHz)	SCALING FACTOR	f_S (kHz)	$T_{RJ(RMS)}$ (ps)
73.728	768	96	21
67.7376	768	88.2	23.2
49.152	768	64	42.6
36.864	768	48	40
36.864	384	96	37
33.8688	768	44.1	44
33.8688	384	88.2	41.3
24.5760	768	32	66
24.5760	384	64	92
24.5760	256	96	50
22.5792	256	88.2	55.1
18.4320	384	48	59
16.9344	384	44.1	69
16.3840	256	64	134
12.2880	256	48	84.8
12.2880	384	32	170
11.2896	256	44.1	100
9.126	768	12	106
8.1920	256	32	250
4.608	384	12	198
3.072	256	12	324

Programmable Audio Clock Generator

Typical Application Circuit



Chip Information

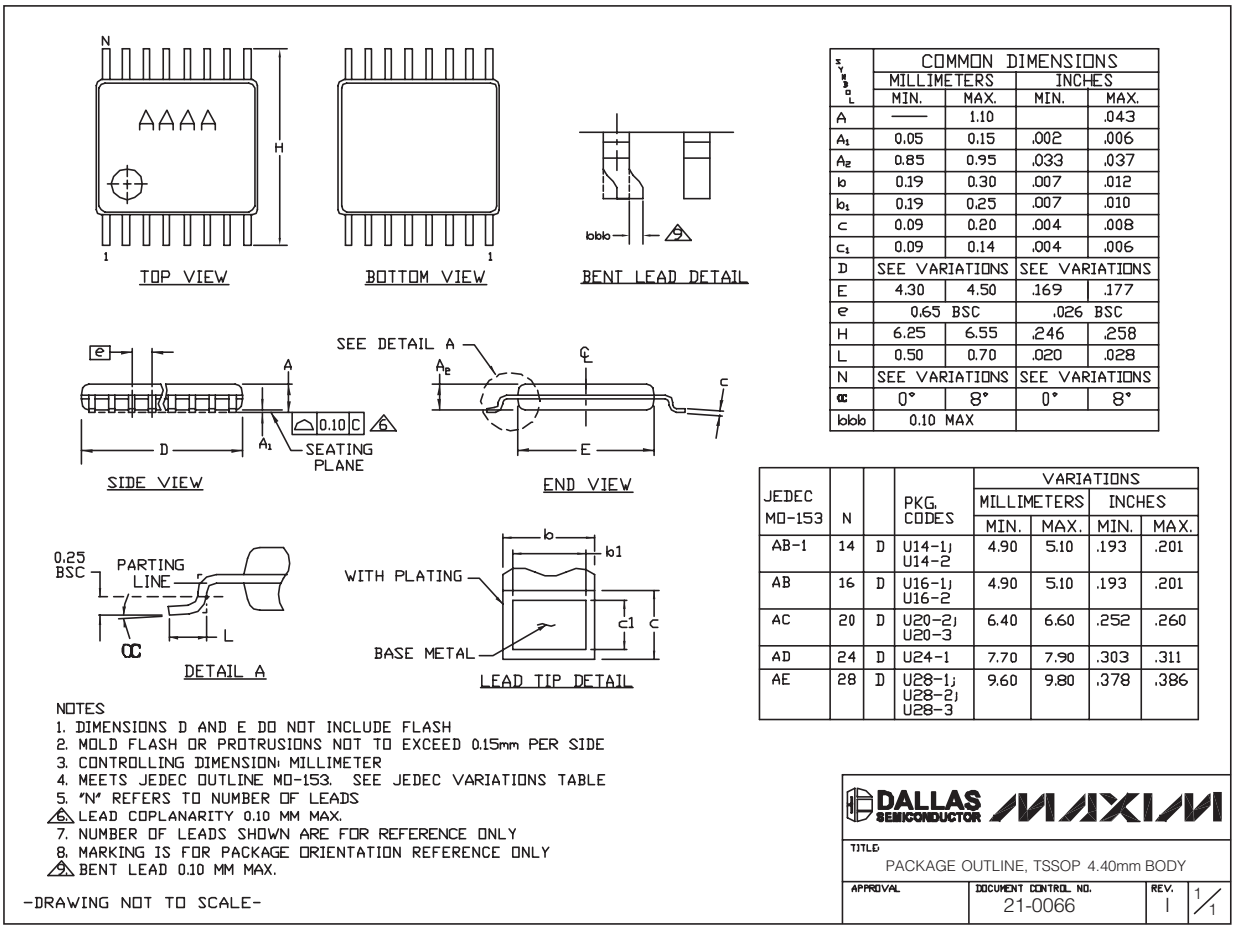
TRANSISTOR COUNT: 9817

PROCESS: CMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
bbb	0.10 MAX			

JEDEC MO-153	N		PKG. CODES	VARIATIONS			
				MILLIMETERS		INCHES	
				MIN.	MAX.	MIN.	MAX.
AB-1	14	D	U14-1, U14-2	4.90	5.10	.193	.201
AB	16	D	U16-1, U16-2	4.90	5.10	.193	.201
AC	20	D	U20-2, U20-3	6.40	6.60	.252	.260
AD	24	D	U24-1	7.70	7.90	.303	.311
AE	28	D	U28-1, U28-2, U28-3	9.60	9.80	.378	.386

NOTES
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. LEAD COPLANARITY 0.10 MM MAX.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
9. BENT LEAD 0.10 MM MAX.

-DRAWING NOT TO SCALE-

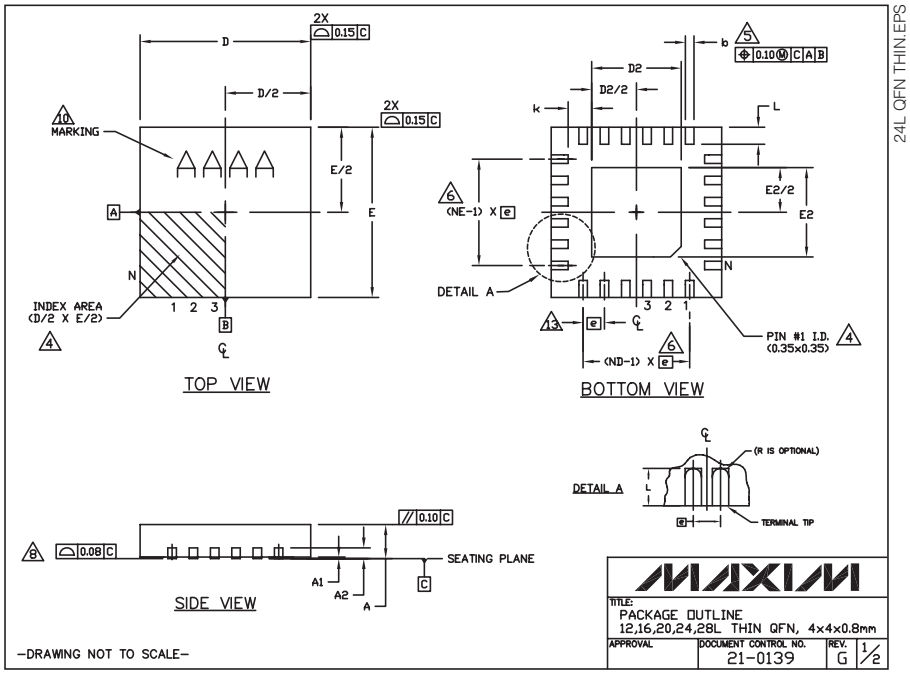
DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	I	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. ALL DIMENSIONS ARE THE SAME FOR LEADED (–) & PbFREE (+) PACKAGE CODES.

–DRAWING NOT TO SCALE–

MAXIM
TITLE:
PACKAGE OUTLINE
12,16,20,24,28L THIN QFN, 4x4x0.8mm
APPROVAL
DOCUMENT CONTROL NO.
21-0139
REV.
G
2/2