19-4187; Rev 0; 7/08

High-Current VCOM Drive Op Amps for TFT LCDs

General Description

The MAX9650/MAX9651 are single- and dual-channel VCOM amplifiers with rail-to-rail inputs and outputs. The MAX9650/MAX9651 can drive up to 1300mA of peak current per channel and operate up to 20V.

The MAX9650/MAX9651 are designed to source and sink a high current quickly to hold the VCOM voltage stable in large TFT-LCD panels.

The MAX9650/MAX9651 feature 40V/µs slew rate and 35MHz bandwidth to quickly settle outputs for 120Hz frame rate and full HD television.

The MAX9650/MAX9651 feature output short-circuit protection and thermal shutdown. These devices are available in exposed pad packages for excellent heat dissipation.

Applications

TFT-LCD Panels

Instrument Control Voltage Sources

Features

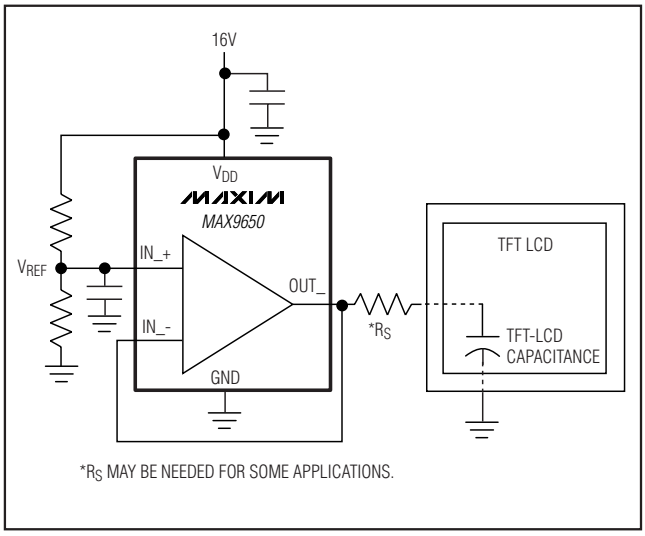
- **1300mA Peak Output Current**
- **Rail-to-Rail Inputs and Outputs**
- **Operates Up to 20V**
- **35V/µs Slew Rate**
- **35MHz Bandwidth**
- **5mA Quiescent Current per Channel**
- **Excellent Heat Dissipation (Exposed Pad)**

Ordering Information

PART	AMPS PER PACKAGE	PIN-PACKAGE	TOP MARK
MAX9650AZK+	1	5 SOT23	ADSI
MAX9650AUA+	1	8 µMAX-EP*	AABI
MAX9651AUA+	2	8 µMAX-EP*	AABH

Note: *All devices are specified over the -40°C to +125°C operating range.*
+Denotes a lead-free/RoHS-compliant package.
**EP = Exposed pad.*

Typical Operating Circuit



High-Current VCOM Drive Op Amps for TFT LCDs

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to GND) .....-0.3V to +22V
Any Other Pin to GND .....-0.3V to (V_{DD} + 0.3V)
IN_+/IN_- (current).....±20mA
OUT_ (current) 1.3A
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 3.7 mW/°C above +70°C).....297.4mW
8-Pin µMAX-EP (derate 12.9mW/°C above +70°C).....1030.9mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 19V, V_{GND} = 0, V_{CM} = V_{OUT} = V_{DD}/2, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by PSRR		6		20	V
Quiescent Current	I_{DD}	Per channel			3.7	8	mA
High Output Voltage	V_{OH}	I_H = +5mA, V_{IN} = V_{DD}		V_{DD} - 0.30	V_{DD} - 0.05		V
Low Output Voltage	V_{OL}	I_L = -5mA, V_{IN} = 0			0.05	0.30	V
Input Offset Voltage	V_{OS}	T_A = +25°C		-14	3.5	+14	V
		T_A = -40°C to +125°C		-17		+17	
Load Regulation	LR	I_{OUT} = 0 to -80mA			+0.2		mV/mA
		I_{OUT} = 0 to +80mA			-0.2		
Input Bias Current	I_{FB}	At V_{IN} = 9.5V			0.01	1	µA
Voltage Gain	A_V	A_V = 1V/V, R_L = 10kΩ, C_L = 50pF		0.99		1.01	V/V
Power-Supply Rejection Ratio	PSRR	V_{DD} = 6V to 20V, V_{CM} = V_{OUT} = 3V		70	95		dB
Common-Mode Input Voltage Range	CMVR	Inferred from CMRR test		0.5		V_{DD} - 0.5	V
Common-Mode Rejection Ratio	CMRR	0.5V ≤ V_{CM} ≤ V_{DD} - 0.5V		60	80		dB
Continuous Output Current	I_O	V_{OUT} = 9.5V (Note 2)	MAX9650AZK+	20			mA
			MAX965_AUA+	80			
Transient Peak Output Current	I_{PK}	(Note 3)			±1.3		A
Bandwidth	BW	-3dB			35		MHz
Slew Rate	SR	4V step, C_L = 50pF, R_L = 10kΩ, A_V = +1V/V			40		V/µs
Settling Time	t_S	Settling to 0.1% of V_{OUT}, I_L = 0 to 1000mA, R_S = 2.2Ω, C_S = 0.1µF (Figure 1)			2.0		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 19V, V_{GND} = 0, V_{CM} = V_{OUT} = V_{DD}/2, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

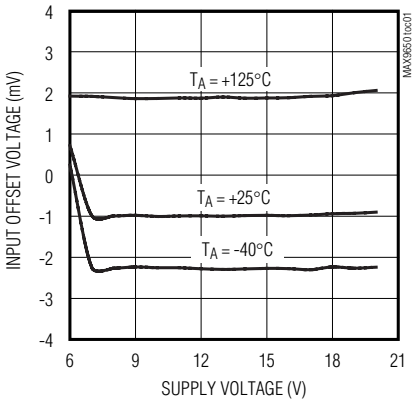
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Load Capacitance	C_{LOAD}	(Note 4)		150		nF
Noninverting Input Resistance	R_{IN+}	(Note 5)		100		MΩ
Inverting Input Resistance	R_{IN-}	(Note 5)		100		MΩ
Input Capacitance	C_{IN}			3		pF
Thermal Shutdown				+170		°C
Thermal Shutdown Hysteresis				15		°C

Note 1: All devices are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 2: Continuous output current is tested with one output at a time.
Note 3: See the *Thermal Shutdown with Temperature Hysteresis* section.
Note 4: A series resistor can extend load capacitance range. The settling time can be optimized by a small series resistance. See the *Applications Information* section for more information.
Note 5: Inputs are protected by back-to-back diodes.

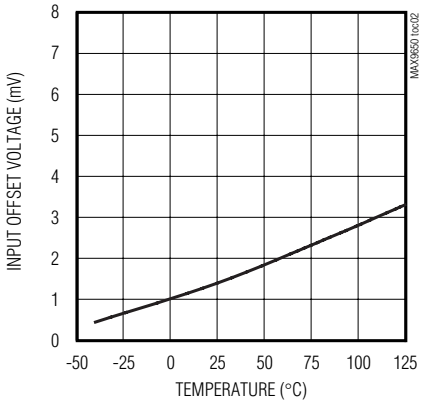
Typical Operating Characteristics

(V_{DD} = 19V, GND = 0, V_{CM} = V_{OUT} = V_{DD}/2, T_A = +25°C, unless otherwise specified.)

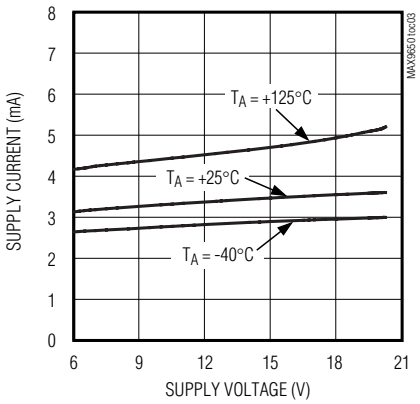
INPUT OFFSET VOLTAGE DEVIATION vs. SUPPLY VOLTAGE



INPUT OFFSET VOLTAGE DEVIATION vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE

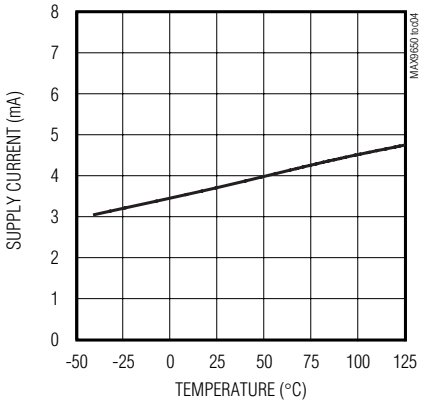


High-Current VCOM Drive Op Amps for TFT LCDs

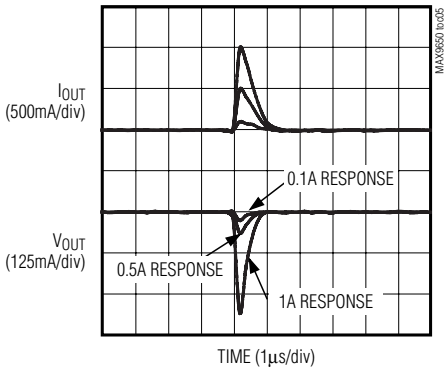
Typical Operating Characteristics (continued)

(V_{DD} = 19V, GND = 0, V_{CM} = V_{OUT} = V_{DD}/2, T_A = +25°C, unless otherwise specified.)

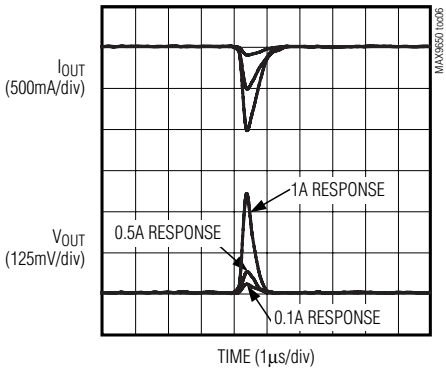
SUPPLY CURRENT vs. TEMPERATURE



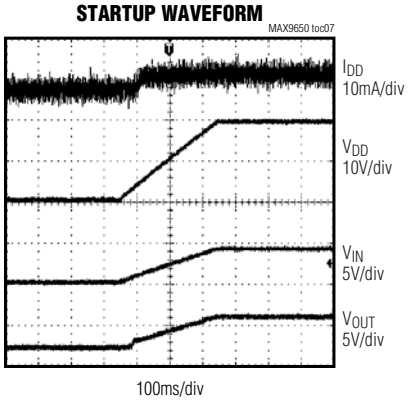
LOAD TRANSIENT SOURCING



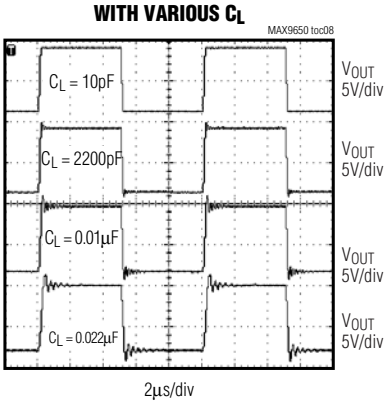
LOAD TRANSIENT SINKING



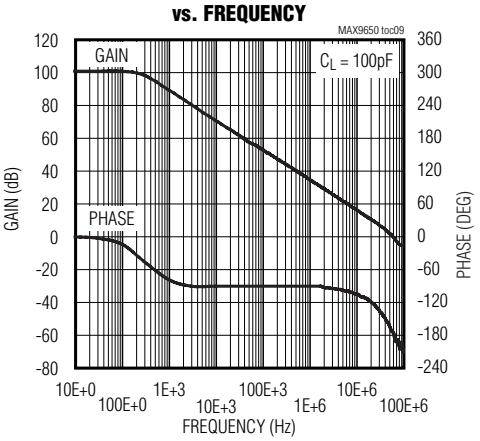
STARTUP WAVEFORM



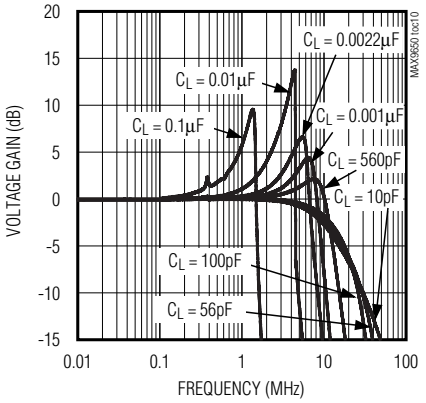
MAX9560 STEP RESPONSE WITH VARIOUS C_L



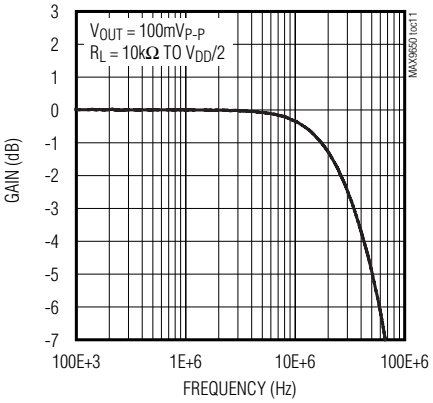
OPEN-LOOP GAIN AND PHASE vs. FREQUENCY



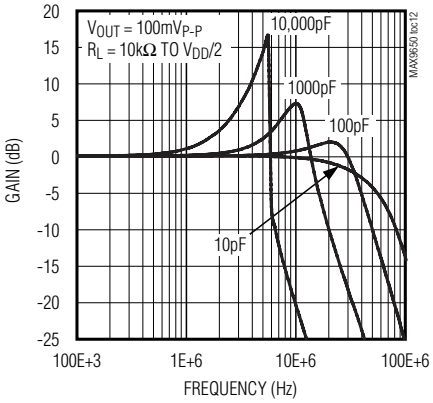
CLOSED-LOOP SMALL-SIGNAL FREQUENCY RESPONSE FOR VARIOUS C_L



SMALL-SIGNAL GAIN vs. FREQUENCY



SMALL-SIGNAL GAIN vs. FREQUENCY WITH VARIOUS C_L



Pin Description

PIN			NAME	FUNCTION
MAX9650		MAX9651		
SOT23	µMAX			
1	6	1	OUTA	VCOM Output A
2	4	4	GND	Ground
3	3	3	INA+	Positive Input A
4	2	2	INA-	Negative Input A
5	7	8	V_{DD}	Positive-Supply Input. Bypass V_{DD} to GND with a 0.1µF capacitor as close as possible to the device.
—	—	5	INB+	Positive Input B
—	—	6	INB-	Negative Input B
—	—	7	OUTB	VCOM Output B
—	1, 5, 8	—	N.C.	No Connection. Not internally connected.
—	—	—	EP	Exposed Pad. EP is internally connected to GND. Connect EP to GND.

Detailed Description

The MAX9650/MAX9651 operational rail-to-rail input/output amplifiers hold the VCOM voltage stable while providing the ability to source and sink a high current quickly (1.3A) into a capacitive load such as the backplane of a TFT-LCD panel.

Thermal Shutdown with Temperature Hysteresis

The MAX9650/MAX9651 are capable of high output currents and feature thermal-shutdown protection with temperature hysteresis. When the die temperature reaches +170°C, the device shuts down. When the die cools down by 15°C, the device turns on again. In a TFT-LCD application, the duty cycle is very low. Even with high values of voltage and current, the power dissipation is low and the chip does not shut down.

Applications Information

Output Load

The MAX9650/MAX9651 are designed to drive capacitive loads. A small value of series resistance improves the performance of the device to ensure stability and fast settling with very large or very small capacitive loads. In many cases, this resistance is already present due to connection resistance in the wiring and no additional physical resistor is necessary.

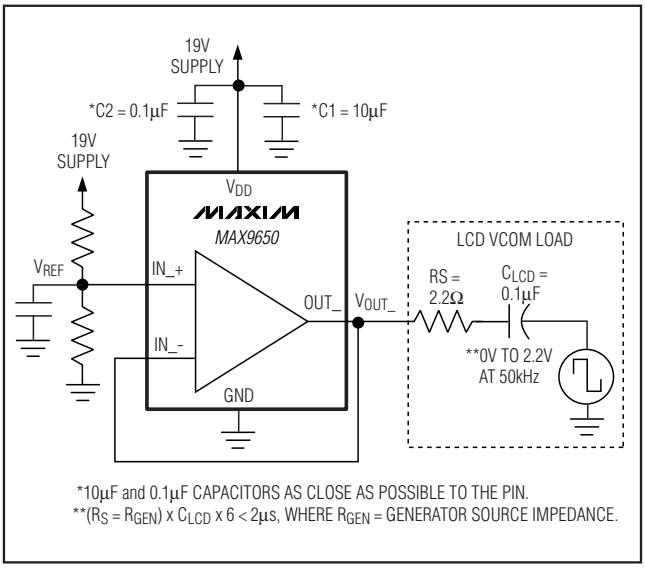


Figure 1. Settling Time Test Circuit

Power Supplies and Bypass Capacitors

The MAX9650/MAX9651 operate from a 9V to 20V single supply or from ±4.5V to ±10V dual supplies. Proper supply bypassing ensures stability while driving high transient loads. The MAX9650/MAX9651 require a minimum 10µF (C1) and 0.1µF (C2) power-supply bypass capacitors placed as close as possible to the power-supply pin

High-Current VCOM Drive Op Amps for TFT LCDs

(V_{DD}). See Figure 2. For dual-supply operation, use 10µF and 0.1µF bypass capacitors on both supplies (V_{DD} and GND) with each capacitor placed as close as possible to V_{DD} and GND.

Layout and Grounding

The exposed pad on the µMAX package provides a low thermal resistance for heat dissipation. Solder the exposed pad to a ground plane for best thermal performance. Do not route traces under these packages. For dual-supply operation, the exposed pad (EP) can be electrically connected to the negative supply or it can be left unconnected.

Chip Information

PROCESS: BiCMOS

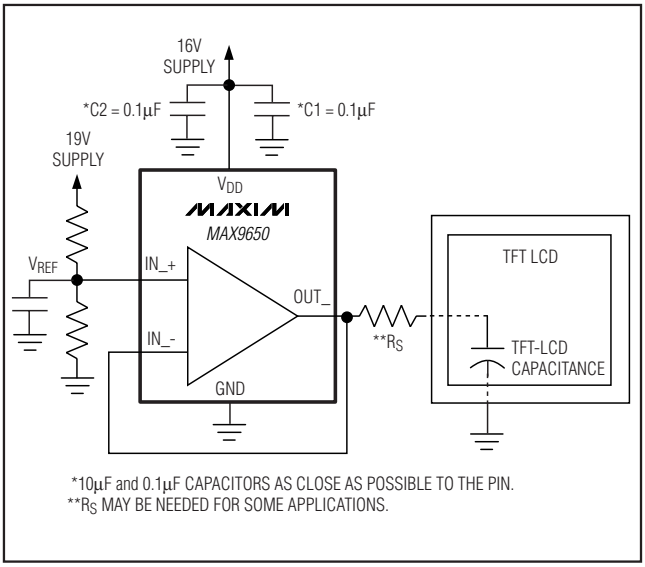
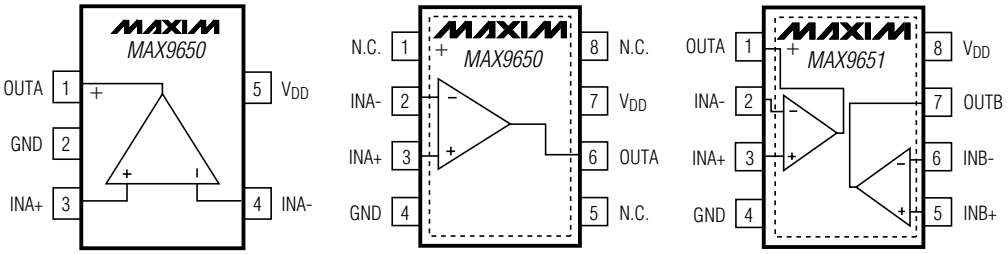


Figure 2. Typical TFT-LCD Backplane Drive Circuit

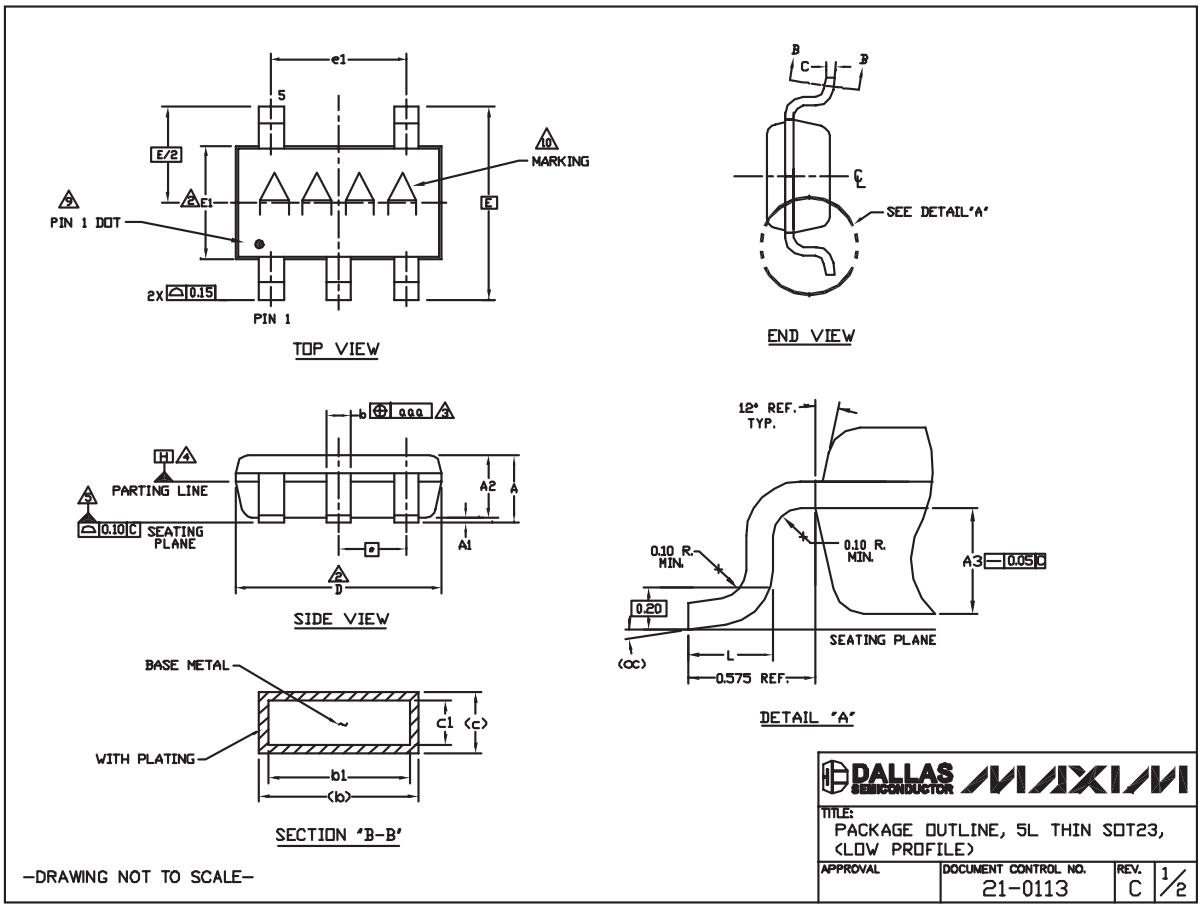
Pin Configurations



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

THIN SOT23.EPS



High-Current VCOM Drive Op Amps for TFT LCDs

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "D" AND "E1" ARE REFERENCE DATUM AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15mm ON "D" AND 0.25mm ON "E" PER SIDE.
3. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUM PLANE "H" LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT THE BOTTOM OF PARTING LINE.
5. THE LEAD TIPS MUST LINE WITHIN A SPECIFIED TOLERANCE ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL LINES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; AND THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITH 0.10mm AT SEATING PLANE.
6. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-193 EXCEPT FOR THE "e" DIMENSION WHICH IS 0.95mm INSTEAD OF 1.00mm. THIS PART IS IN FULL COMPLIANCE TO EIAJ SPECIFICATION SC-74.
7. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
8. WARPAGE SHALL NOT EXCEED 0.10mm.
9. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 PP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

SYMBOLS			
	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	0.075	0.10
A2	0.85	0.88	0.90
A3		0.50 BSC	
b	0.30	-	0.45
b1	0.25	0.35	0.40
c	0.15	-	0.20
c1	0.12	0.127	0.15
D	2.80	2.90	3.00
E		2.75 BSC	
E1	1.55	1.60	1.65
L	0.30	0.40	0.50
e1		1.90 BSC	
e		0.95 BSC	
∝	0°	4°	8°
aaa		0.20	
Pkg. codes:	Z5-1; Z5-2		

-DRAWING NOT TO SCALE-

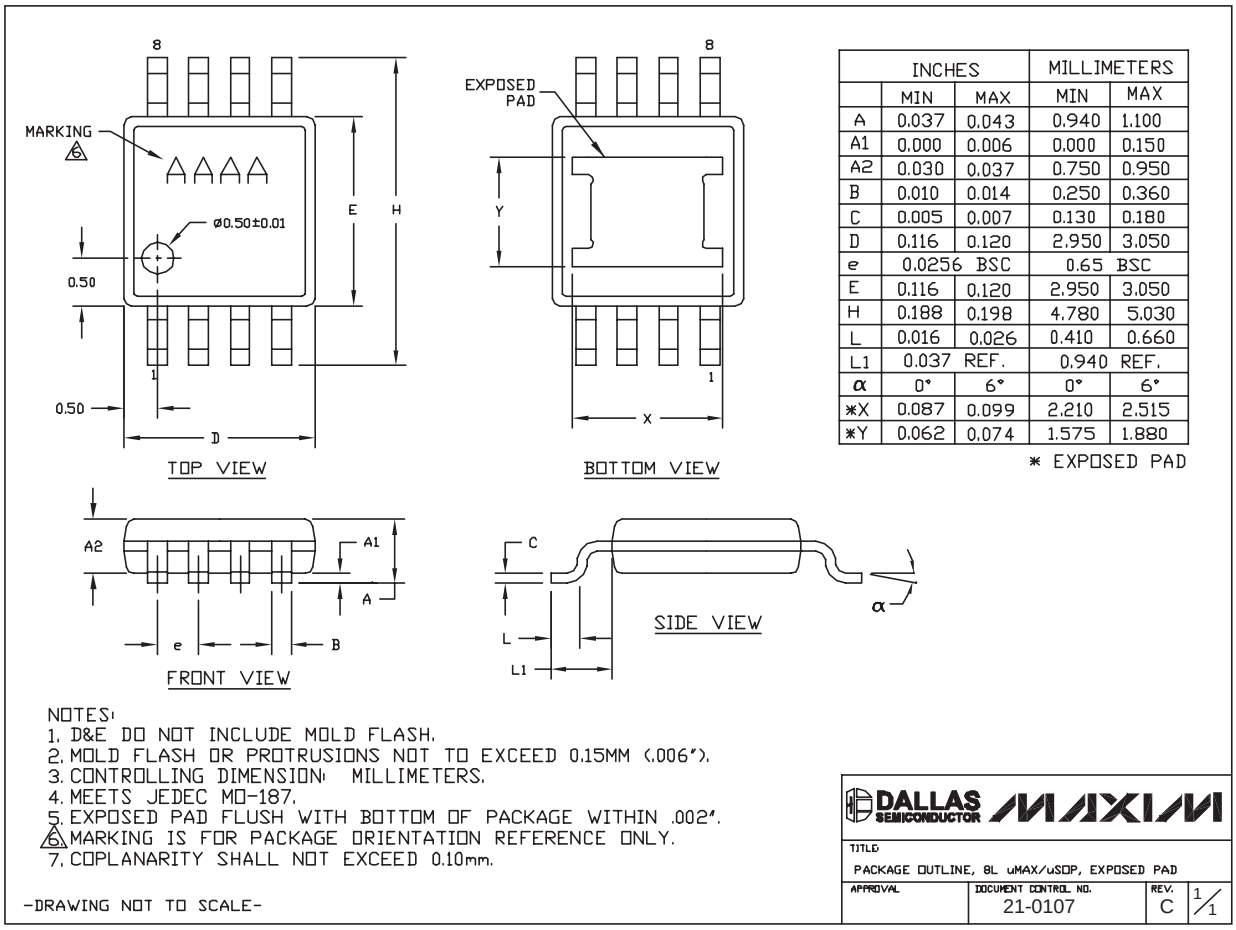
DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 5L THIN SOT23, (LOW PROFILE)

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0113	C	2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.037	0.043	0.940	1.100
A1	0.000	0.006	0.000	0.150
A2	0.030	0.037	0.750	0.950
B	0.010	0.014	0.250	0.360
C	0.005	0.007	0.130	0.180
D	0.116	0.120	2.950	3.050
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.950	3.050
H	0.188	0.198	4.780	5.030
L	0.016	0.026	0.410	0.660
L1	0.037 REF.		0.940 REF.	
α	0°	6°	0°	6°
*X	0.087	0.099	2.210	2.515
*Y	0.062	0.074	1.575	1.880

* EXPOSED PAD