



# Low-Jitter, Low-Noise LVPECL-to-LVDS Level Translator in an SC70 Package

## General Description

The MAX9156 is an LVPECL-to-LVDS level translator that accepts a single LVPECL input and translates it to a single LVDS output. It is ideal for interfacing between LVPECL and LVDS interfaces in systems that require minimum jitter, noise, power, and space.

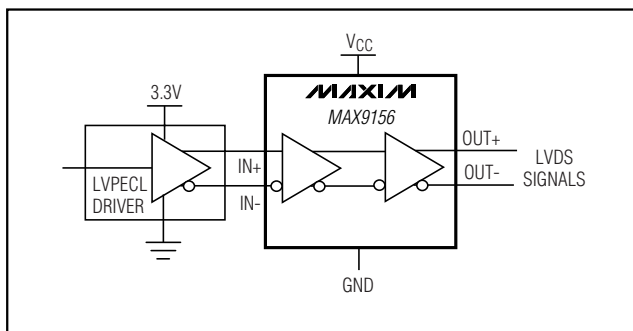
Ultra-low, 23ps<sub>p-p</sub> added deterministic jitter and 0.6ps<sub>RMS</sub> added random jitter ensure reliable communication in high-speed links that are highly sensitive to timing errors, especially those incorporating clock-and-data recovery, PLLs, serializers, or deserializers. The MAX9156's switching performance guarantees a 200Mbps data rate, but minimizes radiated noise by guaranteeing 0.5ns minimum output transition time.

The MAX9156 operates from a single +3.3V supply and consumes only 10mA supply current over a -40°C to +85°C temperature range. It is available in a tiny 6-pin SC70 package (half the size of a SOT23). Refer to the MAX9155 data sheet for a low-jitter, low-noise LVDS repeater in an SC70 package.

## Applications

Digital Cross-Connects  
Add/Drop Muxes  
Network Switches/Routers  
Cellular Phone Base Stations  
DSLAMs  
Multidrop Buses

## Typical Operating Circuit



## Features

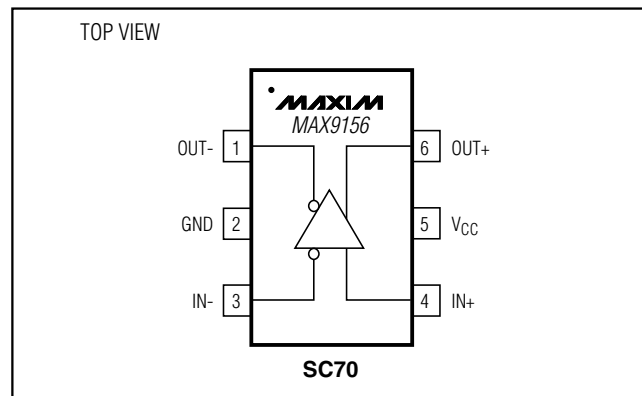
- ◆ Tiny SC70 Package
- ◆ Ultra-Low Jitter
  - 23ps<sub>p-p</sub> Added Deterministic Jitter (2<sup>23</sup>-1 PRBS)
  - 0.6ps<sub>RMS</sub> Added Random Jitter
- ◆ 0.5ns (min) Transition Time Minimizes Radiated Noise
- ◆ 200Mbps Guaranteed Data Rate
- ◆ Low 10mA Supply Current
- ◆ Output Conforms to ANSI/EIA/TIA-644 LVDS Standard
- ◆ High-Impedance Inputs and Outputs in Power-Down Mode

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## Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	TOP MARK
MAX9156EXT-T	-40°C to +85°C	6 SC70-6	ABD

## Pin Configuration



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## ABSOLUTE MAXIMUM RATINGS

V <sub>CC</sub> to GND	-0.3V to +4.0V	Storage Temperature Range	-65°C to +150°C
IN+, IN- to GND	-0.3V to +4.0V	Junction Temperature	+150°C
OUT+, OUT- to GND	-0.3V to +4.0V	Operating Temperature Range	-40°C to +85°C
Short-Circuit Duration (OUT+, OUT-)	Continuous	ESD Protection	
Continuous Power Dissipation (T <sub>A</sub> = +70°C)		Human Body Model, IN+, IN-, OUT+, OUT-	±8kV
6-Pin SC70 (derate 3.1mW/°C above +70°C)	245mW	Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +3.0V to +3.6V, R<sub>L</sub> = 100Ω ±1%, |V<sub>ID</sub>| = 0.05V to V<sub>CC</sub>, V<sub>CM</sub> = |V<sub>ID</sub> / 2| to V<sub>CC</sub> - |V<sub>ID</sub> / 2|, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values at V<sub>CC</sub> = +3.3V, T<sub>A</sub> = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>LVPECL INPUT</b>						
Differential Input High Threshold	V <sub>TH</sub>			7	50	mV
Differential Input Low Threshold	V <sub>TL</sub>		-50	-7		mV
Input Resistor	R <sub>IN</sub>	Figure 1	360	1328		kΩ
Input Current	I <sub>IN+</sub> , I <sub>IN-</sub>	IN+ = 3.6V, IN- = 0	-10	2.7	10	μA
		IN+ = 0, IN- = 3.6V	-10	2.7	10	
Power-Off Input Current	I <sub>IN+</sub> , I <sub>IN-</sub>	V <sub>CC</sub> = 0, IN+ = 3.6V, IN- = 0	-10	2.7	10	μA
		Figure 1, IN+ = 0, IN- = 3.6V	-10	2.7	10	
<b>LVDS OUTPUT</b>						
Differential Output Voltage	V <sub>OD</sub>	Figure 2	250	360	450	mV
Differential Output Voltage	ΔV <sub>OD</sub>	Figure 2		0.008	25	mV
Offset (Common-Mode) Voltage	V <sub>OS</sub>	Figure 2	1.125	1.25	1.375	V
Change in V <sub>OS</sub> for Complementary Output States	ΔV <sub>OS</sub>	Figure 2		0.005	25	mV
Output High Voltage	V <sub>OH</sub>			1.44	1.6	V
Output Low Voltage	V <sub>OL</sub>		0.9	1.08		V
Differential Output Voltage	V <sub>OD+</sub>	IN+, IN- open	+250	+360	+450	mV
Power-Off Output Leakage Current	I <sub>O</sub> OFF	V <sub>CC</sub> = 0, OUT+ = 3.6V, other output open	-10	0.02	10	μA
		OUT- = 3.6V, other output open	-10	0.02	10	
Differential Output Resistance	R <sub>O</sub> DIFF	V <sub>CC</sub> = +3.6V or 0	100	260	400	Ω
Output Short Current	I <sub>SC</sub>	V <sub>ID</sub> = +50mV, OUT+ = GND		-5	-15	mA
		V <sub>ID</sub> = -50mV, OUT- = GND		-5	-15	
<b>POWER SUPPLY</b>						
Supply Current	I <sub>CC</sub>			10	15	mA

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## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +3.0V$  to  $+3.6V$ ,  $R_L = 100\Omega \pm 1\%$ ,  $C_L = 10pF$ ,  $|V_{ID}| = 0.15V$  to  $V_{CC}$ ,  $V_{CM} = |V_{ID}|/2$  to  $V_{CC} - |V_{ID}|/2$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values at  $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$ .) (Notes 3, 4, 5) (Figures 3, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Propagation Delay High to Low	$t_{PHLD}$		1.3	2.0	2.8	ns
Differential Propagation Delay Low to High	$t_{PLHD}$		1.3	2.0	2.8	ns
Added Deterministic Jitter (Notes 6, 11)	$t_{DJ}$	200Mbps $2^{23}$ -1 PRBS data pattern		23	100	pSp-p
Added Random Jitter (Notes 7, 11)	$t_{RJ}$	$f_{IN} = 100MHz$		0.6	2.9	pSRMS
Differential Part-to-Part Skew (Note 8)	$t_{SKPP1}$			0.17	0.6	ns
Differential Part-to-Part Skew (Note 9)	$t_{SKPP2}$				1.5	ns
Switching Supply Current	$I_{CCSW}$			11.3	18	mA
Rise Time	$t_{TLH}$		0.5	0.66	1.0	ns
Fall Time	$t_{THL}$		0.5	0.64	1.0	ns
Input Frequency (Note 10)	$f_{MAX}$		100			MHz

**Note 1:** All devices are 100% tested at  $T_A = +25^\circ C$ . Limits over temperature are guaranteed by design and characterization.

**Note 2:** Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except  $V_{TH}$ ,  $V_{TL}$ ,  $V_{OD}$ , and  $\Delta V_{OD}$ .

**Note 3:** Guaranteed by design and characterization.

**Note 4:** Signal generator output (unless otherwise noted): frequency = 100MHz, 50% duty cycle,  $R_O = 50\Omega$ ,  $t_R = 1.5ns$ , and  $t_F = 1.5ns$  (0% to 100%).

**Note 5:**  $C_L$  includes scope probe and test jig capacitance.

**Note 6:** Signal generator output for  $t_{DJ}$ :  $V_{OD} = 150mV$ ,  $V_{OS} = 1.2V$ ,  $t_{DJ}$  includes pulse (duty cycle) skew.

**Note 7:** Signal generator output for  $t_{RJ}$ :  $V_{OD} = 150mV$ ,  $V_{OS} = 1.2V$ .

**Note 8:**  $t_{SKPP1}$  is the magnitude difference of any differential propagation delays between devices operating over rated conditions at the same supply voltage, input common-mode voltage, and ambient temperature.

**Note 9:**  $t_{SKPP2}$  is the magnitude difference of any differential propagation delays between devices operating over rated conditions.

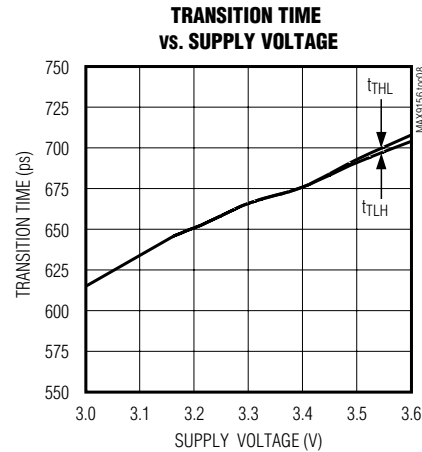
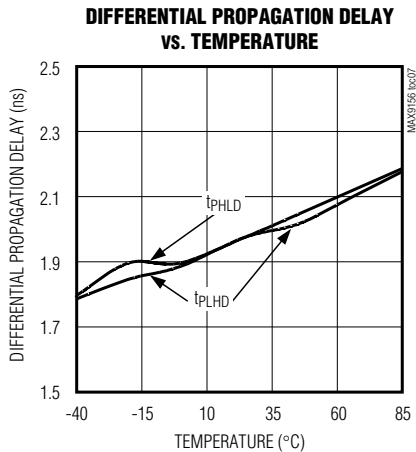
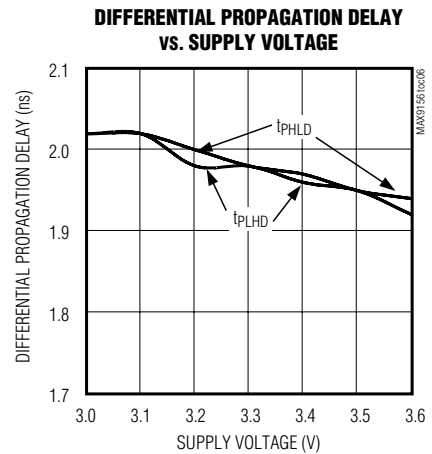
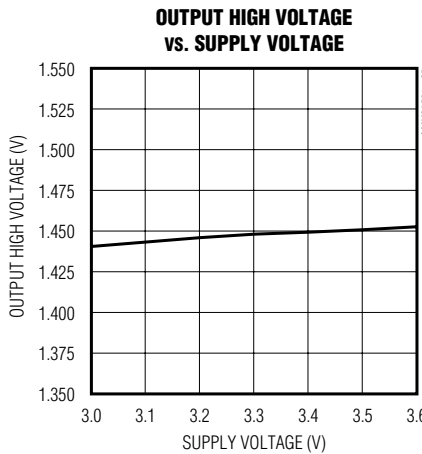
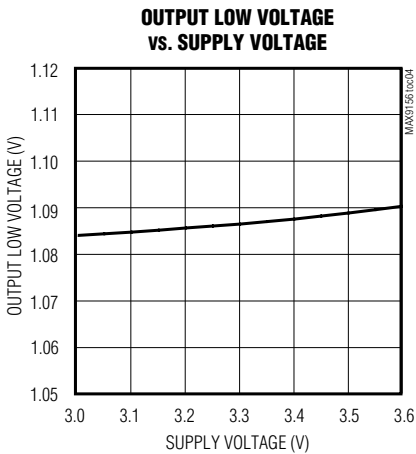
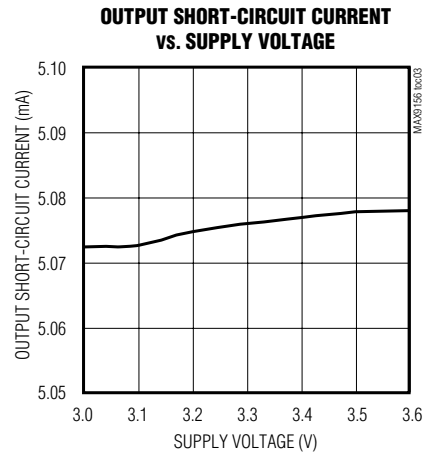
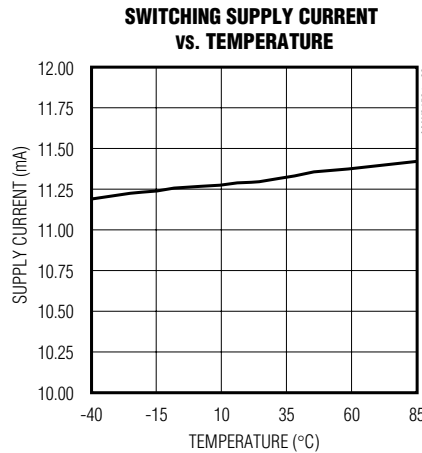
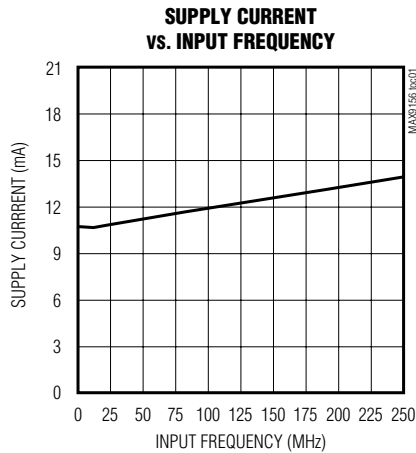
**Note 10:** Device meets  $V_{OD}$  DC specification and AC specifications while operating at  $f_{MAX}$ .

**Note 11:** Jitter added to the input signal.

# Low-Jitter, Low-Noise LVPECL-to-LVDS Level Translator in an SC70 Package

## Typical Operating Characteristics

( $V_{CC} = +3.3V$ ,  $R_L = 100\Omega \pm 1\%$ ,  $C_L = 10pF$ ,  $|V_{ID}| = 0.2V$ ,  $V_{CM} = 1.2V$ ,  $T_A = +25^\circ C$ , unless otherwise noted. Signal generator output: frequency = 100MHz, 50% duty cycle,  $R_O = 50\Omega$ ,  $t_R = 1.5ns$ , and  $t_F = 1.5ns$  (0% to 100%), unless otherwise noted.)

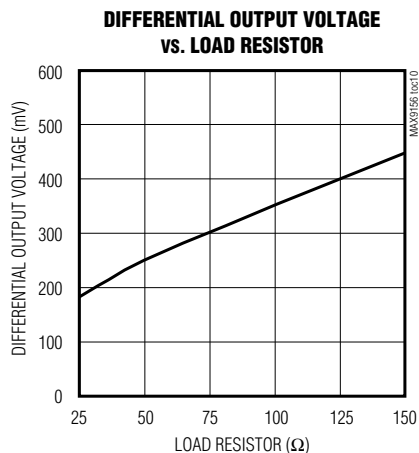
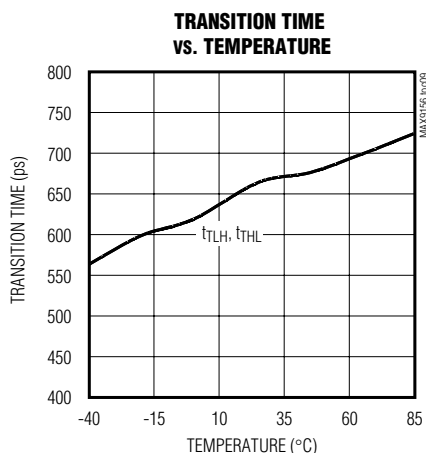


# Low-Jitter, Low-Noise LVPECL-to-LVDS Level Translator in an SC70 Package

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## Typical Operating Characteristics (continued)

( $V_{CC} = +3.3V$ ,  $R_L = 100\Omega \pm 1\%$ ,  $C_L = 10pF$ ,  $|V_{ID}| = 0.2V$ ,  $V_{CM} = 1.2V$ ,  $T_A = +25^\circ C$ , unless otherwise noted. Signal generator output: frequency = 100MHz, 50% duty cycle,  $R_O = 50\Omega$ ,  $t_R = 1.5ns$ , and  $t_F = 1.5ns$  (0% to 100%), unless otherwise noted.)



## Pin Description

PIN	NAME	FUNCTION
1	OUT-	Inverting LVDS Output
2	GND	Ground
3	IN-	Inverting LVPECL-Compatible Input
4	IN+	Noninverting LVPECL-Compatible Input
5	V <sub>CC</sub>	Power Supply. Bypass V <sub>CC</sub> to GND with a 0.01μF ceramic capacitor.
6	OUT+	Noninverting LVDS Output

Table 1. Function Table (Figure 2)

INPUT, V <sub>ID</sub>	OUTPUT, V <sub>OD</sub>
≥ 50mV	High
≤ -50mV	Low
50mV > V <sub>ID</sub> > -50mV	Indeterminate
Open	High

**Note:**  $V_{ID} = (IN+ - IN-)$ ,  $V_{OD} = (OUT+ - OUT-)$   
 High =  $450mV \geq V_{OD} \geq 250mV$   
 Low =  $-250mV \geq V_{OD} \geq -450mV$

## Detailed Description

The LVDS interface standard is a signaling method intended for point-to-point communication over a controlled-impedance medium, as defined by the ANSI/TIA/EIA-644 and IEEE 1596.3 standards. The LVDS standard uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise.

The MAX9156 is a 200Mbps LVDS translator intended for high-speed, point-to-point, low-power applications. The MAX9156 accepts differential LVPECL inputs and produces an LVDS output. The input voltage range includes signals from GND up to V<sub>CC</sub>, allowing interoperability with 3.3V LVPECL devices.

The MAX9156 provides a high output when the inputs are open. See Table 1.

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## Applications Information

### Supply Bypassing

Bypass  $V_{CC}$  with a high-frequency surface-mount ceramic  $0.01\mu\text{F}$  capacitor as close to the device as possible.

### Differential Traces

Input and output trace characteristics affect the performance of the MAX9156. Use controlled-impedance differential traces. Ensure that noise couples as common mode by running the traces within a differential pair close together.

Maintain the distance within a differential pair to avoid discontinuities in differential impedance. Avoid  $90^\circ$  turns and minimize the number of vias to further prevent impedance discontinuities.

### Cables and Connectors

The LVDS standards define signal levels for interconnect with a differential characteristic impedance and termination of  $100\Omega$ . Interconnects with a characteristic impedance and termination of  $90\Omega$  to  $132\Omega$  impedance are allowed, but produce different signal levels (see *Termination*).

LVPECL signals are typically specified for  $50\Omega$  single-ended characteristic impedance interconnect terminated through  $50\Omega$  to  $V_{CC} - 2\text{V}$ .

Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

### Termination

For point-to-point LVDS links, the termination resistor should be located at the LVDS receiver input and

match the differential characteristic impedance of the transmission line.

Each line of a differential LVPECL link should be terminated through  $50\Omega$  to  $V_{CC} - 2\text{V}$  or be replaced by the Thevinin equivalent.

The LVDS output voltage level depends upon the differential characteristic impedance of the interconnect and the value of the termination resistance. The MAX9156 is guaranteed to produce LVDS output levels into  $100\Omega$ . With the typical  $3.6\text{mA}$  output current, the MAX9156 produces an output voltage of  $360\text{mV}$  when driving a  $100\Omega$  transmission line terminated with a  $100\Omega$  termination resistor ( $3.6\text{mA} \times 100\Omega = 360\text{mV}$ ). For typical output levels with different loads, see the Differential Output Voltage vs. Load Resistor typical operating curve.

## Chip Information

TRANSISTOR COUNT: 401

PROCESS: CMOS

# Low-Jitter, Low-Noise LVPECL-to-LVDS Level Translator in an SC70 Package

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## Test Circuits and Timing Diagrams

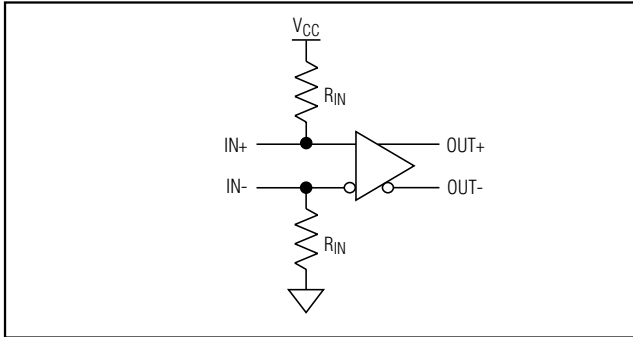


Figure 1. LVPECL Input Bias

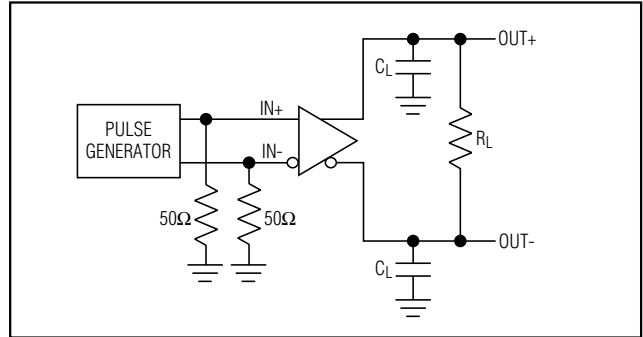


Figure 3. Transition Time and Propagation Delay Test Circuit

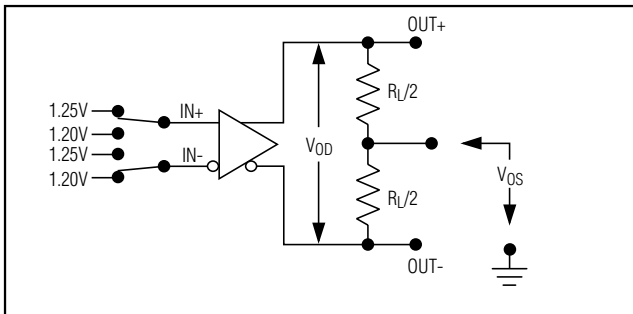


Figure 2. DC Load Test Circuit

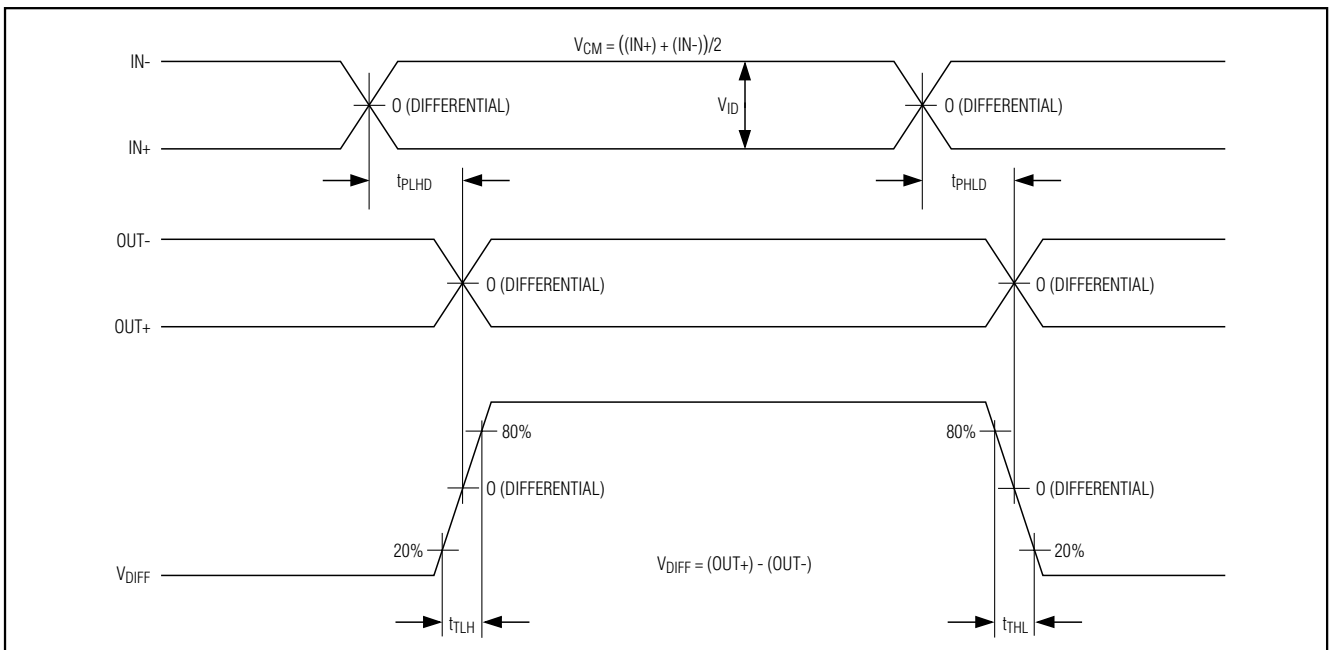


Figure 4. Transition Time and Propagation Delay Timing Diagram

# Low-Jitter, Low-Noise LVPECL-to-LVDS Level Translator in an SC70 Package

## Package Information

SYMBOL	MIN	MAX
e	0.65	BSC
D	1.80	2.20
b	0.15	0.30
E	1.15	1.35
HE	1.80	2.40
Q1	0.10	0.40
A2	0.80	1.00
A1	0.00	0.10
A	0.80	1.10
c	0.10	0.18
L	0.10	0.30
L1	0.425	TYP.

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS ARE INCLUSIVE OF PLATING
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR
4. ALL SPECIFICATIONS COMPLY TO EIAJ SC70
5. COPLANARITY 4 MILS. MAX.
6. PIN 1 I.D. DOT

<b>MAXIM</b>		
PROPRIETARY INFORMATION		
TITLE: PACKAGE OUTLINE, SC70, 6L		
APPROVAL	DOCUMENT CONTROL NO. 21-0077	REV B
		1/1

SC70, 6LEPS

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