19-0242; Rev 0; 6/05

MAXIM

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

General Description

The MAX9975 dual, low-power, high-speed, pin electronics driver/comparator with 35mA load IC includes, for each channel, a three-level pin driver, a dual comparator, variable clamps, and an active load. An additional differential comparator allows comparisons between the two channels. The driver features a wide voltage range and high-speed operation, includes high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low voltage swings. The dual comparator provides low dispersion (timing variation) over a wide variety of input conditions, and differential outputs. The clamps provide damping of high-speed device-under-test (DUT) waveforms when the device is configured as a high-impedance receiver. The programmable load supplies up to 35mA of source and sink current. The load facilitates contact/continuity testing, at-speed parametric testing of I_{OH} and I_{OL}, and pullup of high-output-impedance devices.

The MAX9975 provides high-speed, differential control inputs and open-collector outputs with internal 50Ω termination resistors that make it CML compatible. These features significantly reduce the discrete component count on the circuit board.

A 3-wire, low-voltage, CMOS-compatible serial interface programs the low-leakage and tri-state/terminate operational configurations of the MAX9975.

The MAX9975ARCCQ operating range is -1.5V to +6.5V. The MAX9975AZCCQ operating range is -1.0V to +7.0V. The MAX9975 features power dissipation of only 1.6W per channel. The device is available in a 100-pin, 14mm x 14mm x 0.1mm body, and 0.5mm pitch TQFP. An exposed 8mm x 8mm die pad on the top of the package facilitates efficient heat removal. The device is specified to operate with an internal die temperature of +60°C to +100°C, and features a die temperature monitor output.

Applications

Medium-Performance Commodity Memory ATE

Features

- **Low 1.6W/Channel (typ) Power Dissipation**
- **Greatly Reduced Power Penalty when Load Commutated**
- **High Speed: 1200Mbps at $3V_{P-P}$ and 1800Mbps at $1V_{P-P}$**
- **Programmable 35mA Active-Load Current**
- **Low Timing Dispersion**
- **Wide -1.5V to +6.5V (MAX9975AR) or -1.0V to +7.0V (MAX9975AZ) Operating Range**
- **Active Termination (3rd-Level Drive)**
- **Integrated Clamps**
- **Integrated Differential Comparator**
- **Interfaces Easily with Most Logic Families**
- **Internal 50Ω Termination Resistors**
- **Low Gain and Offset Errors**
- **Comparator Hysteresis Control from 0V to 15mV**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9975ARCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9975ARCCQ+	0°C to +70°C	100 TQFP-EPR**
MAX9975AZCCQ*	0°C to +70°C	100 TQFP-EPR**
MAX9975AZCCQ+*	0°C to +70°C	100 TQFP-EPR**

*Future product—contact factory for availability.
**EPR = Exposed pad reversed (TOP).
+Denotes lead-free package.

Pin Configuration and Selector Guide appear at end of data sheet.

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

ABSOLUTE MAXIMUM RATINGS

MAX9975AR
- V_{CC} to GND .....-0.3V to +11V
- V_{EE} to GND .....-5.75V to +0.3V
- DUT_ to GND .....-2.75V to +7.5V
- DHV_, DLV_, DTV_, CHV_, CLV_, COM_ to GND.....-2.5V to +7.5V
- CPHV_ to GND .....-1.0V to +8.5V
- CPLV_ to GND.....-3.5V to +6.0V
- DUT_ Short Circuit to -1.5V to +6.5V.....Continuous

MAX9975AZ
- V_{CC} to GND.....-0.3V to +11.5V
- V_{EE} to GND.....-5.25V to +0.3V
- DUT_ to GND.....-2.25V to +8.0V
- DHV_, DLV_, DTV_, CHV_, CLV_, COM_ to GND.....-2.0V to +8.0V
- CPHV_ to GND .....-0.5V to +9.0V
- CPLV_ to GND.....-3.0V to +6.5V
- DUT_ Short Circuit to -1.0V to +7.0V.....Continuous

V_{CC} - V_{EE}.....-0.3V to +16.75V
GS to GND.....±1V
LDH_, LDL_ to GND .....-0.3V to +6V
DATA_, NDATA_, RCV_, NRCV_ to GND .....-2.5V to +5V
LDEN_, NLDEN_ to GND.....-2.5V to +5V
DATA_ to NDATA_, RCV_ to NRCV_, LDEN_ to NLDEN_.....±1.5V
TDATA_, TLDEN_ to GND .....-2.5V to +5V
DATA_, NDATA_ to TDATA_.....±2V
LDEN_, NLDEN_ to TLDEN_.....±2V
$V_{CCO\_}$ to GND.....-0.3V to +5V
SCLK, DIN, $\overline{CS}$, $\overline{RST}$ to GND .....-1V to +5V
DHV_ to DLV_.....±10V
DHV_ to DTV_.....±10V
DLV_ to DTV_.....±10V
CHV_ or CLV_ to DUT_.....±10V
CH_, NCH_, CL_, NCL_ to GND.....-1V to +5V
HYS_ Current .....-1mA to +1mA
All Other Pins to GND .....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
TEMP Current.....-0.5mA to +20mA
Power Dissipation (T_A = +70°C)
- 100-Pin TQFP-EPR (derate 167mW/°C above +70°C) 13.3W*

Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature, Lead-Free (soldering, 10s).....+260°C
Lead Temperature, Leaded (soldering, 10s).....+300°C

**Dissipation wattage values are based on still air with no heat sink. Actual maximum power dissipation is a function of heat-extraction techniques and may be substantially higher.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Positive Supply	V_{CC}	MAX9975AR	9.5	9.75	10.5	V
		MAX9975AZ	10.0	10.25	11.0	
Negative Supply	V_{EE}	MAX9975AR	-5.25	-4.75	-4.50	V
		MAX9975AZ	-4.75	-4.25	-4.00	
Positive Supply Current (Note 2)	I_{CC}	$V_{LDH\_}$ = $V_{LDL\_}$ = 0V, R_L ≥ 10MΩ		170	190	mA
		$V_{LDH\_}$ = $V_{LDL\_}$ = 3.5V, R_L = 0, $V_{COM\_}$ = 1.5V, load enabled, driver = high impedance		250	280	
Negative Supply Current (Note 2)	I_{EE}	$V_{LDH\_}$ = $V_{LDL\_}$ = 0V, R_L ≥ 10MΩ		-290	-320	mA
		$V_{LDH\_}$ = $V_{LDL\_}$ = 3.5V, R_L = 0, $V_{COM\_}$ = -1V, load enabled, driver = high impedance		-370	-410	
Power Dissipation (Notes 2, 3)	P_D	$V_{LDH\_}$ = $V_{LDL\_}$ = 0V		3.2	3.6	W
		$V_{LDH\_}$ = $V_{LDL\_}$ = 3.5V, R_L = 0, $V_{COM\_}$ = 1.5V, load enabled, driver = high impedance		3.7	4.1	

ELECTRICAL CHARACTERISTICS (continued)

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DUT_ CHARACTERISTICS							
Operating Voltage Range (Note 4)	V_{DUT}	MAX9975AR		-1.5		+6.5	V
		MAX9975AZ		-1.0		+7.0	
Leakage Current in High-Impedance Mode	I_{DUT}	MAX9975AR	LLEAK = 0, $V_{DUT\_}$ = -1.5V, 0V, +3V, +6.5V			±3	µA
		MAX9975AZ	LLEAK = 0, $V_{DUT\_}$ = -1V, 0V, +3V, +7V			±3	
Leakage Current in Low-Leakage Mode		MAX9975AR	LLEAK = 1, $V_{DUT\_}$ = -1.5V, 0V, +3V, +6.5V			±15	nA
		MAX9975AZ	LLEAK = 1, $V_{DUT\_}$ = -1V, 0V, +3V, +7V			±15	
Combined Capacitance	C_{DUT}	Driver in term mode (DUT_ = DTV_)			3	5	pF
		Driver in high-impedance mode			5	6	
Low-Leakage Enable Time		(Notes 5, 6)			20		µs
Low-Leakage Disable Time		(Notes 6, 7)			0.1		µs
CONTROL AND LEVELS INPUTS							
LEVEL PROGRAMMING INPUTS (DHV_, DLV_, DTV_, CHV_, CLV_, CPHV_, CPLV_, COM_, LDH_, LDL_)							
Input Bias Current	I_{BIAS}					±25	µA
Settling Time		To 0.1% of full-scale change			1		µs
DIFFERENTIAL CONTROL INPUTS (DATA_, NDATA_, RCV_, NRCV_, LDEN_, NLDEN_)							
Input High Voltage	V_{IH}			0		3.5	V
Input Low Voltage	V_{IL}			-0.2		+3.2	V
Differential Input Voltage	V_{DIFF}	Between differential inputs		±0.15		±1.00	V
		Between a differential input and its termination voltage				±1.9	
Input Bias Current						±25	µA
Input Termination Voltage	$V_{TDATA\_}$ $V_{TLDEN\_}$			0		+3.5	V
Input Termination Resistor		Between signal and corresponding termination voltage input		47.5		52.5	Ω
SINGLE-ENDED CONTROL INPUTS ($\overline{CS}$, SCLK, DIN, $\overline{RST}$)							
Internal Threshold Reference	V_{THRINT}			1.05	1.25	1.45	V
Internal Reference Output Resistance	R_O				20		kΩ
External Threshold Reference	V_{THR}			0.43		1.73	V
Input High Voltage	V_{IH}			V_{THR} + 0.2		3.5	V
Input Low Voltage	V_{IL}			-0.1		V_{THR} - 0.2	V
Input Bias Current	I_B					±25	µA

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

ELECTRICAL CHARACTERISTICS (continued)

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SERIAL INTERFACE TIMING (Figure 6)							
SCLK Frequency	f_{SCLK}					50	MHz
SCLK Pulse-Width High	t_{CH}			8			ns
SCLK Pulse-Width Low	t_{CL}			8			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}			3.5			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}			3.5			ns
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}			3.5			ns
DIN to SCLK High Setup	t_{DS}			3.5			ns
DIN to SCLK High Hold	t_{DH}			3.5			ns
$\overline{CS}$ Pulse-Width High	t_{CSWH}			20			ns
TEMPERATURE MONITOR (TEMP)							
Nominal Voltage		T_J = +70°C, R_L ≥ 10MΩ			3.33		V
Temperature Coefficient					+10		mV/°C
Output Resistance					20		kΩ
DRIVERS (Note 8)							
DC OUTPUT CHARACTERISTICS (R_L ≥ 10MΩ)							
DHV_, DLV_, DTV_, Output Offset Voltage	V_{OS}	At DUT_ with $V_{DHV\_}$, $V_{DTV\_}$, $V_{DLV\_}$ independently tested at +1.5V				±15	mV
Output Offset Voltage Due to Ground Sense	V_{GSOS}	MAX9975AR	V_{GS} = +100mV, $V_{DHV\_}$ = 6.5V + 100mV		±2		mV
			V_{GS} = -100mV, $V_{DLV\_}$ = -1.5V - 100mV		±2		
		MAX9975AZ	V_{GS} = +100mV, $V_{DHV\_}$ = 7V + 100mV		±2		
			V_{GS} = -100mV, $V_{DLV\_}$ = -1V - 100mV		±2		
DHV_, DLV_, DTV_ Output-Offset Temperature Coefficient					+200		µV/°C
DHV_, DLV_, DTV_ Gain	A_V	Measured with $V_{DHV\_}$, $V_{DLV\_}$, and $V_{DTV\_}$ at 0V and 4.5V		0.997	1.00	1.003	V/V
DHV_, DLV_, DTV_ Gain Temperature Coefficient					-50		ppm/°C
Linearity Error		$V_{DUT\_}$ = 1.5V, 3V (Note 9)				±5	mV
		Full range (Notes 9, 10)				±15	
DHV_ to DLV_ Crosstalk		MAX9975AR	$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 200mV, 6.5V			±2	mV
		MAX9975AZ	$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 200mV, 7V			±2	

ELECTRICAL CHARACTERISTICS (continued)

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DLV_ to DHV_ Crosstalk		MAX9975AR	$V_{DHV\_}$ = 5V, $V_{DLV\_}$ = -1.5V, +4.8V			±2	mV
		MAX9975AZ	$V_{DHV\_}$ = 5V, $V_{DLV\_}$ = -1V, +4.8V			±2	
DTV_ to DLV_ and DHV_ Crosstalk		MAX9975AR	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = -1.5V, +6.5V			±2	mV
		MAX9975AZ	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = -1V, +7V			±2	
DHV_ to DTV_ Crosstalk		$V_{DTV\_}$ = 1.5V, $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 1.6V, 3V				±2	mV
DLV_ to DTV_ Crosstalk		$V_{DTV\_}$ = 1.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, 1.4V				±2	mV
DHV_, DTV_, DLV_ DC Power-Supply Rejection Ratio	PSRR	(Note 11)				±18	mV/V
Maximum DC Drive Current	$I_{DUT\_}$			±40		±80	mA
DC Output Resistance	$R_{DUT\_}$	$I_{DUT\_}$ = ±30mA (Note 12)		47	48	49	Ω
DC Output Resistance Variation	$\Delta R_{DUT\_}$	$I_{DUT\_}$ = ±1mA, ±8mA			0.5	1	Ω
		$I_{DUT\_}$ = ±1mA, ±8mA, ±15mA, ±40mA			0.75	1.5	
DYNAMIC OUTPUT CHARACTERISTICS (Z_L = 50Ω)							
AC Drive Current				±80			mA
Drive-Mode Overshoot		$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 0.1V			15	22	mV
		$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 1V			110	130	
		$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 3V			210	370	
Drive-Mode Undershoot		$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 0.1V			4	11	mV
		$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 1V			20	65	
		$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 3V			30	185	
Term-Mode Overshoot (Note 13)		$V_{DUT\_}$ = 1.0V_{P-P}, t_R = t_F = 250ps, 10% to 90%			60	150	mV
		$V_{DUT\_}$ = 3.0V_{P-P}, t_R = t_F = 500ps, 10% to 90%			0		
Term-Mode Spike		$V_{DHV\_}$ = $V_{DTV\_}$ = 1V, $V_{DLV\_}$ = 0V			180	250	mV
		$V_{DLV\_}$ = $V_{DTV\_}$ = 0V, $V_{DHV\_}$ = 1V			180	250	
High-Impedance-Mode Spike		$V_{DLV\_}$ = -1.0V, $V_{DHV\_}$ = 0V			100		mV
		$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = 1V			100		
Settling Time to within 25mV		3V step (Note 14)			4		ns
Settling Time to within 5mV		3V step (Note 14)			40		ns

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

ELECTRICAL CHARACTERISTICS (continued)

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Z_L = 50Ω) (Note 15)							
Prop Delay, Data to Output	t_{PDD}			1.2	1.5	1.9	ns
Prop-Delay Match, t_{LH} vs. t_{HL}		3V_{P-P}			±40	±100	ps
Prop-Delay Match, Drivers within Package		(Note 16)			40		ps
Prop-Delay Temperature Coefficient					+1.6		ps/°C
Prop-Delay Change vs. Pulse Width		0.2V_{P-P}, 40MHz, 0.6ns to 24.4ns pulse width, relative to 12.5ns pulse width			±25	±50	ps
		1V_{P-P}, 40MHz, 0.6ns to 24.4ns pulse width, relative to 12.5ns pulse width			±25	±50	
		3V_{P-P}, 40MHz, 0.9ns to 24.1ns pulse width, relative to 12.5ns pulse width			±35	±60	
		5V_{P-P}, Z_L = 500Ω, 40MHz, 1.4ns to 23.6ns pulse width, relative to 12.5ns pulse width			±100		
Prop-Delay Change vs. Common-Mode Voltage		MAX9975AR	$V_{DHV\_}$ - $V_{DLV\_}$ = 1V, $V_{DHV\_}$ = 0 to 6V		50	75	ps
		MAX9975AZ	$V_{DHV\_}$ - $V_{DLV\_}$ = 1V, $V_{DHV\_}$ = 0.5V to 6.5V		50	75	
Prop Delay, Drive to High Impedance	t_{PDDZ}	$V_{DHV\_}$ = 1.0V, $V_{DLV\_}$ = -1.0V, $V_{DTV\_}$ = 0V		1.6	2.1	2.6	ns
Prop Delay, High Impedance to Drive	t_{PDZD}	$V_{DHV\_}$ = 1.0V, $V_{DLV\_}$ = -1.0V, $V_{DTV\_}$ = 0V		2.6	3.2	3.9	ns
Prop-Delay Match, t_{PDDZ} vs. t_{PDZD}				-1.5	-1.1	-0.7	ns
Prop-Delay Match, t_{PDDZ} vs. t_{LH}				0.2	0.6	1.0	ns
Prop Delay, Drive to Term	t_{PDDT}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V		1.3	1.8	2.3	ns
Prop Delay, Term to Drive	t_{PDTD}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V		1.6	2.1	2.7	ns
Prop-Delay Match, t_{PDDT} vs. t_{PDTD}				-0.7	-0.3	+0.1	ns
Prop-Delay Match, t_{PDDT} vs. t_{LH}				-0.1	+0.3	+0.7	ns
DYNAMIC PERFORMANCE (Z_L = 50Ω)							
Rise and Fall Time	t_R, t_F	0.2V_{P-P}, 10% to 90%		300	350	400	ps
		1V_{P-P}, 10% to 90%		330	390	450	
		2V_{P-P}		430	500	570	
		3V_{P-P}, 10% to 90%		500	650	750	
		5V_{P-P}, Z_L = 500Ω, 10% to 90%		800	1000	1200	
Rise and Fall Time Match	t_R vs. t_F	3V_{P-P}, 10% to 90%			±50		ps

ELECTRICAL CHARACTERISTICS (continued)

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Pulse Width (Note 17)		$0.2V_{P-P}$			550		ps
		$1V_{P-P}$			550	630	
		$2V_{P-P}$			650	750	
		$3V_{P-P}$			850	1000	
		$5V_{P-P}$, Z_L = 500Ω			1300		
Data Rate (Note 18)		$0.2V_{P-P}$			1800		Mbps
		$1V_{P-P}$			1800		
		$2V_{P-P}$			1500		
		$3V_{P-P}$			1200		
		$5V_{P-P}$, Z_L = 500Ω			800		
Dynamic Crosstalk		(Note 19)			12		mV_{P-P}
Rise and Fall Time, Drive to Term	t_{DTR}, t_{DTF}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, 10% to 90%, Figure 1a (Note 20)		0.6	1.0	1.3	ns
Rise and Fall Time, Term to Drive	t_{TDR}, t_{TDF}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{DTV\_}$ = 1.5V, 10% to 90%, Figure 1b (Note 20)		0.6	1.0	1.3	ns
COMPARATORS (Note 8)							
COMPARATOR DC CHARACTERISTICS							
Input Voltage Range (Note 4)	V_{IN}	MAX9975AR		-1.5		+6.5	V
		MAX9975AZ		-1.0		+7.0	
Differential Input Voltage	V_{DIFF}			±8			V
Input Offset Voltage	V_{OS}	$V_{DUT\_}$ = 1.5V				±20	mV
Input Offset-Voltage Temperature Coefficient					±10		µV/°C
Common-Mode Rejection Ratio (Note 21)	CMRR	MAX9975AR	$V_{DUT\_}$ = -1.5V, +6.5V		±0.25	±2	mV/V
		MAX9975AZ	$V_{DUT\_}$ = -1V, +7V		±0.25	±2	
Linearity Error (Note 9)		MAX9975AR	$V_{DUT\_}$ = 1.5V, 3V			±3	mV
			$V_{DUT\_}$ = -1.5V, +6.5V			±10	
		MAX9975AZ	$V_{DUT\_}$ = 1.5V, 3V			±3	
			$V_{DUT\_}$ = -1V, +7V			±10	
Power-Supply Rejection Ratio (Note 11)	PSRR	$V_{DUT\_}$ = 1.5V			±0.035	±2	mV/V
COMPARATOR HYSTERESIS							
Input Hysteresis		R_{HYS} = open			0		mV
		R_{HYS} = 5kΩ			2		
		R_{HYS} = 3.8kΩ			5		
		R_{HYS} = 2.9kΩ			10		
		R_{HYS} = 2.3kΩ			15		

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

ELECTRICAL CHARACTERISTICS (continued)

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
COMPARATOR AC CHARACTERISTICS (Note 22)							
Bandwidth		Term mode, t_R = t_F = 150ps		1.5	2.5		GHz
		High-impedance mode		0.5	0.7		
Minimum Pulse Width (Note 23)	$t_{PW(MIN)}$				500	650	ps
Prop Delay	t_{PDL}			0.9	1.3	1.7	ns
Prop-Delay Temperature Coefficient					+1.7		ps/°C
Prop-Delay Match, High/Low vs. Low/High					±10	±50	ps
Prop-Delay Match High vs. Low Comparator					±50		ps
Prop-Delay Match, Comparators within Package		(Note 16)			±80		ps
Prop-Delay Dispersion vs. Common-Mode Input (Note 24)		MAX9975AR	$V_{CHV\_}$ = $V_{CLV\_}$ = -1.4V to +6.4V		40	60	ps
		MAX9975AZ	$V_{CHV\_}$ = $V_{CLV\_}$ = -0.9V to +6.9V		40	60	
Prop-Delay Dispersion vs. Overdrive		$V_{CHV\_}$ = $V_{CLV\_}$ = 0.1V to 0.9V, $V_{DUT\_}$ = 1V_{P-P}, t_R = t_F = 250ps, 10% to 90% relative to timing at 50% point			±40	±70	ps
		$V_{CHV\_}$ = $V_{CLV\_}$ = 40mV to 160mV, $V_{DUT\_}$ = 0.2V_{P-P}, t_R = t_F = 150ps, 10% to 90% relative to timing at 50% point			±40	±60	
Prop-Delay Dispersion vs. Pulse Width		0.6ns to 24.4ns pulse width, relative to 12.5ns pulse width			±30	±50	ps
Prop-Delay Dispersion vs. Slew Rate		0.5V/ns to 6V/ns slew rate, relative to 4V/ns slew rate			±30	±60	ps
Waveform Tracking 10% to 90%		$V_{DUT\_}$ = 1.0V_{P-P}, t_R = t_F = 250ps, term mode, 10% to 90% relative to timing at 50% point			±40	±70	ps
		$V_{DUT\_}$ = 1.0V_{P-P}, t_R = t_F = 250ps, high-impedance mode, 10% to 90% relative to timing at 50% point			±250	±350	
		$V_{DUT\_}$ = 3V_{P-P}, t_R = t_F = 500ps, high-impedance mode, 10% to 90% relative to timing at 50% point			±150	±200	
DUT_ Slew-Rate Tracking		Term mode			6		V/ns
		High-impedance mode			5		

ELECTRICAL CHARACTERISTICS (continued)

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
COMPARATOR LOGIC OUTPUTS (CH_, NCH_, CL_, NCL_)							
$V_{CCO\_}$ Voltage Range	$V_{VCCO\_}$			1.5		3.5	V
$V_{CCO\_}$ Current	$I_{VCCO\_}$				64		mA
Output Low Voltage Compliance		Set by I_{OL}, R_{TERM}, and $V_{CCO\_}$			-0.5		V
Output High Voltage	V_{OH}	$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0		$V_{CCO\_}$ - 0.1	$V_{CCO\_}$ - 0.01	$V_{CCO\_}$ + 0.02	V
Output Low Voltage	V_{OL}	$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0			$V_{CCO\_}$ - 0.8		V
Output Voltage Swing		$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0		760	800	840	mV
Internal Output Termination Resistor	R_{TERM}	Single-ended measurement from $V_{CCO\_}$ to CH_, NCH_, CL_, NCL_		48		52	Ω
Differential Rise and Fall Times	t_R, t_F	20% to 80%			210	250	ps
CLAMPS							
High-Clamp Input Voltage Range	$V_{CPH\_}$	MAX9975AR		0		7.5	V
		MAX9975AZ		0.5		8.0	
Low-Clamp Input Voltage Range	$V_{CPL\_}$	MAX9975AR		-2.5		+5.0	V
		MAX9975AZ		-2.0		+5.5	
Clamp Offset Voltage	V_{OS}	MAX9975AR	At DUT_ with $I_{DUT\_}$ = 1mA, $V_{CPHV\_}$ = 0V			±100	mV
			At DUT_ with $I_{DUT\_}$ = -1mA, $V_{CPLV\_}$ = 0V			±100	
		MAX9975AZ	At DUT_ with $I_{DUT\_}$ = 1mA, $V_{CPHV\_}$ = 0.5V			±100	
			At DUT_ with $I_{DUT\_}$ = -1mA, $V_{CPLV\_}$ = 0V			±100	
Offset-Voltage Temperature Coefficient					±250		µV/°C
Clamp Power-Supply Rejection Ratio (Note 11)	PSRR	MAX9975AR	$I_{DUT\_}$ = 1mA, $V_{CPHV\_}$ = 0V		±10		mV/V
			$I_{DUT\_}$ = -1mA, $V_{CPLV\_}$ = 0V		±10		
		MAX9975AZ	$I_{DUT\_}$ = 1mA, $V_{CPHV\_}$ = 0.5V		±10		
			$I_{DUT\_}$ = -1mA, $V_{CPLV\_}$ = 0V		±10		
Voltage Gain	A_V			0.96		1.005	V/V
Voltage-Gain Temperature Coefficient					-30		ppm/°C

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

ELECTRICAL CHARACTERISTICS (continued)

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Clamp Linearity		MAX9975AR	$I_{DUT\_}$ = 1mA, $V_{CPLV\_}$ = -1.5V, $V_{CPHV\_}$ = 0 to 6.5V		±10		mV
			$I_{DUT\_}$ = -1mA, $V_{CPHV\_}$ = 6.5V, $V_{CPLV\_}$ = -1.5V to +5.0V		±10		
		MAX9975AZ	$I_{DUT\_}$ = 1mA, $V_{CPLV\_}$ = -1.0V, $V_{CPHV\_}$ = 0.5V to 7.0V		±10		
			$I_{DUT\_}$ = -1mA, $V_{CPHV\_}$ = 7.0V, $V_{CPLV\_}$ = -1.0V to +5.5V		±10		
Short-Circuit Output Current	$I_{SCDUT\_}$	MAX9975AR	$V_{CPHV\_}$ = 0V, $V_{CPLV\_}$ = -1.5V, $V_{DUT\_}$ = 6.5V	40	80		mA
			$V_{CPHV\_}$ = 6.5V, $V_{CPLV\_}$ = 5.0V, $V_{DUT\_}$ = -1.5V	-80	-40		
		MAX9975AZ	$V_{CPHV\_}$ = 0.5V, $V_{CPLV\_}$ = -1.0V, $V_{DUT\_}$ = 7.0V	40	80		
			$V_{CPHV\_}$ = 7.0V, $V_{CPLV\_}$ = 5.5V, $V_{DUT\_}$ = -1.0V	-80	-40		
Clamp DC Impedance	R_{OUT}	$V_{CPHV\_}$ = 3V, $V_{CPLV\_}$ = 0V, $I_{DUT\_}$ = ±5mA and ±15mA		48		53	Ω
Clamp DC Impedance Variation		MAX9975AR	$V_{CPHV\_}$ = 2.5V, $V_{CPLV\_}$ = -1.5V $I_{DUT\_}$ = 10mA, 20mA, 30mA		1.5		Ω
			$V_{CPHV\_}$ = 6.5V $V_{CPLV\_}$ = 2.5V, $I_{DUT\_}$ = -10mA, -20mA, -30mA		1.5		
		MAX9975AZ	$V_{CPHV\_}$ = 2.5V, $V_{CPLV\_}$ = -1.0V $I_{DUT\_}$ = 10mA, 20mA, 30mA		1.5		
			$V_{CPHV\_}$ = 7.0V $V_{CPLV\_}$ = 2.5V, $I_{DUT\_}$ = -10mA, -20mA, -30mA		1.5		

ELECTRICAL CHARACTERISTICS (continued)

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACTIVE LOAD ($V_{COM\_}$ = 1.5V, R_L > 1MΩ, driver in high-impedance mode, unless otherwise noted)							
COM_ Voltage Range	$V_{COM\_}$	MAX9975AR		-1.0		+6.0	V
		MAX9975AZ		-0.5		+6.5	
Differential Voltage Range		$V_{DUT\_}$ - $V_{COM\_}$		-7.5		+7.5	V
COM_ Offset Voltage	V_{OS}	I_{SOURCE} = I_{SINK} = 20mA				±100	mV
Offset-Voltage Temperature Coefficient					+100		µV/°C
COM_ Voltage Gain	A_V	$V_{COM\_}$ = 0, 4.5V, I_{SOURCE} = I_{SINK} = 20mA		0.98		1.00	V/V
Voltage-Gain Temperature Coefficient					-10		ppm/°C
COM_ Linearity Error (Note 10)		MAX9975AR	$V_{COM\_}$ = -1V, +6V I_{SOURCE} = I_{SINK} = 20mA		±3	±15	mV
		MAX9975AZ	$V_{COM\_}$ = -0.5V, +6.5V I_{SOURCE} = I_{SINK} = 20mA		±3	±15	
COM_ Output Voltage Power-Supply Rejection Ratio	PSRR	$V_{COM\_}$ = 2.5V, I_{SOURCE} = I_{SINK} = 20mA (Note 11)				±10	mV/V
Output Resistance, Sink or Source	Ro	MAX9975AR $V_{DUT\_}$ = 3V, 6.5V with $V_{COM\_}$ = -1V and $V_{DUT\_}$ = -1.5V, +2V with $V_{COM\_}$ = +6.0V	I_{SOURCE} = I_{SINK} = 35mA	30			kΩ
			I_{SOURCE} = I_{SINK} = 1mA	500			
		MAX9975AZ $V_{DUT\_}$ = 3.5V, 7.0V with $V_{COM\_}$ = -0.5V and $V_{DUT\_}$ = -1.0V, +2.5V with $V_{COM\_}$ = +6.5V	I_{SOURCE} = I_{SINK} = 35mA	30			
			I_{SOURCE} = I_{SINK} = 1mA	500			
Output Resistance, Linear Region	Ro	$I_{DUT\_}$ = ±33.25mA, I_{SOURCE} = I_{SINK} = 35mA, $V_{COM\_}$ = 2.5V verified by deadband test			11	18	Ω
Deadband		$V_{COM\_}$ = 2.5V, 95% I_{SOURCE} to 95% I_{SINK}			700	1000	mV
SOURCE CURRENT ($V_{DUT\_}$ = 4.5V)							
Maximum Source Current		$V_{LDL\_}$ = 3.8V		36		40	mA
Source Programming Gain	A_{TC}	$V_{LDL\_}$ = 0.2V, 3V, $V_{LDH\_}$ = 0.1V		9.75	10	10.25	mA/V
Source Current Offset (Combined Offset of LDL_ and GS)	I_{OS}	$V_{LDL\_}$ = 200mV		-1000		0	µA
Source-Current Temperature Coefficient		I_{SOURCE} = 35mA			-15		µA/°C
Source-Current Power-Supply Rejection Ratio	PSRR	I_{SOURCE} = 25mA				±60	µA/V
		I_{SOURCE} = 35mA				±84	
Source Current Linearity (Note 25)		$V_{LDL\_}$ = 100mV, 1V, 2.25V				±60	µA
		$V_{LDL\_}$ = 3V				±130	

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

ELECTRICAL CHARACTERISTICS (continued)

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINK CURRENT ($V_{DUT\_}$ = -1.5V, MAX9975AR; $V_{DUT\_}$ = -1.0V, MAX9975AZ)							
Maximum Sink Current		$V_{LDH\_}$ = 3.8V		-40		-36	mA
Sink Programming Gain	A_{TC}	$V_{LDH\_}$ = 0.2V, 3V, $V_{LDL\_}$ = 0.1V		-10.25	-10	-9.75	mA/V
Sink Current Offset (Combined Offset of LDH_ and GS)	I_{OS}	$V_{LDH\_}$ = 200mV		0		1000	µA
Sink-Current Temperature Coefficient		I_{SINK} = 35mA			+8		µA/°C
Sink-Current Power-Supply Rejection Ratio	PSRR	I_{SINK} = 25mA				±60	µA/V
		I_{SINK} = 35mA				±84	
Sink Current Linearity (Note 25)		$V_{LDH\_}$ = 100mV, 1V, 2.25V				±60	µA/V
		$V_{LDH\_}$ = 3V				±130	
GROUND SENSE							
GS Voltage Range	V_{GS}	Verified by GS common-mode error test		-250		+250	mV
GS Common-Mode Error		MAX9975AR	$V_{DUT\_}$ = -1.5V, V_{GS} = ±250mV, $V_{LDH\_}$ - V_{GS} = 0.2V			±20	µA
			$V_{DUT\_}$ = +4.5V, V_{GS} = ±250mV, $V_{LDL\_}$ - V_{GS} = 0.2V			±20	
		MAX9975AZ	$V_{DUT\_}$ = -1V, V_{GS} = ±250mV, $V_{LDH\_}$ - V_{GS} = 0.2V			±20	
			$V_{DUT\_}$ = +4.5V, V_{GS} = ±250mV, $V_{LDL\_}$ - V_{GS} = 0.2V			±20	
GS Input Bias Current		V_{GS} = 0V				±25	µA
AC CHARACTERISTICS (Z_L = 50Ω to GND)							
Enable Time (Note 26)	t_{EN}	I_{SOURCE} = 10mA, $V_{COM\_}$ = -1V		2.7	3.5	4.3	ns
		I_{SINK} = 10mA, $V_{COM\_}$ = 1V		2.7	3.5	4.3	
Disable Time (Note 26)	t_{DIS}	I_{SOURCE} = 10mA, $V_{COM\_}$ = 1V		1.5	2	2.5	ns
		I_{SINK} = 10mA, $V_{COM\_}$ = -1V		1.5	2	2.5	
Current Settling Time on Commutation (Note 27)		I_{SOURCE} = I_{SINK} = 1mA	To 10%		15		ns
			To 1.5%		50		
		I_{SOURCE} = I_{SINK} = 20mA	To 10%		3	5	
			To 1.5%		15		
Spike During Enable/Disable Transition		I_{SOURCE} = I_{SINK} = 35mA, $V_{COM\_}$ = 0V			200	300	mV

ELECTRICAL CHARACTERISTICS (continued)

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

Note 1: All minimum and maximum DC measurements and driver 3V rise- and fall-time test limits are 100% production tested. All other test limits are guaranteed by design. Tests are performed at nominal supply voltages, unless otherwise noted.

Note 2: Total for dual device at worst-case setting.

Note 3: Does not include above ground internal dissipation of the comparator outputs. Additional power dissipation is typically (64mA x $V_{VCCO\_}$).

Note 4: Externally forced voltages may exceed this range provided that the Absolute Maximum Ratings are not exceeded.

Note 5: Transition time from LLEAK being asserted to leakage current dropping below specified limits.

Note 6: Based on simulation results only.

Note 7: Transition time from LLEAK being deasserted to output returning to normal operating mode.

Note 8: With the exception of offset and gain/CMRR tests, reference input values are calibrated for offset and gain.

Note 9: Relative to straight line between 0 and 4.5V.

Note 10: Specifications measured at the endpoints of the full range. Full range for the MAX9975AR is -1.3V ≤ $V_{DHV\_}$ ≤ +6.5V, -1.5V ≤ $V_{DLV\_}$ ≤ +6.3V, -1.5V ≤ $V_{DTV\_}$ ≤ +6.5V. Full range for the MAX9975AZ is -0.8V ≤ $V_{DHV\_}$ ≤ +7V, -1V ≤ $V_{DLV\_}$ ≤ +6.8V, -1V ≤ $V_{DTV\_}$ ≤ +7V.

Note 11: Change in offset voltage with power supplies independently set to their minimum and maximum values.

Note 12: Nominal target value is 48Ω. Contact factory for alternate trim selections within the 45Ω to 51Ω range.

Note 13: $V_{DTV\_}$ = midpoint of voltage swing, R_S = 50Ω. Measurement is made using the comparator.

Note 14: Measured from the crossing point of DATA_ inputs to the settling of the driver output.

Note 15: Prop delays are measured from the crossing point of the differential input signals to the 50% point of the expected output swing. Rise time of the differential inputs DATA_ and RCV_ are 250ps (10% to 90%).

Note 16: Rising edge to rising edge or falling edge to falling edge.

Note 17: Specified amplitude is programmed. At this pulse width, the output reaches at least 90% of its nominal (DC) amplitude. The pulse width is measured at DATA_.

Note 18: Specified amplitude is programmed. Maximum data rate is specified in transitions per second. A square wave that reaches at least 90% of its programmed amplitude may be generated at one-half of this frequency.

Note 19: Crosstalk from either driver to the other. Aggressor channel is driving $3V_{P-P}$ into a 50Ω load. Victim channel is in term mode with $V_{DTV\_}$ = +1.5V.

Note 20: Indicative of switching speed from DHV_ or DLV_ to DTV_ and DTV_ to DHV_ or DLV_ when $V_{DLV\_}$ < $V_{DTV\_}$ < $V_{DHV\_}$. If $V_{DTV\_}$ < $V_{DLV\_}$ or $V_{DTV\_}$ > $V_{DHV\_}$, switching speed is degraded by a factor of approximately 3.

Note 21: Change in offset voltage over the input range.

Note 22: Unless otherwise noted, all propagation delays are measured at 40MHz, $V_{DUT\_}$ = 0 to +1V, $V_{CHV\_}$ = $V_{CLV\_}$ = +0.5V, t_R = t_F = 250ps, Z_S = 50Ω, driver in term mode with $V_{DTV\_}$ = +0.5V. Comparator outputs are terminated with 50Ω to 0.9V and $V_{CCO\_}$ = 1.8V. Measured from $V_{DUT\_}$ crossing calibrated CHV_/CLV_ threshold to crossing point of differential outputs.

Note 23: At this pulse width, the output reaches at least 90% of its DC voltage swing. The pulse width is measured at the crossing points of the differential outputs.

Note 24: $V_{DUT\_}$ = $200mV_{P-P}$. Overdrive = 100mV.

Note 25: Relative to segmented interpolations between 200mV, 2V, 2.5V, and 3.5V.

Note 26: Measured from crossing of LDEN_ inputs to the 50% point of the output current change.

Note 27: V_{COM} = 1V, R_S = 50Ω, driving voltage = 1.55V to 0.45V transition and 0.45V to 1.55V transition (at 1mA) or +2.5V to -0.5V transition and -0.5V to +2.5V transition (at 20mA). Settling time is measured from $V_{DUT\_}$ = 1V to I_{SINK}/I_{SOURCE} settling within specified tolerance.

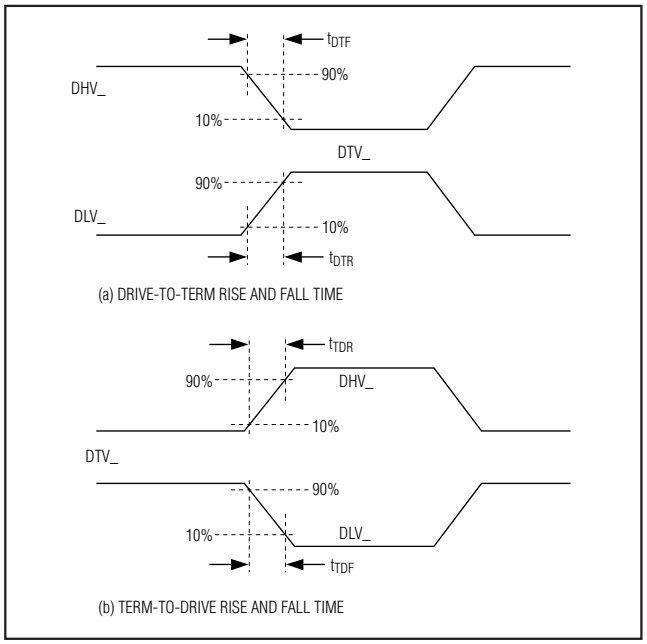


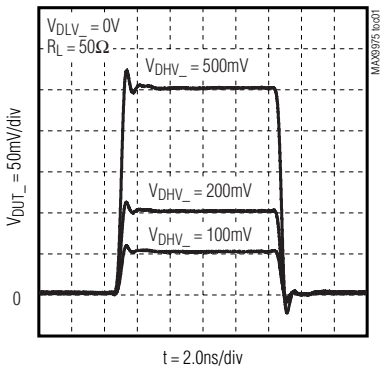
Figure 1. Drive-to-Term and Term-to-Drive Rise and Fall Times

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

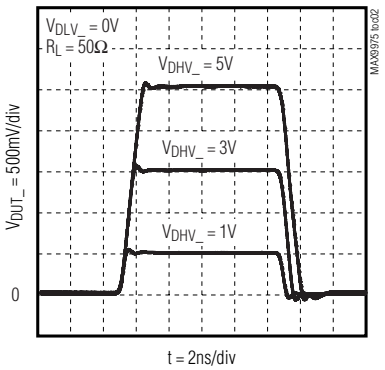
Typical Operating Characteristics

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, $R_{DUT\_}$ trimmed to 50Ω, T_J = +85°C, unless otherwise noted.)

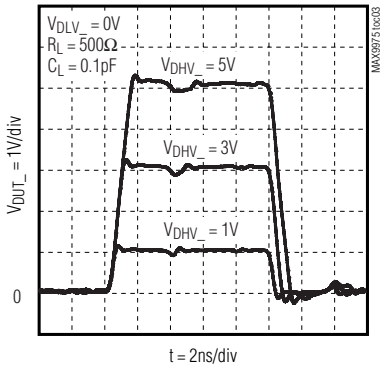
DRIVER SMALL-SIGNAL RESPONSE



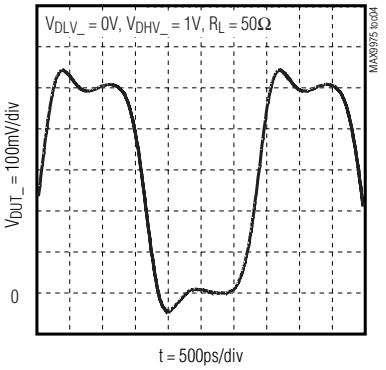
DRIVER LARGE-SIGNAL RESPONSE



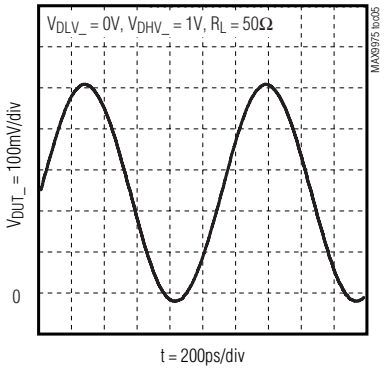
DRIVER LARGE-SIGNAL RESPONSE INTO 500Ω



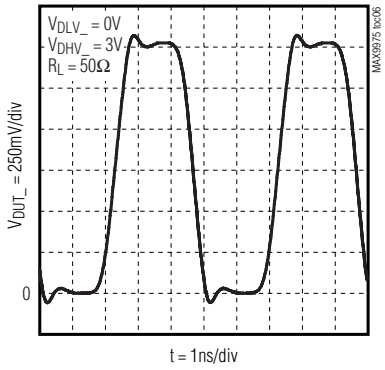
DRIVER 1V, 600Mbps SIGNAL RESPONSE



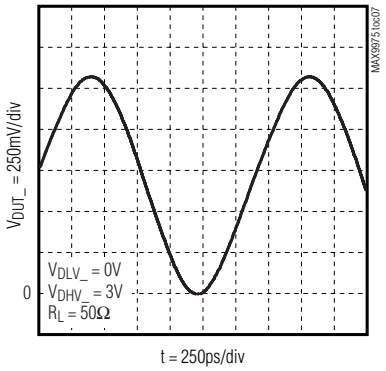
DRIVER 1V, 1800Mbps SIGNAL RESPONSE



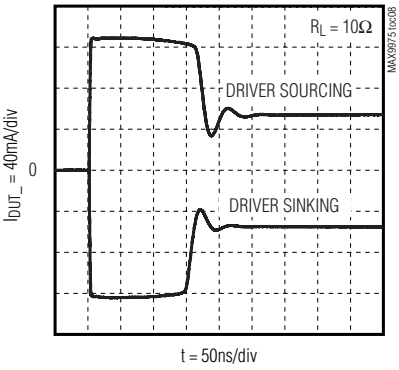
DRIVER 3V, 400Mbps SIGNAL RESPONSE



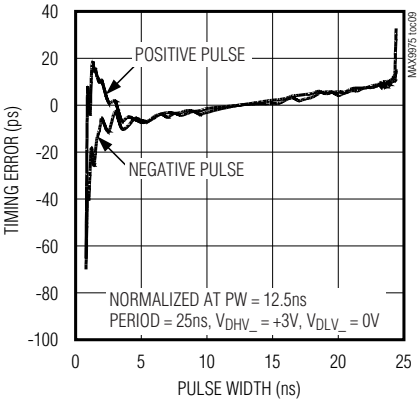
DRIVER 3V, 1200Mbps SIGNAL RESPONSE



DRIVER DYNAMIC CURRENT-LIMIT RESPONSE



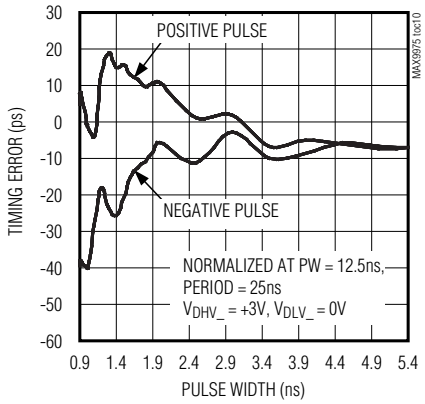
DRIVER 3V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH



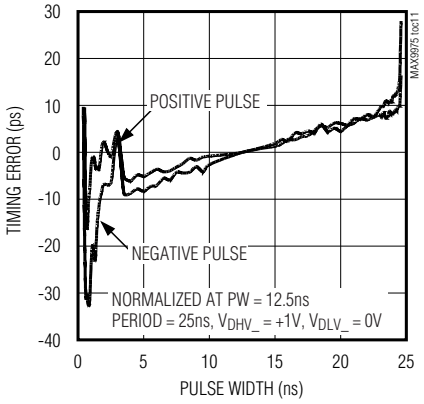
Typical Operating Characteristics (continued)

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, $R_{DUT\_}$ trimmed to 50Ω, T_J = +85°C, unless otherwise noted.)

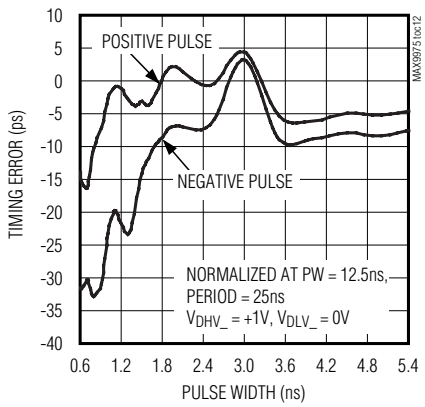
DRIVER 3V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH



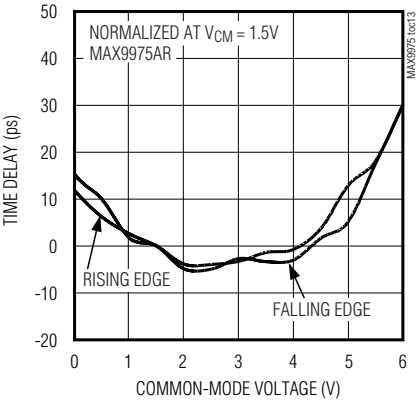
DRIVER 1V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH



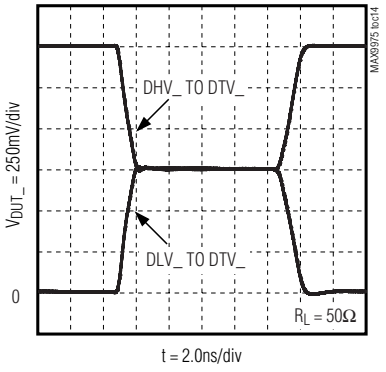
DRIVER 1V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH



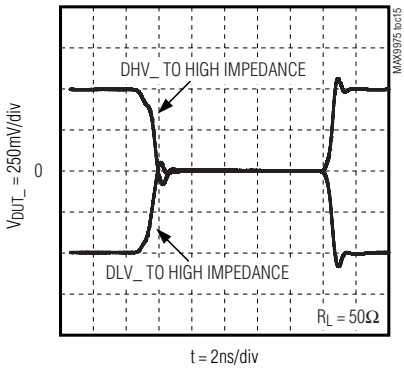
DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE



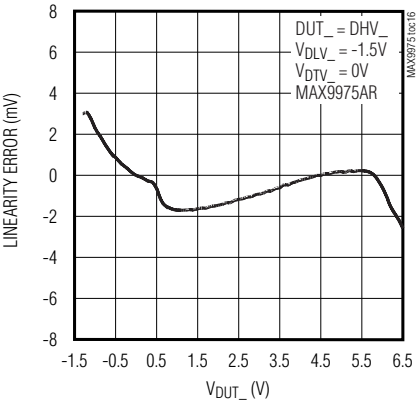
DRIVE-TO-TERM TRANSITION



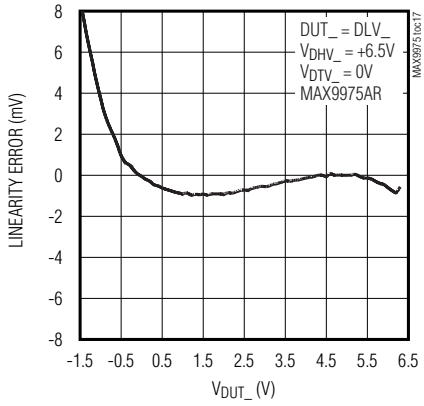
DRIVE TO HIGH-IMPEDANCE TRANSITION



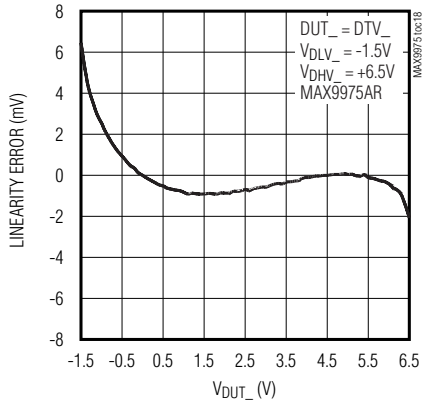
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE

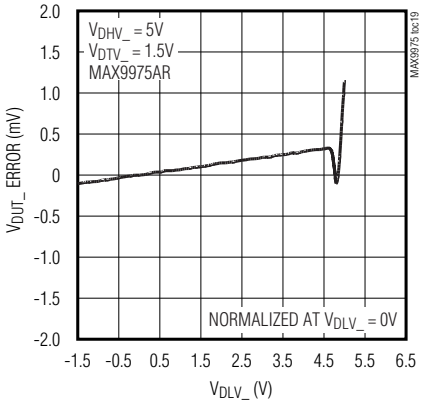


Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

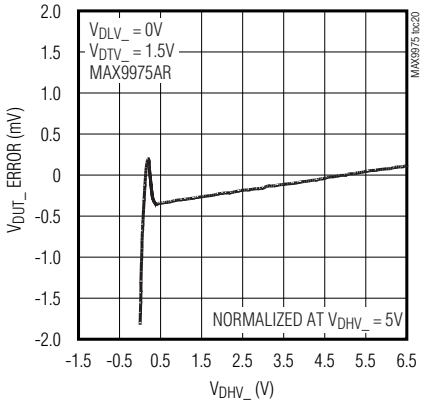
Typical Operating Characteristics (continued)

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, $R_{DUT\_}$ trimmed to 50Ω, T_J = +85°C, unless otherwise noted.)

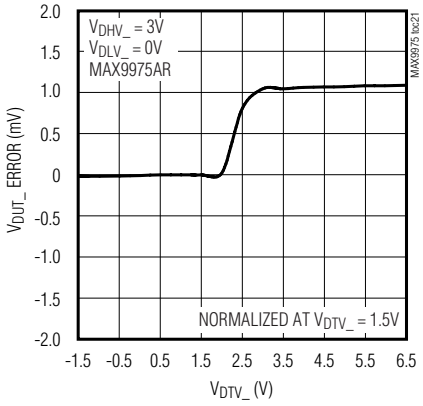
CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DHV_



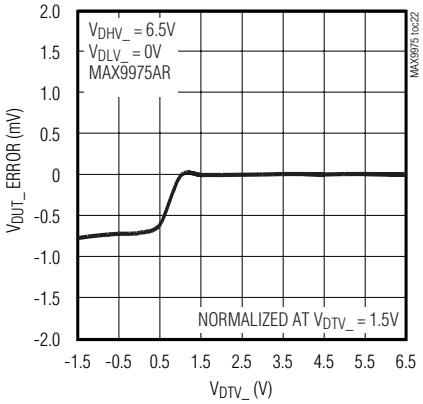
CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DLV_



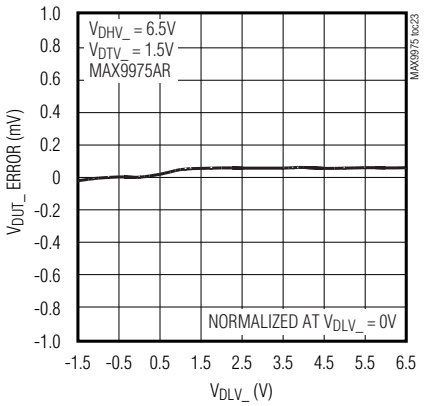
CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DHV_



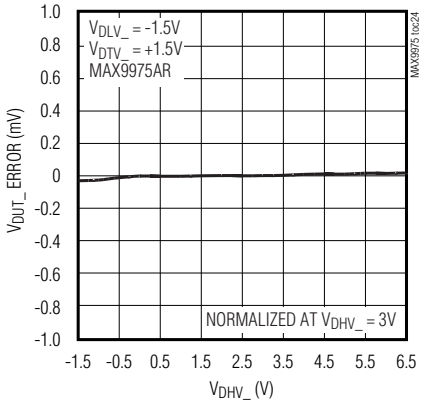
CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DLV_



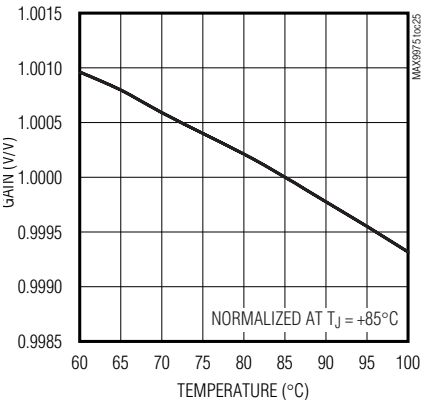
CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DTV_



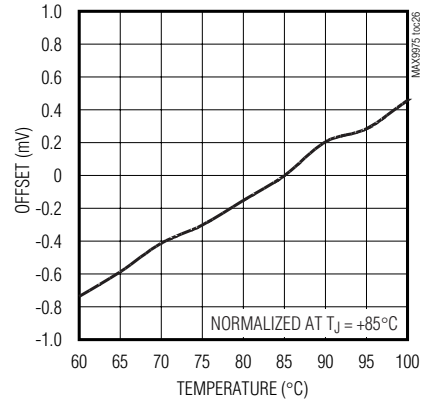
CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DTV_



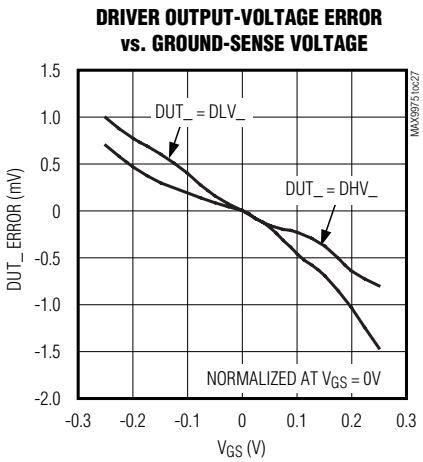
DRIVER GAIN vs. TEMPERATURE



DRIVER OFFSET vs. TEMPERATURE



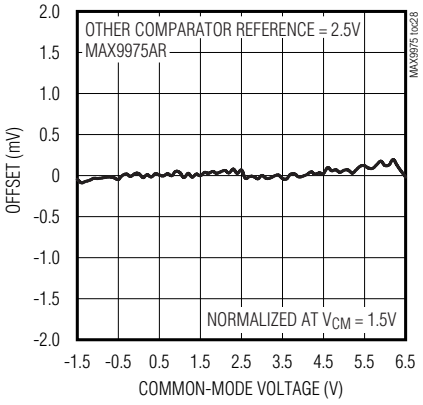
DRIVER OUTPUT-VOLTAGE ERROR vs. GROUND-SENSE VOLTAGE



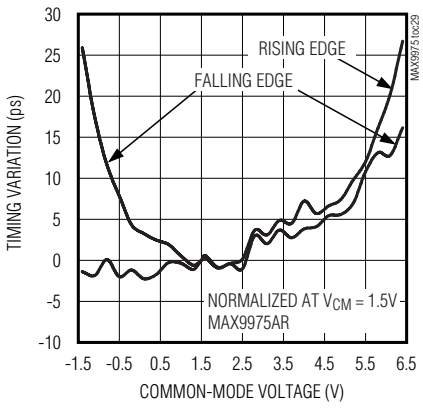
Typical Operating Characteristics (continued)

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, $R_{DUT\_}$ trimmed to 50Ω, T_J = +85°C, unless otherwise noted.)

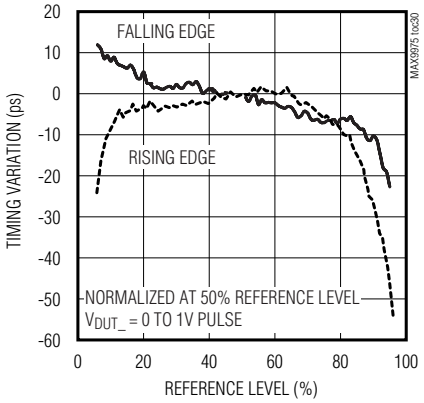
COMPARATOR OFFSET vs. COMMON-MODE VOLTAGE



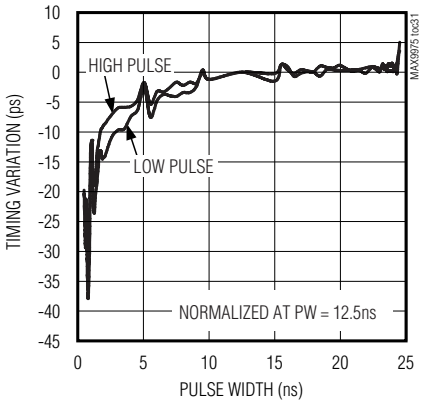
COMPARATOR TIMING VARIATION vs. COMMON-MODE VOLTAGE



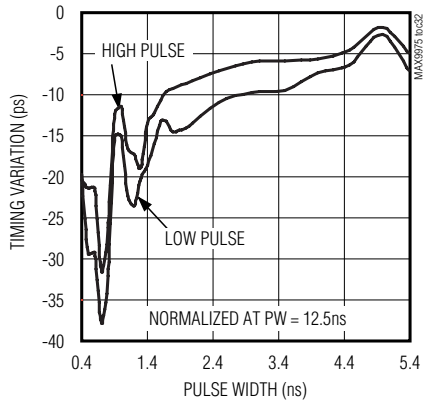
COMPARATOR WAVEFORM TRACKING



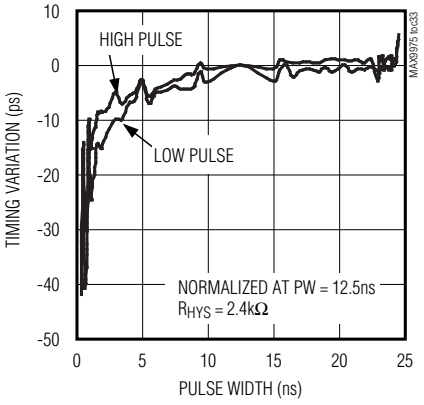
COMPARATOR TRAILING-EDGE TIMING VARIATION vs. PULSE WIDTH



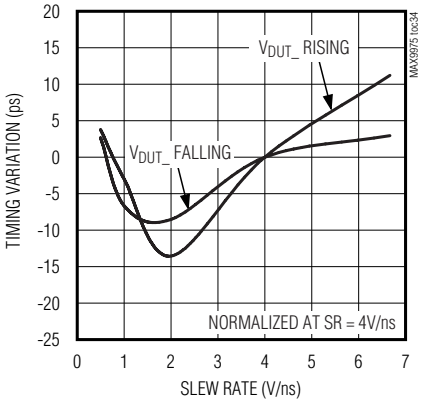
COMPARATOR TRAILING-EDGE TIMING VARIATION vs. PULSE WIDTH



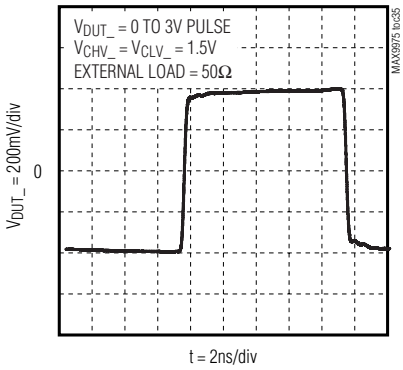
COMPARATOR WITH HYSTERESIS TRAILING-EDGE TIMING VARIATION vs. PULSE WIDTH



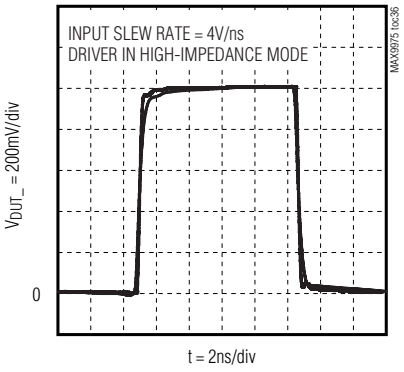
COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE



COMPARATOR DIFFERENTIAL OUTPUT RESPONSE



COMPARATOR RESPONSE TO HIGH SLEW-RATE OVERDRIVE

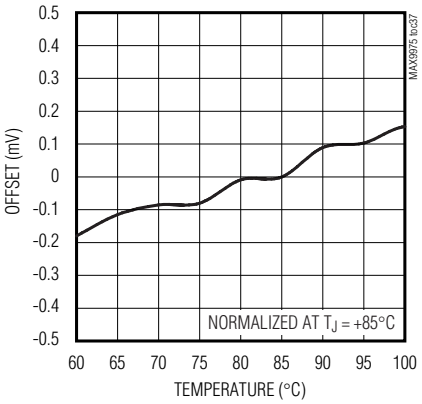


Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

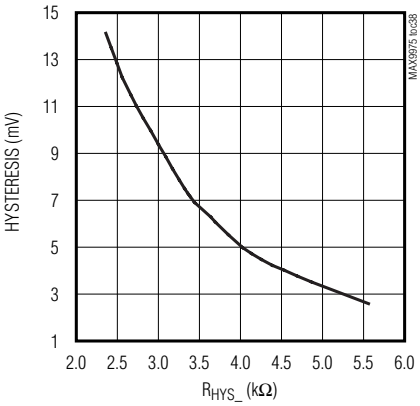
Typical Operating Characteristics (continued)

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, $R_{DUT\_}$ trimmed to 50Ω, T_J = +85°C, unless otherwise noted.)

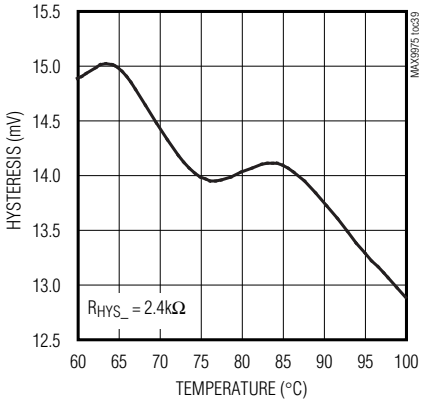
COMPARATOR OFFSET vs. TEMPERATURE



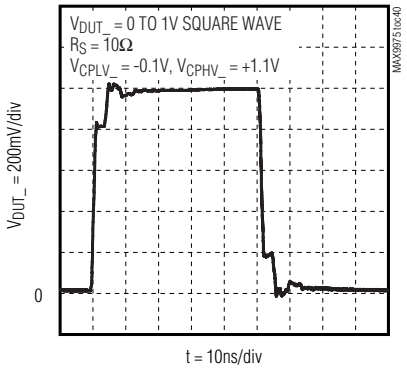
COMPARATOR HYSTERESIS vs. $R_{HYS\_}$ TO GND



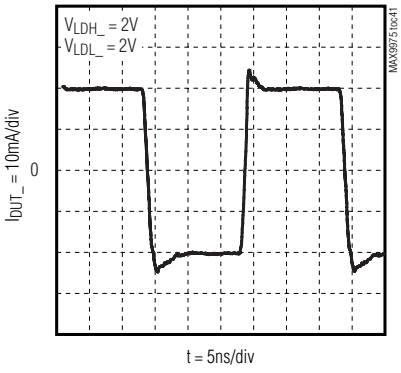
COMPARATOR HYSTERESIS vs. TEMPERATURE



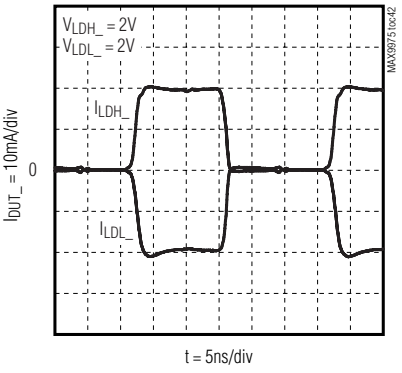
CLAMP RESPONSE AT SOURCE



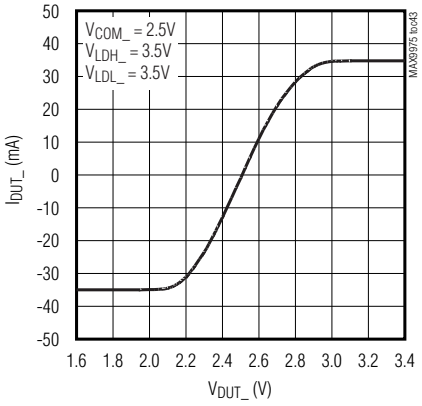
ACTIVE-LOAD COMMUTATION SIGNAL RESPONSE



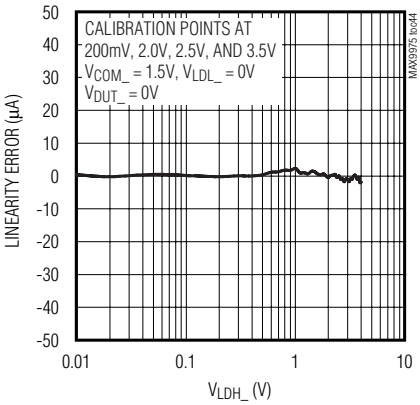
ACTIVE-LOAD ENABLE SIGNAL RESPONSE



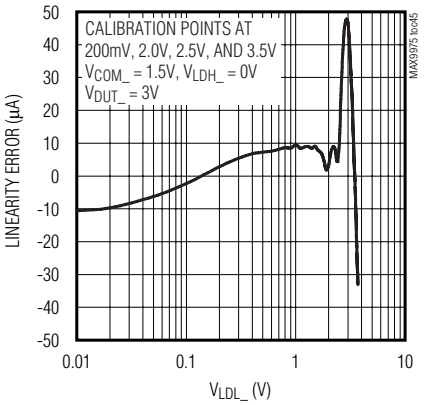
ACTIVE-LOAD CURRENT vs. LOAD VOLTAGE



ACTIVE-LOAD LINEARITY $I_{DUT\_}$ ERROR vs. $V_{LDH\_}$



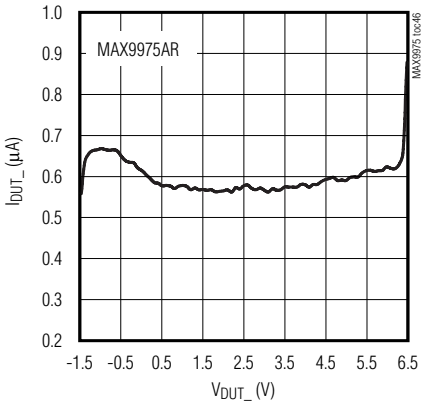
ACTIVE-LOAD LINEARITY $I_{DUT\_}$ ERROR vs. $V_{LDL\_}$



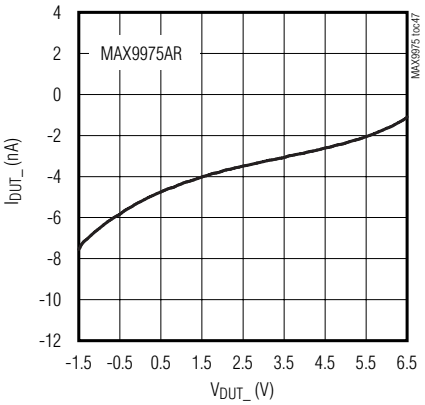
Typical Operating Characteristics (continued)

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, $R_{DUT\_}$ trimmed to 50Ω, T_J = +85°C, unless otherwise noted.)

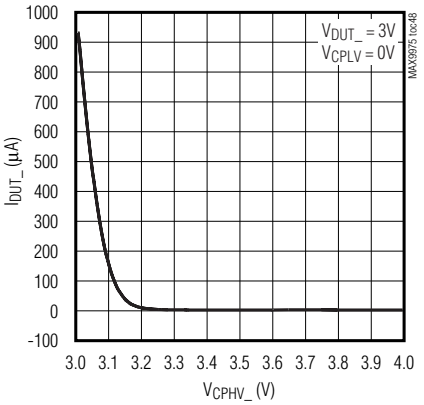
HIGH-IMPEDANCE CURRENT vs. DUT_ VOLTAGE



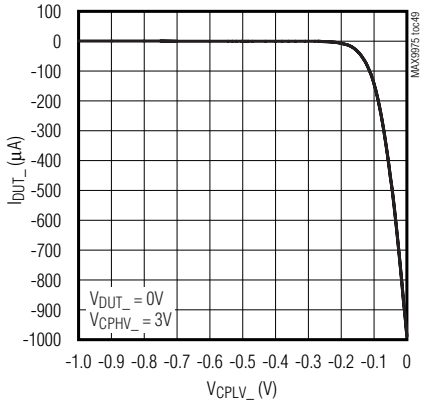
LOW-LEAKAGE CURRENT vs. DUT_ VOLTAGE



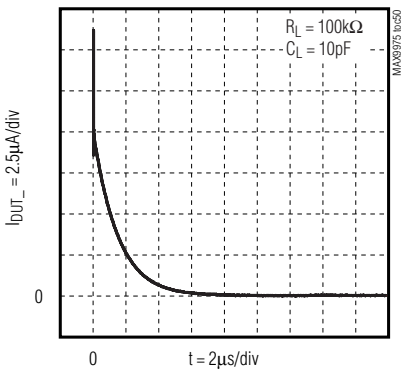
CLAMP CURRENT vs. DIFFERENCE VOLTAGE



CLAMP CURRENT vs. DIFFERENCE VOLTAGE



DRIVE 1V TO LOW-LEAKAGE TRANSITION

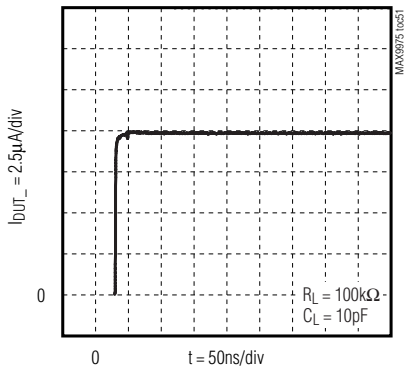


Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

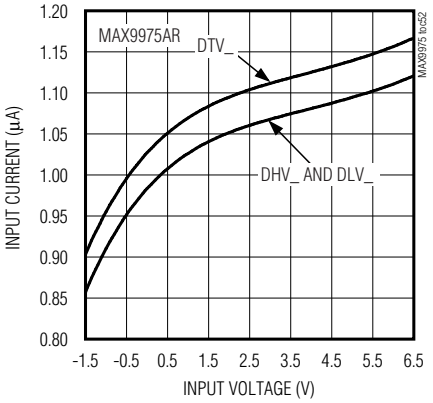
Typical Operating Characteristics (continued)

(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, $R_{DUT\_}$ trimmed to 50Ω, T_J = +85°C, unless otherwise noted.)

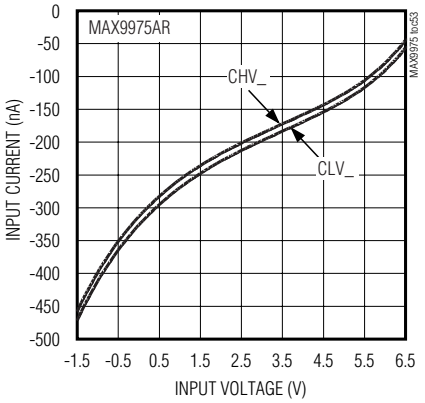
LOW-LEAKAGE TO DRIVE 1V TRANSITION



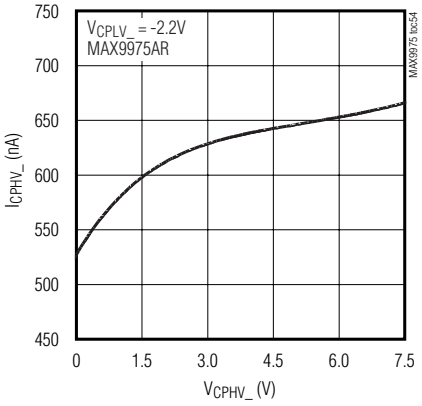
DRIVER REFERENCE CURRENT vs. DRIVER REFERENCE VOLTAGE



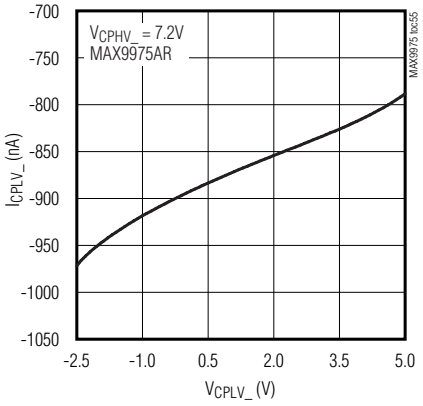
COMPARATOR REFERENCE CURRENT vs. INPUT VOLTAGE



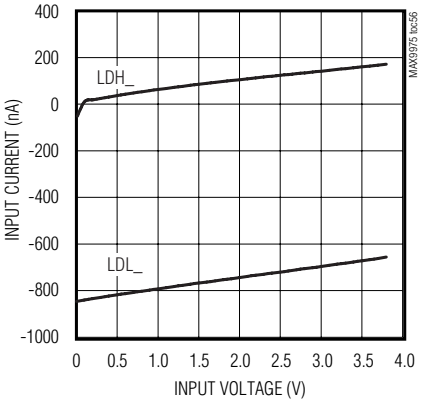
INPUT CURRENT vs. INPUT VOLTAGE, CPHV_



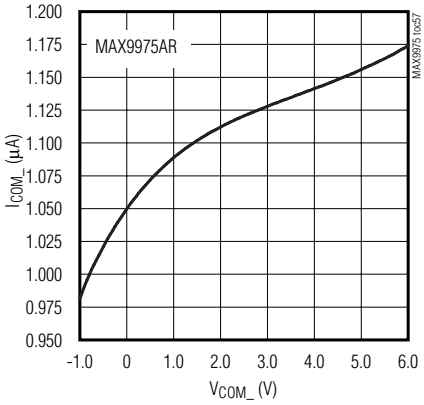
INPUT CURRENT vs. INPUT VOLTAGE, CPLV_



LOAD-REFERENCE INPUT CURRENT vs. INPUT VOLTAGE



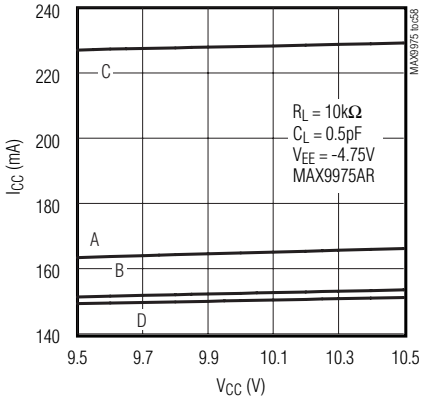
INPUT CURRENT vs. INPUT VOLTAGE, COM_



Typical Operating Characteristics (continued)

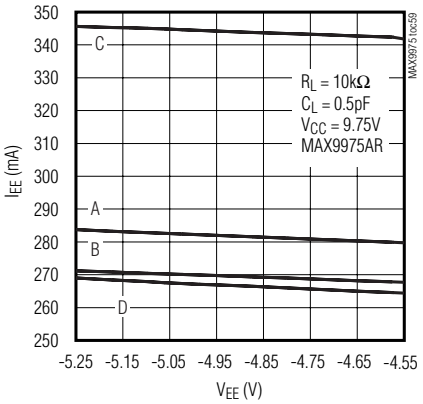
(MAX9975AR: V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V. MAX9975AZ: V_{CC} = +10.25V, V_{EE} = -4.25V, $V_{CPHV\_}$ = +7.7V, $V_{CPLV\_}$ = -1.7V. $V_{CCO\_}$ = +1.8V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, V_{GS} = 0V, $R_{HYS\_}$ = open, $R_{DUT\_}$ trimmed to 50Ω, T_J = +85°C, unless otherwise noted.)

SUPPLY CURRENT I_{CC} vs. SUPPLY VOLTAGE V_{CC}



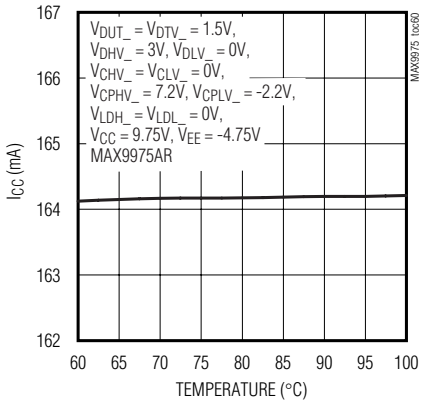
A: $V_{DUT\_}$ = $V_{DTV\_}$ = 1.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{CHV\_}$ = $V_{CLV\_}$ = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, I_{SINK} = I_{SOURCE} = 0
B: SAME AS A EXCEPT DRIVER DISABLED HIGH IMPEDANCE AND LOAD ENABLED
C: SAME AS B EXCEPT I_{SOURCE} = I_{SINK} = 35mA, $V_{COM\_}$ = 1.5V, R_L = 0
D: SAME AS C EXCEPT LOW-LEAKAGE MODE ASSERTED

SUPPLY CURRENT I_{EE} vs. SUPPLY VOLTAGE V_{EE}

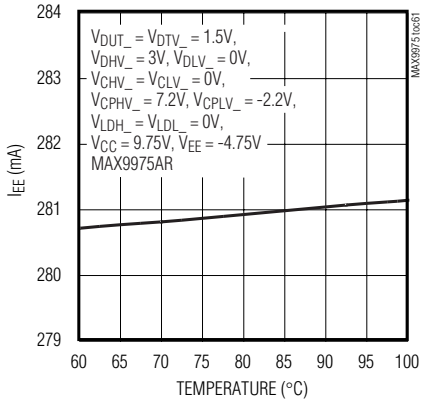


A: $V_{DUT\_}$ = $V_{DTV\_}$ = 1.5V, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0V, $V_{CHV\_}$ = $V_{CLV\_}$ = 0V, $V_{CPHV\_}$ = 7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0V, I_{SINK} = I_{SOURCE} = 0
B: SAME AS A EXCEPT DRIVER DISABLED HIGH IMPEDANCE AND LOAD ENABLED
C: SAME AS B EXCEPT I_{SOURCE} = I_{SINK} = 35mA, $V_{COM\_}$ = -1V, R_L = 0
D: SAME AS C EXCEPT LOW-LEAKAGE MODE ASSERTED

SUPPLY CURRENT I_{CC} vs. TEMPERATURE



SUPPLY CURRENT I_{EE} vs. TEMPERATURE



Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

Pin Description

PIN	NAME	FUNCTION
1	TEMP	Temperature Monitor Output
2, 9, 12, 14, 17, 24, 35, 45, 46, 60, 80, 81, 91	V_{EE}	Negative Power-Supply Input
3, 5, 10, 16, 21, 23, 25, 34, 43, 44, 82, 83, 92	GND	Ground Connection
4, 11, 15, 22, 33, 41, 42, 66, 84, 85, 93	V_{CC}	Positive Power-Supply Input
6, 8, 18, 20, 54, 72	N.C.	No Connection. Do not connect.
7	DUT1	Channel 1 DUT Input/Output. Combined I/O for driver, comparator, clamp, and load.
13	GS	Ground Sense. GS is the ground reference for LDH_ and LDL_.
19	DUT2	Channel 2 DUT Input/Output. Combined I/O for driver, comparator, clamp, and load.
26	CLV2	Channel 2 Low-Comparator Reference Input
27	CHV2	Channel 2 High-Comparator Reference Input
28	DLV2	Channel 2 Driver-Low Reference Input
29	DTV2	Channel 2 Driver-Termination Reference Input
30	DHV2	Channel 2 Driver-High Reference Input
31	CPLV2	Channel 2 Low-Clamp Reference Input
32	CPHV2	Channel 2 High-Clamp Reference Input
36	NCH2	Channel 2 High-Comparator Output. Differential output of channel 2 high comparator.
37	CH2	
38	V_{CCO2}	Channel 2 Collector Voltage Input. Voltage input for channel 2 comparator output termination resistors. Provides pullup voltage and current for the output termination resistors.
39	NCL2	Channel 2 Low-Comparator Output. Differential output of channel 2 low comparator.
40	CL2	
47	COM2	Channel 2 Active-Load Commutation-Voltage Reference Input

Pin Description (continued)

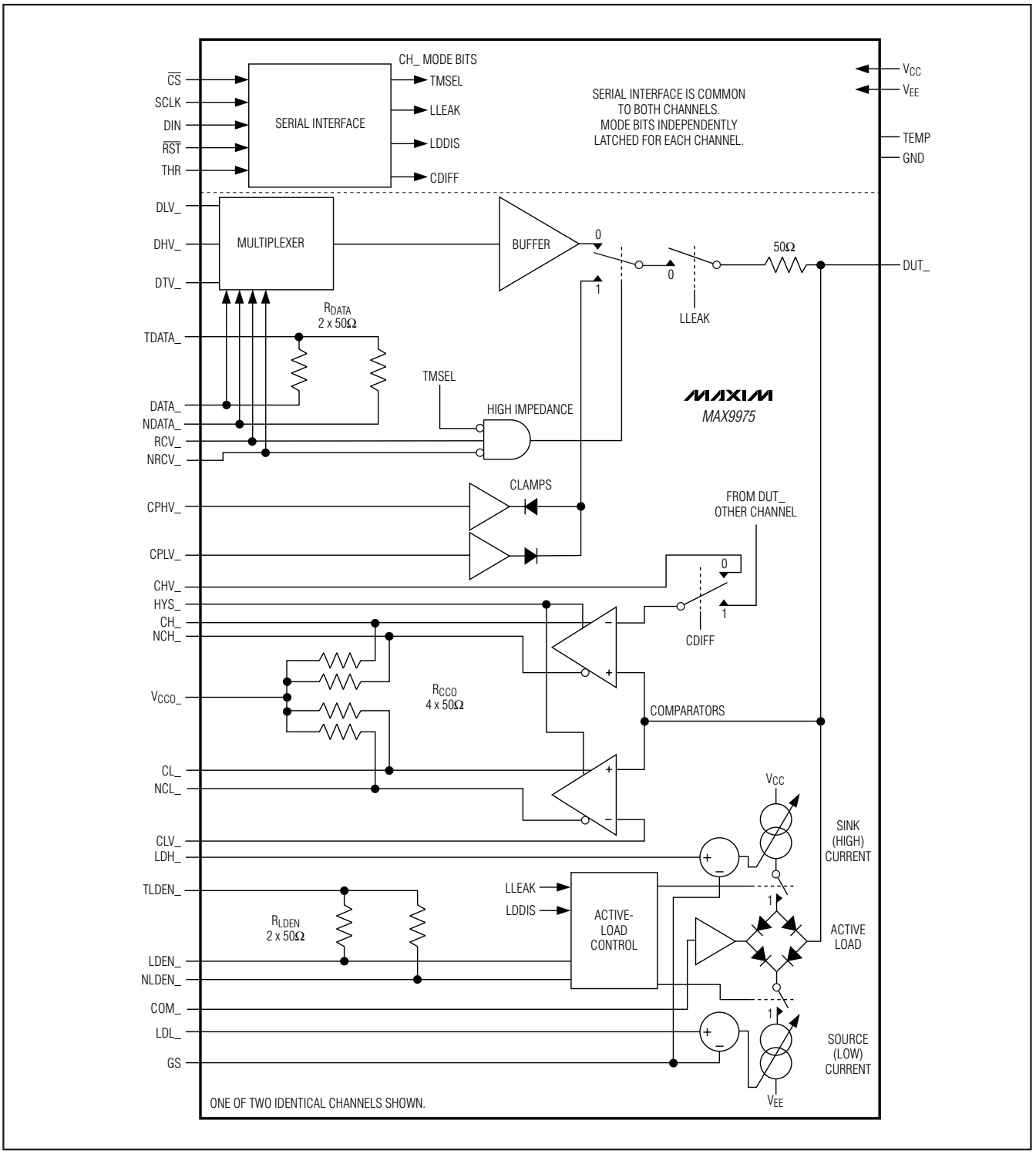
PIN	NAME	FUNCTION
48	LDL2	Channel 2 Active-Load Source-Current Reference Input
49	LDH2	Channel 2 Active-Load Sink-Current Reference Input
50	HYS2	Channel 2 Hysteresis Input for Single-Ended Compare Mode. See HYS1 when in differential compare mode. Nominal V_{HYS2} = -1V.
51	TDATA2	Channel 2 Data-Termination Voltage Input. Termination voltage input for the DATA2 and NDATA2 differential inputs.
52	NDATA2	Channel 2 Multiplexer Control Inputs. Differential controls DATA2 and NDATA2 select driver 2's input from DHV2 or DLV2. Drive DATA2 above NDATA2 to select DHV2. Drive NDATA2 above DATA2 to select DLV2.
53	DATA2	
55	NRCV2	Channel 2 Multiplexer Control Inputs. Differential controls RCV2 and NRCV2 place channel 2 in receive mode. Drive RCV2 above NRCV2 to place channel 2 into receive mode. Drive NRCV2 above RCV2 to place channel 2 into drive mode.
56	RCV2	
57	TLDEN2	Channel 2 Load-Enable Termination Voltage Input. Termination voltage input for the LDEN2 and NLDEN2 differential inputs.
58	NLDEN2	Channel 2 Multiplexer Control Inputs. Differential controls LDEN2 and NLDEN2 enable/disable the active load. Drive LDEN2 above NLDEN2 to enable the channel 2 active load. Drive NLDEN2 above LDEN2 to disable the channel 2 active load.
59	LDEN2	
61	$\overline{RST}$	Reset Input. Asynchronous reset input for the serial register. $\overline{RST}$ is active low.
62	$\overline{CS}$	Chip-Select Input. Serial port activation input. $\overline{CS}$ is active low.
63	THR	Single-Ended Logic Threshold. Leave THR unconnected to set the threshold to +1.25V or force THR to a desired threshold voltage.
64	SCLK	Serial Clock Input. Clock for serial port.
65	DIN	Data Input. Serial port data input.
67	LDEN1	Channel 1 Multiplexer Control Inputs. Differential controls LDEN1 and NLDEN1 enable/disable the active load. Drive LDEN1 above NLDEN1 to enable the channel 1 active load. Drive NLDEN1 above LDEN1 to disable the channel 1 active load.
68	NLDEN1	
69	TLDEN1	Channel 1 Load-Enable Termination Voltage Input. Termination voltage input for the LDEN1 and NLDEN1 differential inputs.

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

Pin Description (continued)

PIN	NAME	FUNCTION
70	RCV1	Channel 1 Multiplexer Control Inputs. Differential controls RCV1 and NRCV1 place channel 1 in receive mode. Drive RCV1 above NRCV1 to place channel 1 into receive mode. Drive NRCV1 above RCV1 to place channel 1 into drive mode.
71	NRCV1	
73	DATA1	Channel 1 Multiplexer Control Inputs. Differential controls DATA1 and NDATA1 select driver 1's input from DHV1 or DLV1. Drive DATA1 above NDATA1 to select DHV1. Drive NDATA1 above DATA1 to select DLV1.
74	NDATA1	
75	TDATA1	Channel 1 Data-Termination Voltage Input. Termination voltage input for the DATA1 and NDATA1 differential inputs.
76	HYS1	Channel 1 Hysteresis Input for Single-Ended Compare Mode. Channel 1 and channel 2 hysteresis input for differential compare mode. Nominal V_{HYS1} = -1V.
77	LDH1	Channel 1 Active-Load Sink-Current Reference Input
78	LDL1	Channel 1 Active-Load Source-Current Reference Input
79	COM1	Channel 1 Active-Load Commutation-Voltage Reference Input
86	CL1	Channel 1 Low-Comparator Output. Differential output of channel 1 low comparator.
87	NCL1	
88	V_{CCO1}	Channel 1 Collector Voltage Input. Voltage input for channel 1 comparator output termination resistors. Provides pullup voltage and current for the output termination resistors.
89	CH1	Channel 1 High-Comparator Output. Differential output of channel 1 high comparator.
90	NCH1	
94	CPHV1	Channel 1 High-Clamp Reference Input
95	CPLV1	Channel 1 Low-Clamp Reference Input
96	DHV1	Channel 1 Driver-High Reference Input
97	DTV1	Channel 1 Driver-Termination Reference Input
98	DLV1	Channel 1 Driver-Low Reference Input
99	CHV1	Channel 1 High-Comparator Reference Input
100	CLV1	Channel 1 Low-Comparator Reference Input

Functional Diagram



Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

Detailed Description

The MAX9975 dual, low-power, high-speed, pin-electronics DCL IC includes, for each channel, a three-level pin driver, a dual comparator, variable clamps, and an active load. An additional differential comparator allows comparisons between the two channels. The driver features a -1.5V to +6.5V (MAX9975AR) or a -1.0V to +7.0V (MAX9975AZ) operating range and high-speed operation, includes high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low voltage swings. The dual comparator provides low dispersion (timing variation) over a wide variety of input conditions, and differential outputs. The clamps provide damping of high-speed DUT waveforms when the device is configured as a high-impedance receiver. The programmable load supplies up to 35mA of source and sink current. The load facilitates contact/continuity testing, at-speed parametric test of I_{OH} and I_{OL}, and pullup of high-output-impedance devices.

Internal resistors at the high-speed inputs provide compatibility with CML interfaces. In addition, flexible open-collector outputs with optional internal pullup resistors are available for the comparators. These features significantly reduce the discrete component count on the circuit board.

A 3-wire, low-voltage CMOS-compatible serial interface programs the low-leakage, load-disable, slew-rate, differential/window comparator and tri-state/terminate operational configurations of the MAX9975.

MAX9975 and MAX9969 Compatibility

The MAX9975 is pin compatible and functionally similar to the MAX9969. The MAX9975 differs from the MAX9969 in the following ways.

- The MAX9975 has lower DHV_, DLV_, and DTV_ gain errors.
- The MAX9975 has no programmable slew-rate control; the slew rate control bits are ignored.
- The MAX9975 features programmable hysteresis.
- The MAX9975 features double the comparator output current.
- The MAX9975AZ features a -1V to +7V operating range.

Output Driver

The driver input is a high-speed multiplexer that selects one of three voltage inputs: DHV_, DLV_, or DTV_. This switching is controlled by high-speed inputs DATA_ and RCV_ and mode-control bit TMSEL (Table 1).

DUT_ can be toggled at high speed between the buffer output and high-impedance mode, or it can be placed into low-leakage mode (Figure 2, Table 1). In high-impedance mode, the clamps are connected. High-speed input RCV_ and mode-control bits TMSEL and

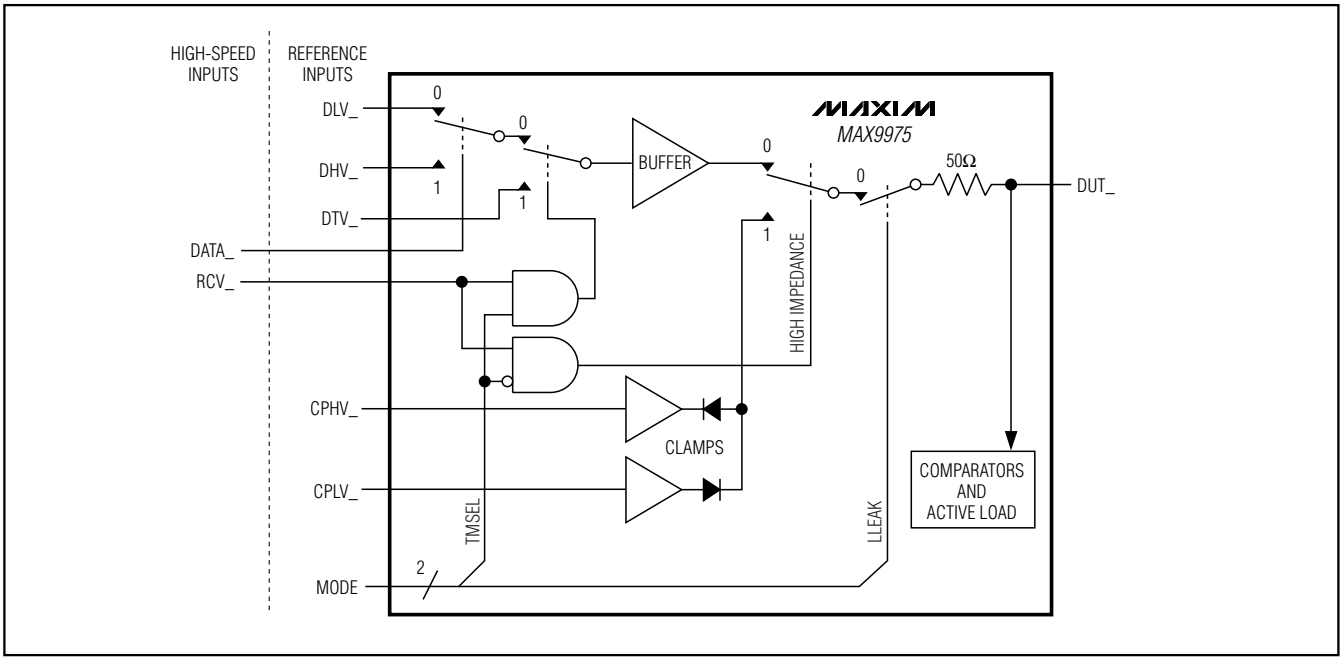


Figure 2. Simplified Driver Channel

Table 1. Driver Logic

EXTERNAL CONNECTIONS		INTERNAL CONTROL REGISTER		DRIVER OUTPUT
DATA	RCV	TMSEL	LLEAK	
1	0	X	0	Drive to DHV_
0	0	X	0	Drive to DLV_
X	1	1	0	Drive to DTV_ (term mode)
X	1	0	0	High-impedance mode (high-Z)
X	X	X	1	Low-leakage mode

LLEAK control the switching. In high-impedance mode, the bias current at DUT_ is less than 3µA over the 0 to 3V range, while the node maintains its ability to track high-speed signals. In low-leakage mode, the bias current at DUT_ is further reduced to less than 15nA, and signal tracking slows. See the *Low-Leakage Mode, LLEAK* section for more details.

The nominal driver output resistance can be trimmed to different values. Contact the factory for different resistance values within the 45Ω to 51Ω range.

Clamps

Configure the voltage clamps (high, CPHV_ and low, CPLV_) to limit the voltage at DUT_ and to suppress reflections when the channel is configured as a high-impedance receiver. The clamps behave as diodes connected to the outputs of high-current buffers. Internal circuitry compensates for the diode drop at 1mA clamp current. Set the clamp voltages using the external connections CPHV_ and CPLV_. The clamps are enabled only when the driver is in high-impedance mode (Figure 2). For transient suppression, set the clamp voltages to approximately the minimum and maximum expected DUT_ voltage range. The optimal clamp voltages are application specific and must be empirically determined. If clamping is not desired, set the clamp voltages at least 0.7V outside the expected DUT_ voltage range; overvoltage protection remains active without loading DUT_.

Comparators

The MAX9975 provides two independent high-speed comparators for each channel. Each comparator has one input connected internally to DUT_ and the other input connected to either CHV_ or CLV_ (see the *Functional Diagram*). Comparator outputs are a logical result of the input conditions, as indicated in Tables 2 and 3.

The comparator differential outputs are open-collector outputs to ease interfacing with a wide variety of logic families. Internal termination resistors switch a 16mA current source between the two outputs (Figure 3). The termination resistors connect the outputs to voltage input $V_{CCO\_}$. Connect $V_{CCO\_}$ to the desired V_{OH} voltage. Each output provides a nominal $800mV_{P-P}$ swing and 50Ω source termination. If an additional external 50Ω destination termination is used to double-terminate the line, the nominal 800mV swing will be halved.

The upper comparators are configurable as differential receivers for LVDS and other differential DUT_ signals. When mode bit CDIFF is asserted, the upper comparator inputs are routed from the DUT_ outputs for both channels.

Hysteresis

The comparator function incorporates hysteresis control. Hysteresis rejects noise and prevents oscillations on low-slew input signals. External resistors control hysteresis levels. HYS1 controls channel 1 and HYS2 controls channel 2, when the MAX9975 is programmed in single-ended compare mode (CDIFF = 0). HYS1 also controls channel 2's high-comparator output when the MAX9975 is programmed in differential compare mode (CDIFF = 1). With HYS_ unconnected, the programmed hysteresis is 0mV. Connect an external resistor between HYS_ and GND to program nonzero hysteresis. See the *Typical Operating Characteristics* for typical resistance values.

Table 2. Comparator Logic, CDIFF = 0 (Single-Ended Compare Mode)

SC1	SC0	DRIVER SLEW RATE (%)
0	0	100
0	1	75
1	0	50
1	1	25

Table 3. Comparator Logic, CDIFF = 1 (Differential Compare Mode)

DUT1 > DUT2	DUT_ > CLV_	CL_	CH_
0	0	0	0
0	1	1	0
1	0	0	1
1	1	1	1

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

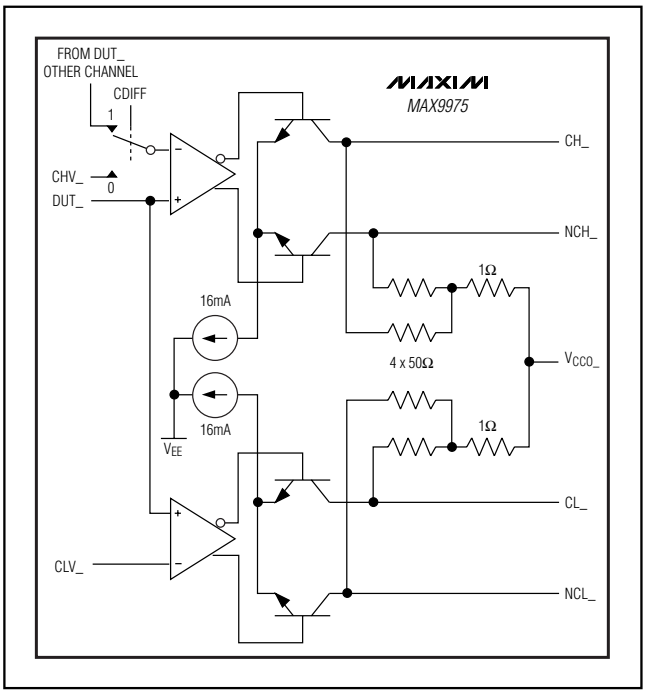


Figure 3. Open-Collector Comparator Outputs

Active Load

The active load consists of linearly programmable, Class AB source and sink current sources, a commutation buffer, and a diode bridge (see the *Functional Diagram*). Analog control inputs LDH_ and LDL_ program the sink and source currents, respectively, within the 0 to 35mA range. Analog reference input COM_ sets the commutation buffer output voltage. The source and sink naming convention is referenced to the DUT. Current out of the MAX9975 constitutes sink current and current into the MAX9975 constitutes source current. The Class AB loads of the MAX9975 offer substantial efficiency improvement over conventional active-load circuitry.

The programmed source (low) current loads the DUT when $V_{DUT\_} > V_{COM\_}$. The programmed sink (high) current loads the DUT when $V_{DUT\_} < V_{COM\_}$.

High-speed differential input LDEN_ and 2 bits of the control word (LDDIS and LLEAK) control the load (Table 4). When the load is enabled, the internal source and sink current sources connect to the diode bridge. When the load is disabled, the internal current sources shunt to ground and the top and bottom of the bridge float (see the *Functional Diagram*). LLEAK places the load in low-leakage mode, and overrides LDEN_. See the *Low-Leakage Mode, LLEAK* section for more detailed information.

LDDIS

In some tester configurations, the load enable is driven with the complement of the driver high-impedance signal (RCV_), so disabling the driver enables the load and vice versa. The LDDIS signal allows the load to be disabled independent of the state of LDEN_ (Table 4).

GS Input

GS is the ground-sense input. A level-setting DAC, such as the MAX5631 or MAX5734, programs the MAX9975's active load, driver, comparator, and clamps. Although all the DAC levels are typically offset by V_{GS}, the operation of the MAX9975's ground-sense input nullifies this offset with respect to the active-load current. Connect GS to the same ground reference used by the DAC. ($V_{LDL\_}$ - V_{GS}) sets the source current by +10mA/V. ($V_{LDH\_}$ - V_{GS}) sets the sink current by -10mA/V.

To maintain an 8V range in the presence of GS variations, GS offsets DHV_, DLV_, DTV_, CPHV_, CPLV_, and COM_ ranges. Adequate supply headroom must be maintained in the presence of GS variations. Ensure:

$$V_{CC} \geq 9.5V + Max(V_{GS}) \text{ (MAX9975AR)}$$

$$V_{CC} \geq 10.0V + Max(V_{GS}) \text{ (MAX9975AZ)}$$

$$V_{EE} \leq -4.5V + Min(V_{GS}) \text{ (MAX9975AR)}$$

$$V_{EE} \leq -4.0V + Min(V_{GS}) \text{ (MAX9975AZ)}$$

Low-Leakage Mode, LLEAK

Asserting LLEAK through the serial port or with $\overline{RST}$ places the MAX9975 into a very low-leakage state (see the *Electrical Characteristics* table). With LLEAK asserted, the comparators function at a reduced speed, and

Table 4. Active-Load Programming

EXTERNAL CONNECTIONS	INTERNAL CONTROL REGISTER		MODE
LDEN_	LDDIS	LLEAK	
0	0	0	Normal operating mode, load disabled
1	0	0	Normal operating mode, load enabled
X	1	0	Load disabled
X	X	1	Low-leakage mode

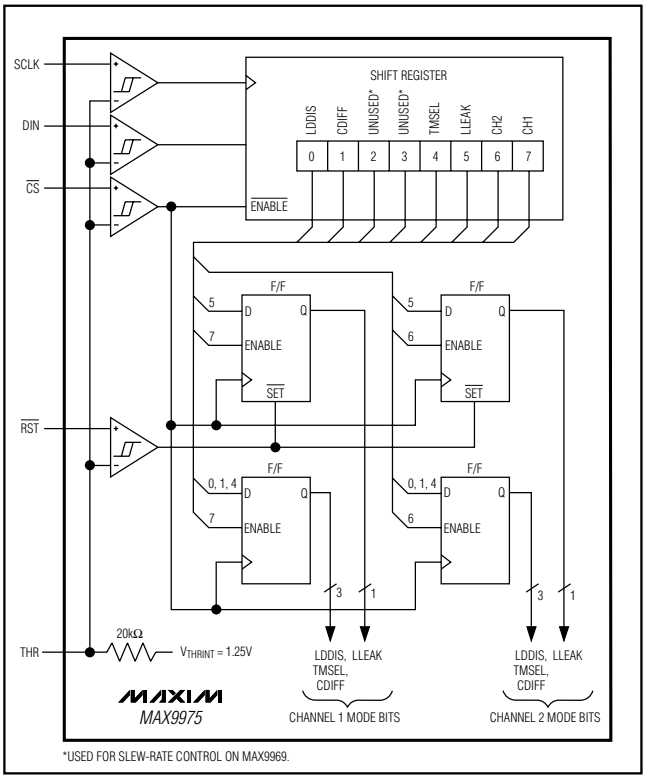


Figure 4. Serial Interface

the driver, clamps, and active load are disabled. This mode is convenient for making IDDQ and PMU measurements without the need for an output disconnect relay. LLEAK is programmed independently for each channel.

When DUT_ is driven with a high-speed signal while LLEAK is asserted, the leakage current momentarily increases beyond the limits specified for normal operation. The low-leakage recovery specification in the *Electrical Characteristics* table indicates device behavior under this condition.

Serial Interface and Device Control

A CMOS-compatible serial interface controls the MAX9975 modes (Figure 4 and Table 5). Control data flow into an 8-bit shift register (MSB first) and are latched when $\overline{CS}$ is taken high, as shown in Figure 5. Latches contain 6 control bits for each channel of the dual-pin driver. Data from the shift register are loaded to either or both of the latches as determined by bits D6 and D7. When CDIFF = 1, its effect is independent of bits D6 and D7. The control bits, in conjunction with external inputs DATA_ and RCV_, manage the features of each channel, as shown in Tables 1 and 2. $\overline{RST}$ sets LLEAK = 1 for both channels, forcing them into low-leakage mode. All other bits are unaffected. At power-up, hold $\overline{RST}$ low until V_{CC} and V_{EE} have stabilized.

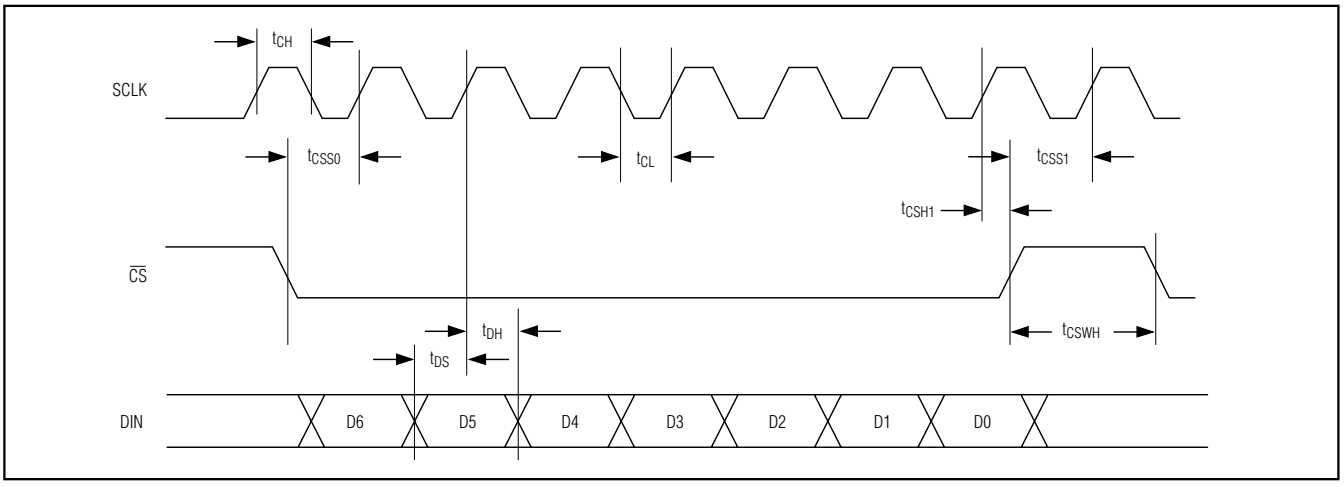


Figure 5. Serial-Interface Timing

Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

Table 5. Shift Register Functions

BIT	NAME	DESCRIPTION
D7	CH1	Channel 1 Write Enable. Set to 1 to update the control byte for channel 1. Set to 0 to make no changes to channel 1.
D6	CH2	Channel 2 Write Enable. Set to 1 to update the control byte for channel 2. Set to 0 to make no changes to channel 2.
D5	LLEAK	Low-Leakage Select. Set to 1 to put driver, load, and clamps in low-leakage mode. Comparators remain active in low-leakage mode, but at reduced speed. Set to 0 for normal operation.
D4	TMSEL	Termination Select. Driver Termination Select Bit. Set to 1 to force the driver output to the DTV_ voltage when RCV_ = 1 (term mode). Set to 0 to place the driver into high-impedance mode when RCV_ = 1 (high-Z). See Table 1.
D3	SC1	Driver Slew Rate Select. SC1 and SC0 set the driver slew rate. See Table 2.
D2	SC0	
D1	CDIFF	Differential Comparator Enable. Set to 1 to enable the differential comparators and disable the CH_ window comparators. Set to 0 to enable the CH_ window comparators and disable the differential comparators. See Tables 3a and 3b.
D0	LDDIS	Load Disable. Set LDDIS to 1 to disable the

Analog control input THR sets the threshold for the input logic, allowing operation with CMOS logic as low as 0.9V. Leaving THR unconnected results in a nominal threshold of 1.25V from an internal reference, providing compatibility with 2.5V to 3.3V logic.

Temperature Monitor

The MAX9975 supplies a temperature output signal, TEMP, that asserts a 3.33V nominal output voltage at a +70°C (343K) die temperature. The output voltage changes proportionally with temperature at 10mV/°C.

Heat Removal

Under normal circumstances, the MAX9975 requires heat removal through the exposed pad by use of an external heat sink. The exposed pad is electrically at V_{EE} potential, and must be either connected to V_{EE} or isolated.

Power dissipation is highly dependent upon the application. The *Electrical Characteristics* table indicates power dissipation under the condition that the source and sink currents are programmed to 0mA. Maximum dissipation occurs when the source and sink currents are both at 35mA, the $V_{DUT\_}$ is at an extreme of the voltage range, and the diode bridge is fully commutated. Under these conditions, the additional power dissipated (per channel) is:

If DUT_ is sourcing current:

$$P_D = (V_{DUT\_} - V_{EE}) \times I_{SOURCE}$$

If DUT_ is sinking current:

$$P_D = (V_{CC} - V_{DUT\_}) \times I_{SINK}$$

DUT_ sources the programmed (low) current when $V_{DUT\_} > V_{COM\_}$. The path of the current is from DUT_ through the outside of the diode bridge and the source (low) current source to V_{EE}. The programmed sink current is greatly reduced by the class AB load architecture.

DUT_ sinks the programmed (high) current when $V_{DUT\_} < V_{COM\_}$. The path of the current is from V_{CC} through the sink (high) current source and the outside of the diode bridge to DUT_. The programmed source current is greatly reduced by the Class AB architecture.

θ_{JC} of the exposed-pad package is very low, approximately 1°C/W to 2°C/W. Die temperature is thus highly dependent upon the heat removal techniques used in the application. Maximum total power dissipation occurs under conditions shown in Table 6.

Table 6. Maximum Power Dissipation Conditions

PARAMETER	MAX9975AR	MAX9975AZ
V_{CC}	+10.5V	+11V
V_{EE}	-5.25V	-4.75V
$I_{SOURCE} = I_{SINK}$	35mA	35mA
LOAD	Both Channels Enabled	Both Channels Enabled
$V_{DUT\_}$	-1.5V	-1V
$V_{COM\_}$	+0.5V	+0.5V

Under these extreme conditions, the total power dissipation is 4.3W typical and 4.8W maximum. If the die temperature cannot be maintained at an acceptable level under these conditions, use software clamping to limit the load output currents to lower values and/or reduce the supply voltages.

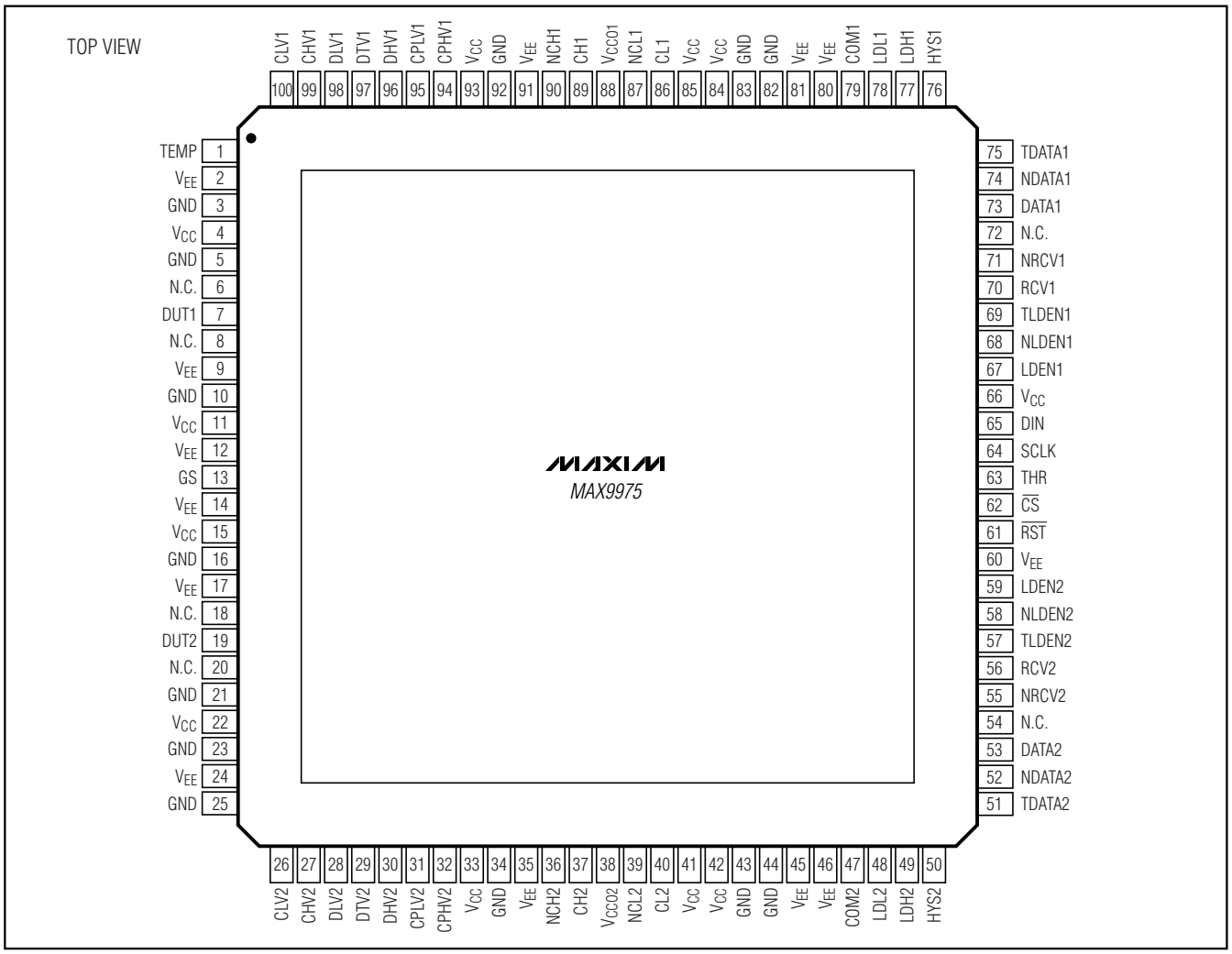
Power-Supply Considerations

Bypass all V_{CC} and V_{EE} power input pins with 0.01µF capacitors, and use bulk bypassing of at least 10µF on each supply.

Selector Guide

PART	ACCURACY GRADE	COMPARATOR OUTPUT TERMINATION	HIGH-SPEED DIGITAL INPUT TERMINATION (Ω)			HEAT EXTRACTION
			RCV_	DATA_	LDEN_	
MAX9969ADCCQ	A	None	None	None	None	Top
MAX9969AGCCQ	A	None	100	100	100	Top

Pin Configuration



Dual, Low-Power, 1200Mbps ATE Driver/Comparator with 35mA Load

Package Information

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