19-4078; Rev 0; 3/08

EVALUATION KIT AVAILABLE

20W Stereo Class D Speaker Amplifier with Volume Control

MAX9744

General Description

The MAX9744 20W stereo Class D audio power amplifier provides Class AB amplifier performance with Class D efficiency, conserving board space and eliminating the need for a bulky heatsink. This device features single-supply operation, adjustable gain, shutdown mode, a SYNC output, speaker mute, and industry-leading click-and-pop suppression.

The MAX9744 features a 64-step dual-mode (analog or digital), programmable volume control and mute function. The MAX9744 operates from a 4.5V to 14V single supply and can deliver up to 20W per channel into a 4Ω speaker with a 14V supply.

The MAX9744 offers two modulation schemes: a fixed-frequency modulation mode that allows one of several preset switching frequencies to be selected, and a spread-spectrum modulation mode that helps to reduce EMI-radiated emissions.

The MAX9744 features high 75dB PSRR, low 0.04% THD+N, and SNR in excess of 90dB. Robust short-circuit and thermal-overload protection prevent device damage during a fault condition. The MAX9744 is available in a 44-pin thin QFN-EP (7mm x 7mm x 0.8mm) package and is specified over the extended -40°C to +85°C temperature range.

Applications

Flat-Panel Televisions

PC Speaker Systems

Multimedia Docking Stations

Features

- **Wide 4.5V to 14V Power-Supply Voltage Range**
- **Filterless Spread-Spectrum Modulation Lowers Radiated RF Emissions from Speaker Cables**
- **20W Stereo Output (4Ω, V_{DD} = 12V, THD+N = 10%)**
- **Integrated Volume Control (I^2C or Analog)**
- **Low 0.04% THD+N**
- **High 75dB PSRR**
- **High 93% Efficiency**
- **Integrated Click-and-Pop Suppression**
- **Low-Power Shutdown Mode**
- **Short-Circuit and Thermal-Overload Protection**
- **Available in a 44-Pin Thin QFN-EP (7mm x 7mm x 0.8mm)**

Ordering Information

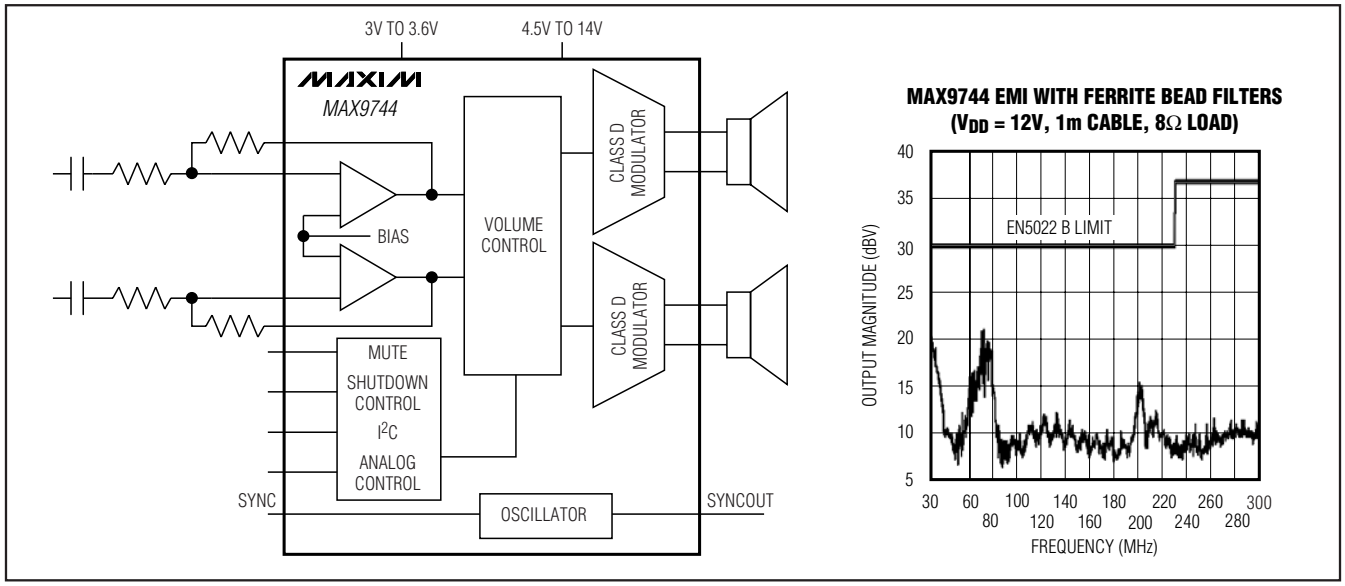
PART	TEMP RANGE	PIN-PACKAGE
MAX9744ETH+	-40°C to +85°C	44 TQFN-EP*

+Denotes a lead-free package.

**EP = Exposed pad.*

Pin Configuration appears at end of data sheet.

Simplified Block Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

20W Stereo Class D Speaker Amplifier with Volume Control

ABSOLUTE MAXIMUM RATINGS

PVDD to PGND .....+16V
V_{DD} to GND .....+4V
FB_, SYNCOUT, SYNC, SDA/VOL, ADDR1, ADDR2 to GND.....-0.3V to (V_{DD} + 0.3V)
BOOT_ to V_{DD} .....-0.3V to +6V
BOOT_ to OUT_.....-0.3V to +6V
OUT_ to GND .....-0.3V to (PVDD + 0.3V)
PGND to GND .....-0.3V to +0.3V
Any Other Pin to GND .....-0.3V to +4V
OUT_, Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)
44-Pin Thin QFN (derate 27mW/°C above +70°C, single-layer board).....2162mW
44-Pin Thin QFN (derate 37mW/°C above +70°C, multilayer board) 2963mW
θ_{JA}, Single-Layer Board.....37°C/W
θ_{JA}, Multilayer Board .....27°C/W
Continuous Input Current (PVDD, PGND).....6.4A
Continuous Output Current (OUT_) 3.2A
Continuous Input Current (except OUT_).....±20mA
Junction Temperature.....+150°C
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(PVDD = 12V, V_{DD} = 3.3V, GND = PGND = 0V, V_{MUTE} = 0V; max volume setting; all speaker load resistors connected between OUT_+ and OUT_-, R_L = ∞, unless otherwise stated, $C_{BOOT\_}$ = 0.1µF, C_{BIAS} = 2.2µF, C_{IN} = 0.47µF, R_{IN} = 20kΩ, $R_{F\_}$ = 20kΩ, spread-spectrum mode, filterless modulation mode, see the *Functional Diagrams/Typical Application Circuits.* T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL							
Speaker Amplifier Supply Voltage Range	PVDD	Inferred from PSRR test		4.5		14	V
Supply Voltage Range	V_{DD}	Inferred from PSRR test		2.7		3.6	V
Quiescent Current	I_{DD}				20	35	mA
	I_{PVDD}				10	20	
Shutdown Current	$I_{VDDSHDN}$				0.1	1	µA
	$I_{PVDDSHDN}$				0.1	1	
Turn-On Time	t_{ON}				200		ms
Common-Mode Bias Voltage	V_{BIAS}				1.5		V
Input Amplifier Output-Voltage Swing High	V_{OH}	Specified as V_{DD} – V_{OH}, R_L = 2kΩ connected to 1.5V			20		mV
Input Amplifier Output-Voltage Swing Low	V_{OL}	Specified as V_{OL} – GND, R_L = 2kΩ connected to 1.5V			20		mV
Input Amplifier Output Short-Circuit Current Limit					±60		mA
Input Amplifier Gain-Bandwidth Product	GBW				1.8		MHz
SPEAKER AMPLIFIERS							
Gain	A_{VMAX}	Maximum volume setting	Output stage gain		29.5		dB
			Total gain (Note 2)		29.5		
Output Offset	V_{OS}	T_A = 25°C			±2	±15	mV

ELECTRICAL CHARACTERISTICS (continued)

(PVDD = 12V, V_{DD} = 3.3V, GND = PGND = 0V, V_{MUTE} = 0V; max volume setting; all speaker load resistors connected between OUT_+ and OUT_-, R_L = ∞, unless otherwise stated, $C_{BOOT\_}$ = 0.1µF, C_{BIAS} = 2.2µF, C_{IN} = 0.47µF, R_{IN} = 20kΩ, $R_{F\_}$ = 20kΩ, spread-spectrum mode, filterless modulation mode, see the *Functional Diagrams/Typical Application Circuits*. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Efficiency (Note 3)	η	Filterless modulation	P_{OUT} = 10W, f_{IN} = 1kHz, 8Ω load		93		%
			P_{OUT} = 15W, f_{IN} = 1kHz, 4Ω load		87		
		PWM	P_{OUT} = 10W, f_{IN} = 1kHz, 8Ω load		92		%
			P_{OUT} = 15W, f_{IN} = 1kHz, 4Ω load		88		
Output Power	P_{OUT}	V_{PVDD} = 5V, f_{IN} = 1kHz	R_L = 8Ω, THD+N = 1%		1.4		W
			R_L = 8Ω, THD+N = 10%		1.8		
			R_L = 4Ω, THD+N = 1%		2.6		
			R_L = 4Ω, THD+N = 10%		3.6		
		V_{PVDD} = 12V, f_{IN} = 1kHz	R_L = 8Ω, THD+N = 1%		8		
			R_L = 8Ω, THD+N = 10%		10		
			R_L = 4Ω, THD+N = 1%		14		
			R_L = 4Ω, THD+N = 10%		17		
		V_{PVDD} = 14V, f_{IN} = 1kHz	R_L = 8Ω, THD+N = 1%		10		
			R_L = 8Ω, THD+N = 10%		13		
			R_L = 4Ω, THD+N = 1%		17.5		
			R_L = 4Ω, THD+N = 10%		22.5		
Hard Output Current Limit	I_{SC}			3.9	5.5		A
Total Harmonic Distortion Plus Noise	THD+N	f = 1kHz, R_L = 8Ω, P_{OUT} = 5W, f_{IN} = 1kHz	Filterless modulation		0.04		%
			PWM		0.04		
Signal-to-Noise Ratio	SNR	P_{OUT} = 10W, R_L = 8Ω, filterless modulation mode, BW = 22Hz to 22kHz	Fixed-frequency modulation, unweighted		91		dB
			Spread-spectrum, unweighted		90		
			Fixed-frequency modulation, A-weighted		94		
			Spread-spectrum, A-weighted		94		
		P_{OUT} = 10W, R_L = 8Ω, PWM mode, BW = 22Hz to 22kHz	Fixed-frequency modulation, unweighted		91		dB
			Spread-spectrum, unweighted		81		
			Fixed-frequency modulation, A-weighted		94		
			Spread-spectrum, A-weighted		89		

20W Stereo Class D Speaker Amplifier with Volume Control

ELECTRICAL CHARACTERISTICS (continued)

(PVDD = 12V, V_{DD} = 3.3V, GND = PGND = 0V, V_{MUTE} = 0V; max volume setting; all speaker load resistors connected between OUT_+ and OUT_-, R_L = ∞, unless otherwise stated, $C_{BOOT\_}$ = 0.1µF, C_{BIAS} = 2.2µF, C_{IN} = 0.47µF, R_{IN} = 20kΩ, $R_{F\_}$ = 20kΩ, spread-spectrum mode, filterless modulation mode, see the *Functional Diagrams/Typical Application Circuits*. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Crosstalk		1kHz			85		dB
		20Hz to 20kHz			68		
Power-Supply Rejection Ratio	PSRR	V_{DD} = 2.7V to 3.6V, T_A = 25°C, MUTE = high			68		dB
		PV_{DD} = 4.5V to 14V		50	83		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P} on V_{DD}			70		
		f = 1kHz, V_{RIPPLE} = 200mV_{P-P} on PVDD			75		
SYNC Frequency	f_{SYNC}	SYNC = GND		1020	1200	1355	kHz
		SYNC = unconnected		1280	1440	1640	
		SYNC = V_{DD} (spread-spectrum mode)			1200 ±30		
Class D Switching Frequency	f_{SW}	SYNC = GND		255	300	338	kHz
		SYNC = unconnected		320	360	410	
		SYNC = V_{DD} (spread-spectrum mode)			300 ±6		
SYNC Frequency Lock Range				1000		1600	kHz
Minimum SYNC Frequency Lock Duty Cycle					40		%
Maximum SYNC Frequency Lock Duty Cycle					60		%
Gain Matching		Full volume (ideal matching for R_{IN} and R_F)			0.2		dB
Click-and-Pop Level	K_{CP}	Peak voltage, 32 samples/second, A-weighted (Note 4)	Into shutdown		-43		dBV
			Out of shutdown		-43		
			Into mute		-46		
			Out of mute		-57		
VOLUME CONTROL							
VOL Input Leakage Current					±5		µA
Input Hysteresis		DC volume control mode			11		mV
9.5dB Gain Voltage		DC volume control mode			0.1 x V_{DD}		V
Full Mute Voltage		DC volume control mode			0.9 x V_{DD}		V
Full Mute Attenuation		f = 1kHz, relative to 9.5dB setting			-115		dB
DIGITAL INPUTS/OUTPUT ($\overline{SHDN}$, MUTE, ADDR1, ADDR2, SCLK, SDA/VOL)							
Input-Voltage High	V_{IH}			0.7 x V_{DD}			V
Input-Voltage Low	V_{IL}					0.3 x V_{DD}	V
Input Leakage Current	I_{LK}					±1	µA
Input Hysteresis		SCLK, SDA/VOL			0.1 x V_{DD}		V
Input Capacitance	C_{IN}				5		pF
Output-Voltage Low	V_{IL}	I_{OL} = 3mA				0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(PVDD = 12V, V_{DD} = 3.3V, GND = PGND = 0V, V_{MUTE} = 0V; max volume setting; all speaker load resistors connected between OUT_+ and OUT_-, R_L = ∞, unless otherwise stated, $C_{BOOT\_}$ = 0.1µF, C_{BIAS} = 2.2µF, C_{IN} = 0.47µF, R_{IN} = 20kΩ, $R_{F\_}$ = 20kΩ, spread-spectrum mode, filterless modulation mode, see the *Functional Diagrams/Typical Application Circuits*. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUT (SYNC)						
Input-Voltage High	V_{SYNCIH}		2.3			V
Input-Voltage Low	V_{SYNCIL}				0.8	V
SYNC Input Leakage	I_{SYNCIN}		±7.5		±13	µA
DIGITAL OUTPUT (SYNCOUT)						
Output-Voltage High	$V_{SYNCOUTIH}$	I_{SOURCE} = 1mA	V_{DD} - 0.3			V
Output-Voltage Low	$V_{SYNCOUTIL}$	I_{SINK} = 1mA			0.3	V
Rise/Fall Time		C_L = 10pF		50		V/µs
THERMAL PROTECTION						
Thermal-Shutdown Threshold				+165		°C
Thermal-Shutdown Hysteresis				15		°C
I^2C TIMING CHARACTERISTICS (Figure 3)						
Serial Clock	f_{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD, STA}$	(Note 5)	0.6			µs
Repeated START Condition Setup Time	$t_{SU, STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU, STO}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		0.9	µs
Data Setup Time	$t_{SU,DAT}$		100			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.6			µs
Rise Time of SDA and SCL, Receiving	t_R	(Note 6)	20 + 0.1C_B		300	ns
Fall Time of SDA and SCL, Receiving	t_F	(Note 6)	20 + 0.1C_B		300	ns
Pulse Width of Spike Suppressed	t_{SP}		0		50	ns
Capacitive Load for Each Bus Line	C_B				400	pF

Note 1: All devices are 100% production tested at +25°C. All temperature limits are guaranteed by design.

Note 2: See the *Gain-Setting Resistors* section.

Note 3: Measured on the MAX9744 Evaluation Kit.

Note 4: Testing performed with an 8Ω resistive load connected across BTL output. Mode transitions are controlled by $\overline{SHDN}$ or MUTE pin, respectively.

Note 5: A master device must provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the SCL's falling edge.

Note 6: C_B = total capacitance of one bus line in pF.

20W Stereo Class D Speaker Amplifier with Volume Control

Typical Operating Characteristics

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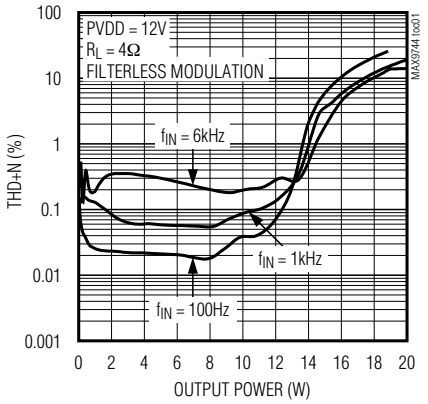
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



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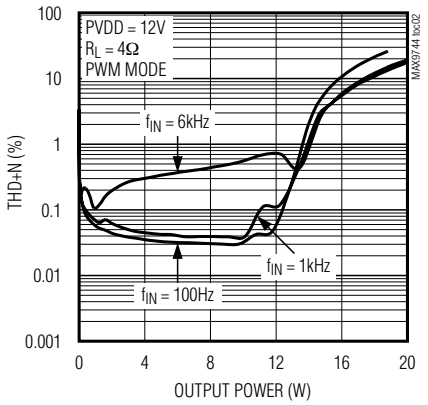

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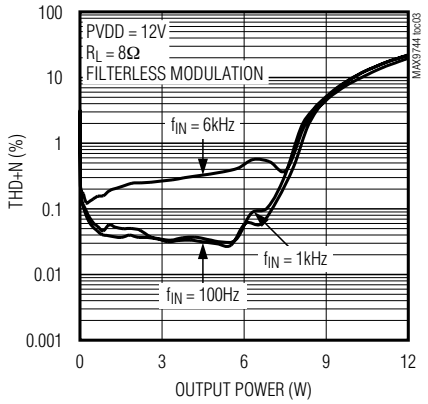

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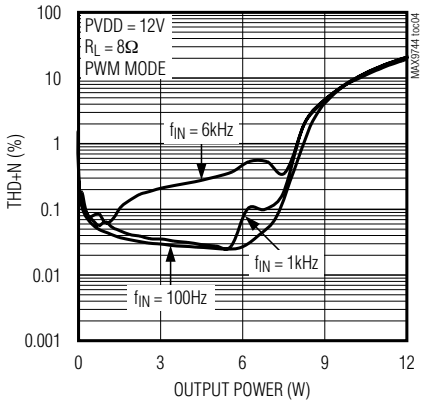

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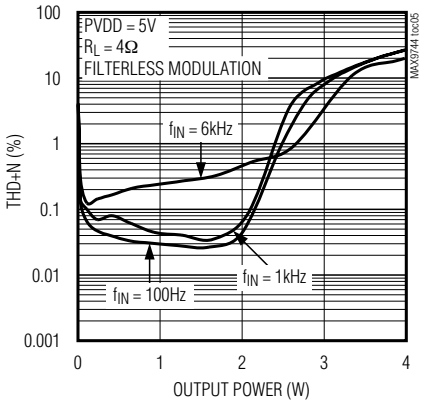

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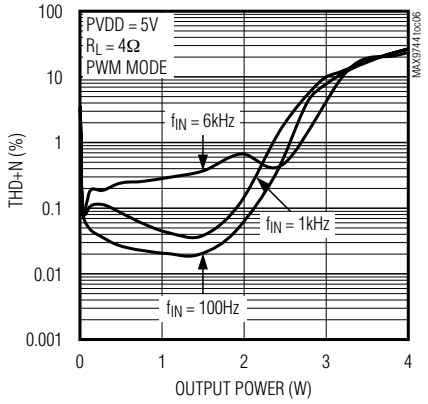

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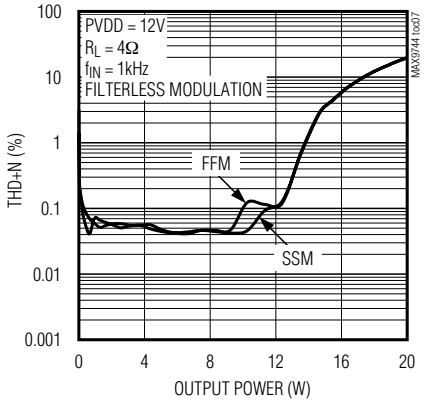

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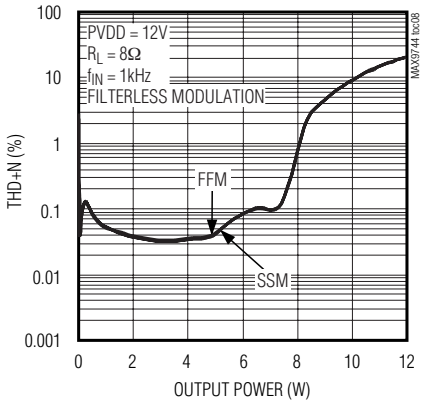

Typical Operating Characteristics (continued)

(V_{PVDD} = 12V, V_{DD} = 3.3V, V_{GND} = V_{PGND} = 0V, V_{MUTE} = 0V; max volume setting; all speaker load resistors connected between OUT_+ and OUT_- with an inductor in series, 8Ω load, L = 68µH, 4Ω load, L= 33µH. R_L = ∞, unless otherwise stated, C_{BIAS} = 2.2µF, C_{IN} = 0.47µF, R_{IN} = 20kΩ, $R_{F\_}$ = 20kΩ, spread-spectrum mode, T_A = +25°C, unless otherwise noted.)

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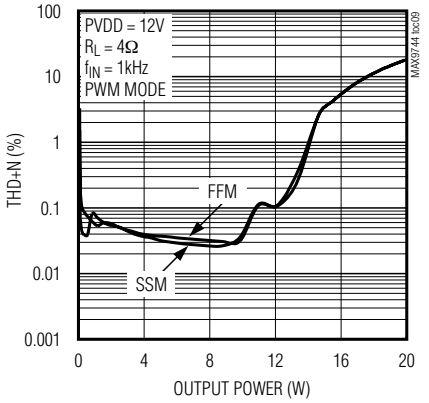
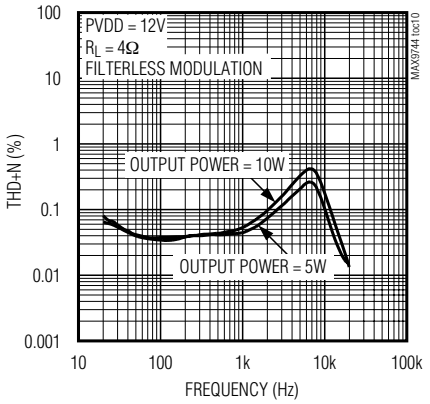


TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



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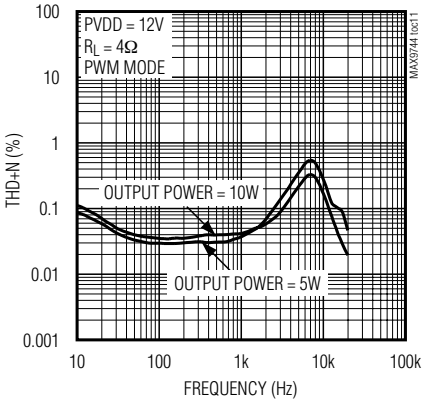

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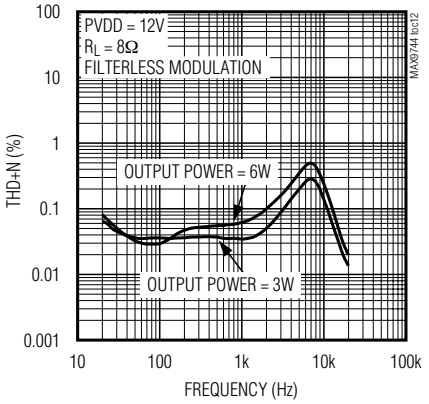

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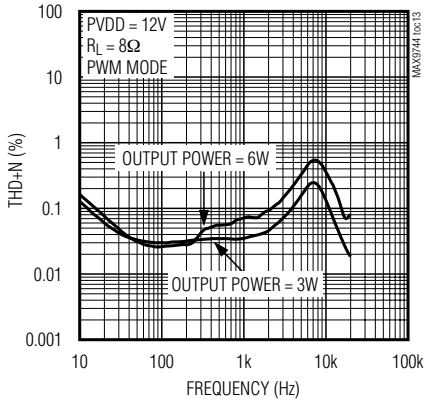

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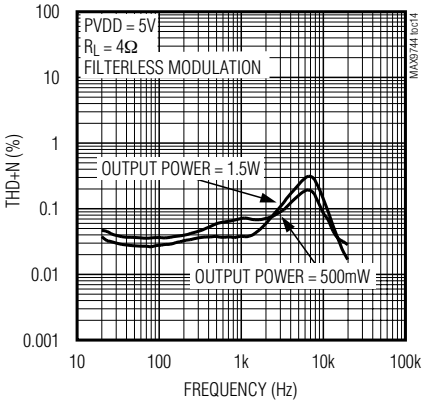

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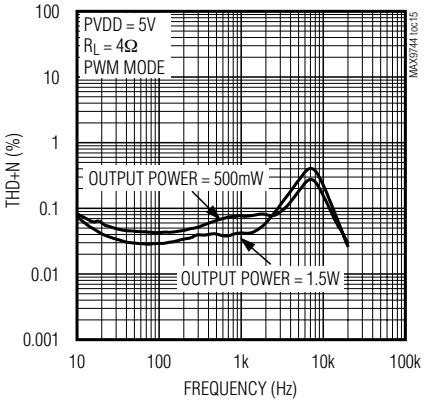

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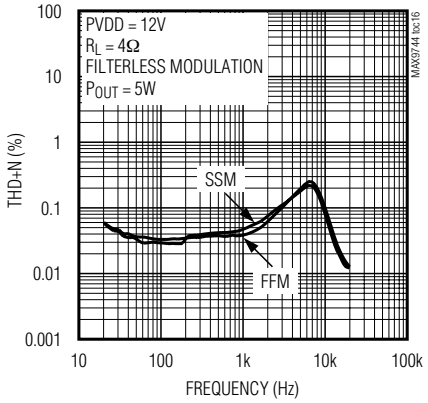

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Typical Operating Characteristics (continued)

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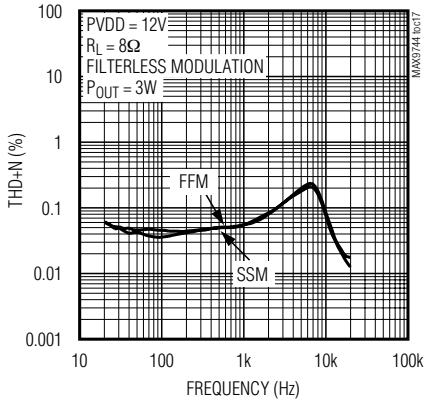
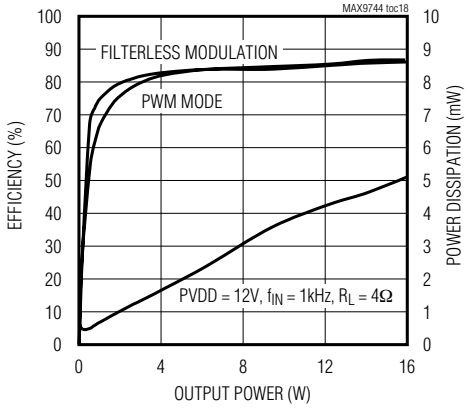
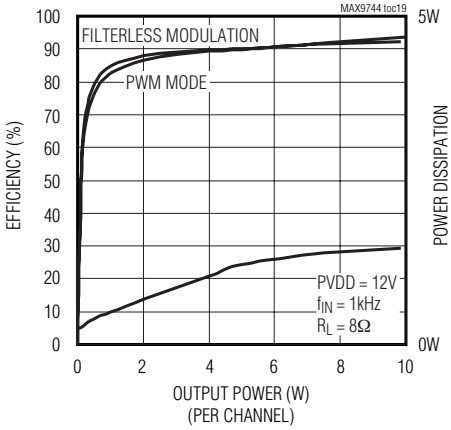


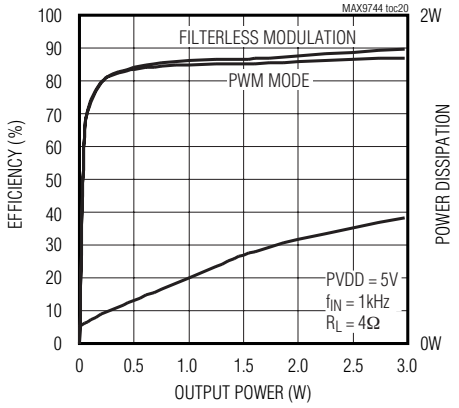
EFFICIENCY vs. OUTPUT POWER



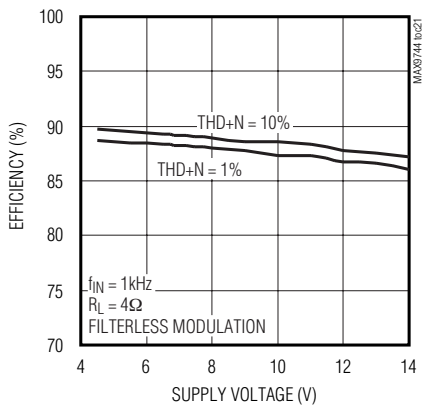
EFFICIENCY vs. OUTPUT POWER



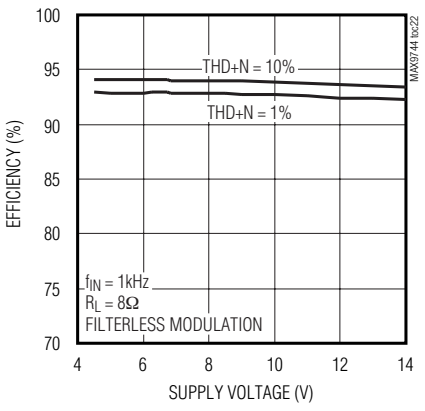
EFFICIENCY vs. OUTPUT POWER



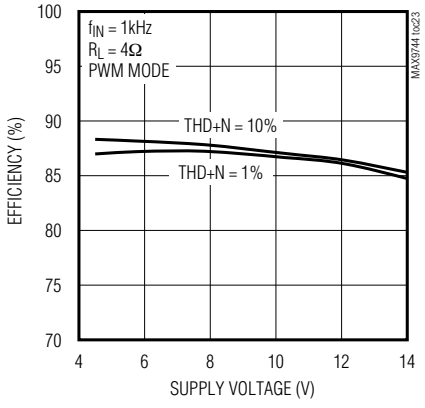
EFFICIENCY vs. SUPPLY VOLTAGE



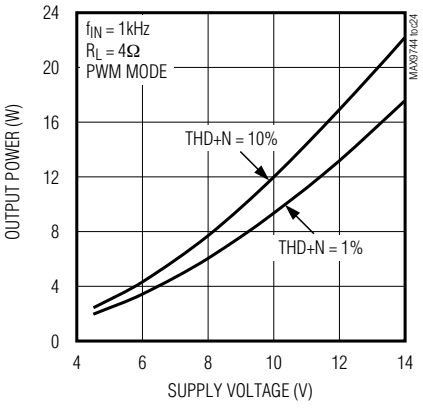
EFFICIENCY vs. SUPPLY VOLTAGE



EFFICIENCY vs. SUPPLY VOLTAGE



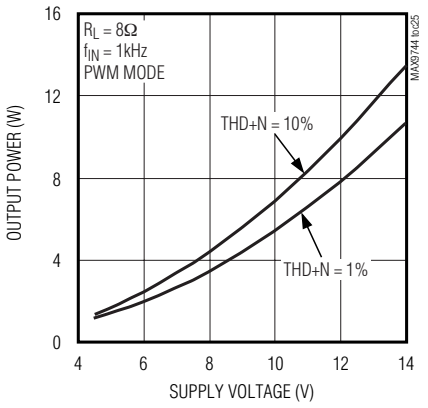
OUTPUT POWER vs. SUPPLY VOLTAGE



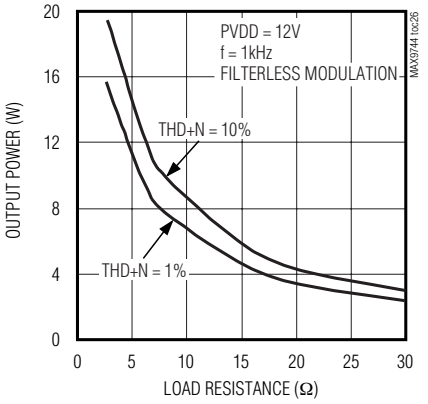
Typical Operating Characteristics (continued)

(V_{PVDD} = 12V, V_{DD} = 3.3V, V_{GND} = V_{PGND} = 0V, V_{MUTE} = 0V; max volume setting; all speaker load resistors connected between OUT_+ and OUT_- with an inductor in series, 8Ω load, L = 68µH, 4Ω load, L= 33µH. R_L = ∞, unless otherwise stated, C_{BIAS} = 2.2µF, C_{IN} = 0.47µF, R_{IN} = 20kΩ, $R_{F\_}$ = 20kΩ, spread-spectrum mode, T_A = +25°C, unless otherwise noted.)

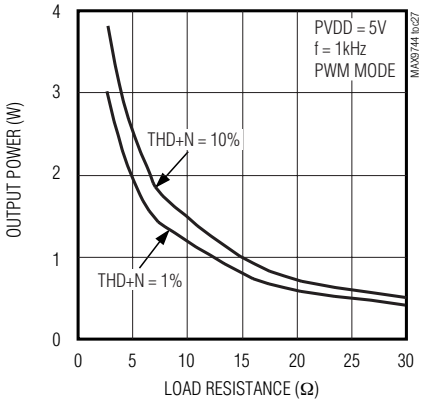
OUTPUT POWER vs. SUPPLY VOLTAGE



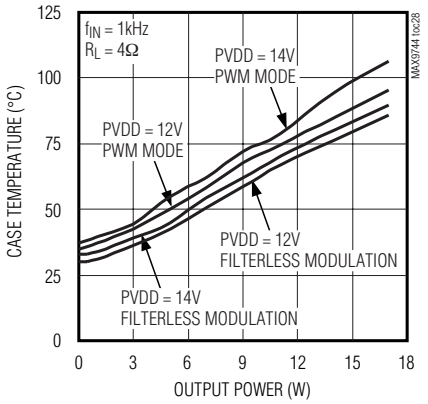
OUTPUT POWER vs. LOAD RESISTANCE



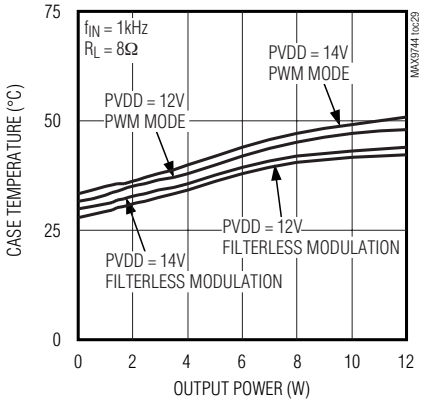
OUTPUT POWER vs. LOAD RESISTANCE



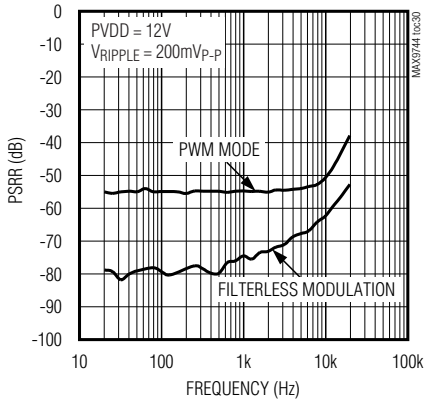
CASE TEMPERATURE vs. OUTPUT POWER



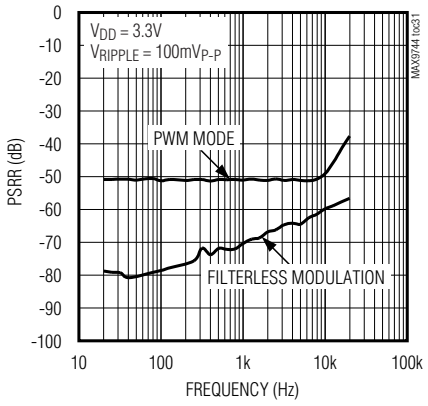
CASE TEMPERATURE vs. OUTPUT POWER



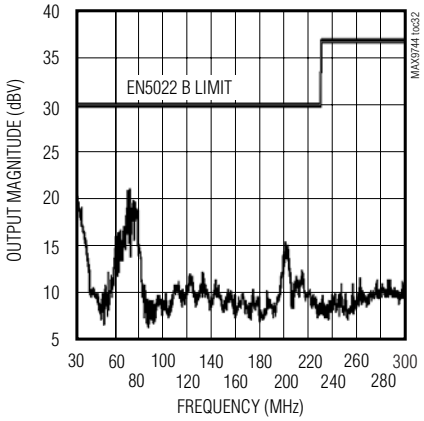
POWER-SUPPLY REJECTION RATIO (PVDD) vs. FREQUENCY



POWER-SUPPLY REJECTION RATIO (V_{DD}) vs. FREQUENCY



EMI WITH FERRITE BEAD FILTERS (V_{DD} = 12V, 1m CABLE, 8Ω LOAD)

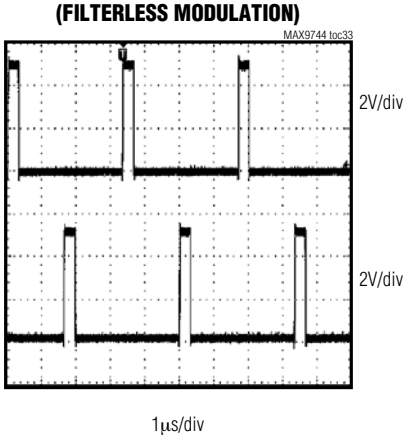


20W Stereo Class D Speaker Amplifier with Volume Control

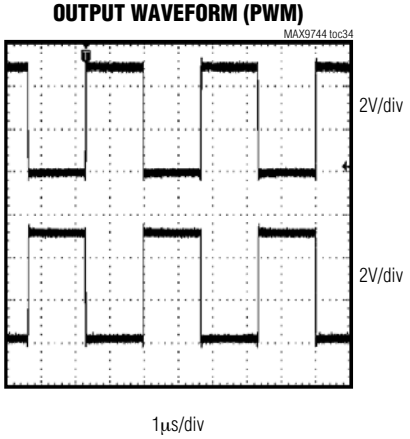
Typical Operating Characteristics (continued)

(V_{PVDD} = 12V, V_{DD} = 3.3V, V_{GND} = V_{PGND} = 0V, V_{MUTE} = 0V; max volume setting; all speaker load resistors connected between OUT_+ and OUT_- with an inductor in series, 8Ω load, L = 68µH, 4Ω load, L= 33µH. R_L = ∞, unless otherwise stated, C_{BIAS} = 2.2µF, C_{IN} = 0.47µF, R_{IN} = 20kΩ, $R_{F\_}$ = 20kΩ, spread-spectrum mode, T_A = +25°C, unless otherwise noted.)

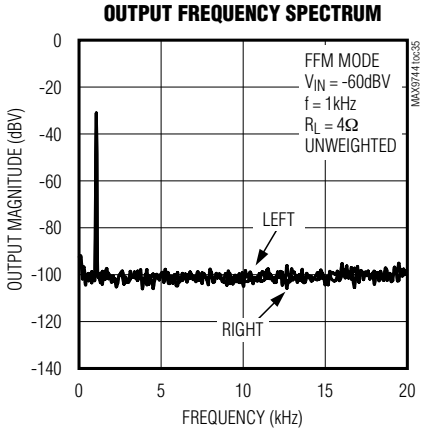
OUTPUT WAVEFORM (FILTERLESS MODULATION)



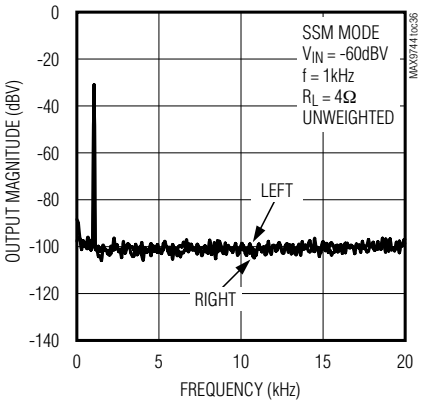
OUTPUT WAVEFORM (PWM)



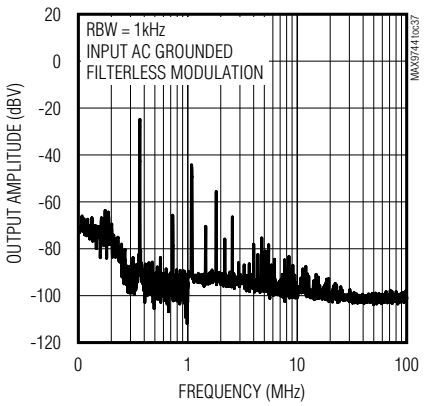
OUTPUT FREQUENCY SPECTRUM



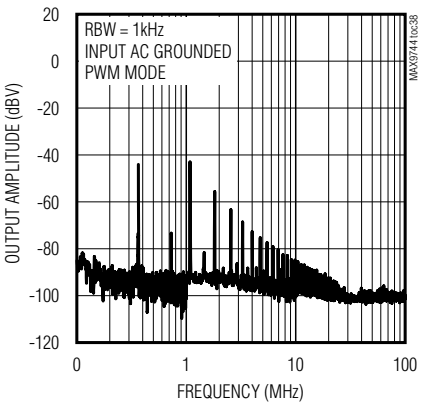
OUTPUT FREQUENCY SPECTRUM



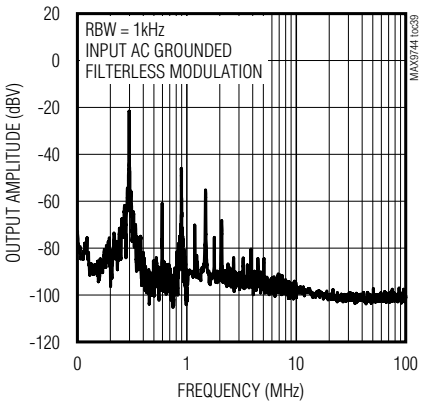
WIDEBAND OUTPUT SPECTRUM (FIXED-FREQUENCY MODULATION MODE)



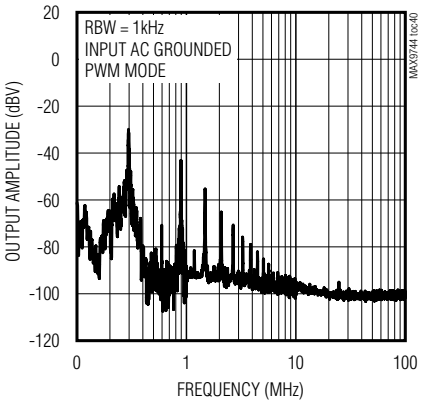
WIDEBAND OUTPUT SPECTRUM (FIXED-FREQUENCY MODULATION MODE)



WIDEBAND OUTPUT SPECTRUM (SPREAD-SPECTRUM MODULATION MODE)



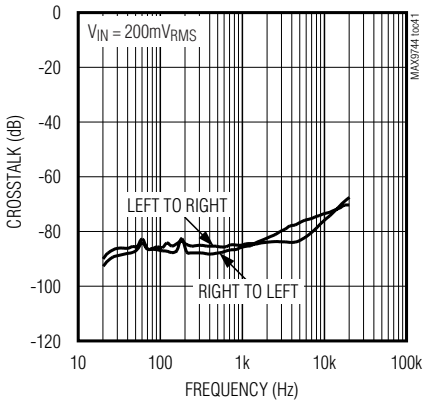
WIDEBAND OUTPUT SPECTRUM (SPREAD-SPECTRUM MODULATION MODE)



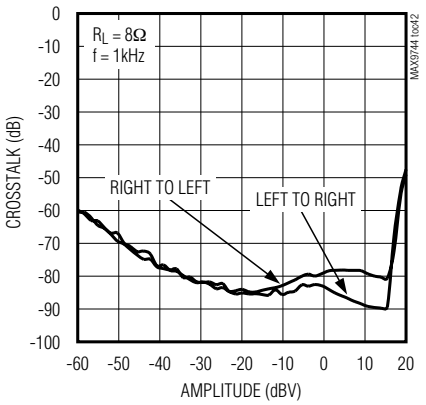
Typical Operating Characteristics (continued)

(V_{PVDD} = 12V, V_{DD} = 3.3V, V_{GND} = V_{PGND} = 0V, V_{MUTE} = 0V; max volume setting; all speaker load resistors connected between OUT_+ and OUT_- with an inductor in series, 8Ω load, L = 68µH, 4Ω load, L= 33µH. R_L = ∞, unless otherwise stated, C_{BIAS} = 2.2µF, C_{IN} = 0.47µF, R_{IN} = 20kΩ, $R_{F\_}$ = 20kΩ, spread-spectrum mode, T_A = +25°C, unless otherwise noted.)

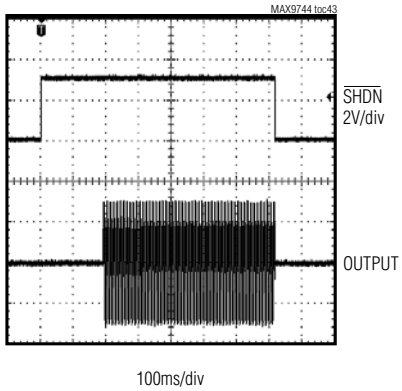
CROSSTALK vs. FREQUENCY



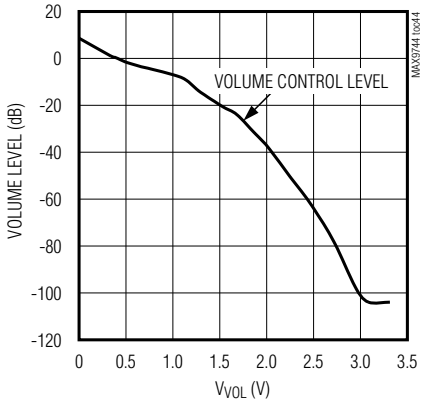
CROSSTALK vs. AMPLITUDE



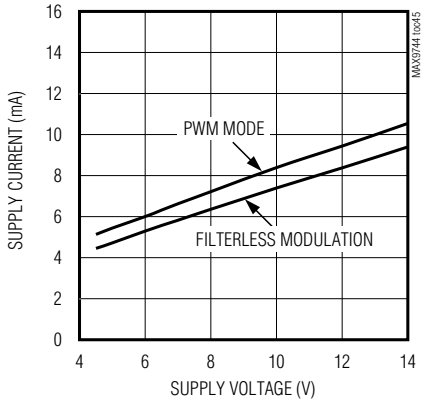
TURN-ON/OFF RESPONSE



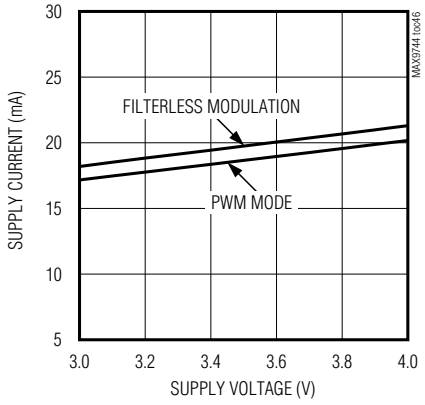
VOLUME CONTROL LEVEL vs. VOLUME CONTROL VOLTAGE



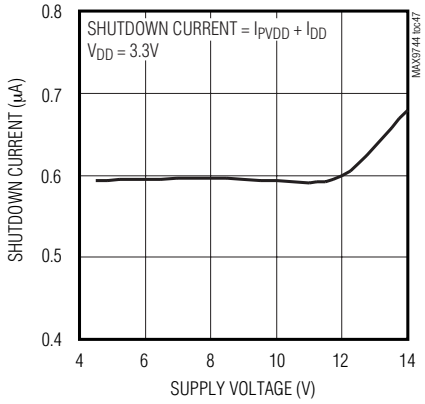
SUPPLY CURRENT (PVDD) vs. SUPPLY VOLTAGE



SUPPLY CURRENT (V_{DD}) vs. SUPPLY VOLTAGE



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



20W Stereo Class D Speaker Amplifier with Volume Control

Pin Description

PIN	NAME	FUNCTION
1	BOOTL+	Left-Channel Positive Speaker Output Boost Flying-Capacitor Connection. Connect a 0.1µF ceramic capacitor between BOOTL+ and OUTL+.
2, 3	OUTL+	Left-Channel Speaker Output, Positive Phase
4, 5, 29, 30	PVDD	Speaker Amplifier Power-Supply Input. Bypass each with a 1µF capacitor to PGND.
6, 10, 21, 28	V_{DD}	Power-Supply Input. Bypass each with a 1µF capacitor to GND.
7, 11, 12, 15, 27	GND	Ground
8	SDA/VOL	I^2C Serial Data I/O and Analog Volume Control Input
9	SCLK/PWM	I^2C Serial Clock Input and Modulation Scheme Select. In I^2C mode (ADDR1 and ADDR2 ≠ GND), acts as I^2C serial clock input. When ADDR1 and ADDR2 = GND, set SCLK = 1 for standard PWM output scheme, or set SCLK = 0 for filterless modulation output scheme.
13	ADDR1	Address Select Input 1. Sets device address for I^2C address option. Connect ADDR1 and ADDR2 to GND to select analog volume control mode.
14	ADDR2	Address Select Input 2. Sets device address for I^2C address option. Connect ADDR1 and ADDR2 to GND to select Analog Volume Control mode.
16	INL	Left-Channel Audio Input
17	FBL	Left-Channel Feedback. Connect feedback resistor between FBL and INL to set amplifier gain. See the *Gain-Setting Resistors* section.
18	FBR	Right-Channel Feedback. Connect feedback resistor between FBR and INR to set amplifier gain. See the *Gain-Setting Resistors* section.
19	INR	Right-Channel Input
20	BIAS	Common-Mode Bias Voltage. Bypass with a 2.2µF capacitor to GND.
22	$\overline{SHDN}$	Shutdown Input. Drive $\overline{SHDN}$ low to disable the audio amplifiers. Connect $\overline{SHDN}$ to V_{DD} or drive high for normal operation.
23	N.C.	No Connection. Not internally connected.
24	MUTE	Mute Input. Drive MUTE high to mute the speaker outputs. Connect MUTE to GND for normal operation (mute function controls speaker outputs only).
25	SYNC	Frequency Select and External Clock Input. SYNC = GND: Fixed-frequency mode with f_{SYNC} = 1200kHz SYNC = Unconnected: Fixed-frequency mode with f_{SYNC} = 1440kHz SYNC = V_{DD}: Spread-spectrum mode with f_{SYNC} = 1200kHz ±30kHz SYNC = Clocked: Fixed-frequency mode with f_{SYNC} = external clock frequency. f_{SW} = 1/4 the value of f_{SYNC}.

Pin Description (continued)

PIN	NAME	FUNCTION
26	SYNCOUT	SYNC Signal Output
31, 32	OUTR+	Right-Channel Positive Speaker Output
33	BOOTR+	Right-Channel Positive Speaker Output Boost Flying-Capacitor Connection. Connect a 0.1µF ceramic capacitor between BOOTR+ and OUTR+.
34, 35, 39, 43, 44	PGND	Power Ground
36, 37	OUTR-	Right-Channel Negative Speaker Output
38	BOOTR-	Right-Channel Negative Speaker Output Boost Flying-Capacitor Connection. Connect a 0.1µF ceramic capacitor between BOOTR- and OUTR-.
40	BOOTL-	Left-Channel Negative Speaker Output Boost Flying-Capacitor Connection. Connect a 0.1µF ceramic capacitor between BOOTL- and OUTL-.
41, 42	OUTL-	Left-Channel Negative Speaker Output
—	EP	Exposed Pad. The external pad lowers the package's thermal impedance by providing a direct heat conduction path from the die to the PCB. Connect the exposed thermal pad to PGND.

Detailed Description

The MAX9744 20W filterless, stereo Class D audio power amplifier offers Class AB performance with Class D efficiency with a minimal board space solution. The MAX9744 features a spread-spectrum modulation scheme offering significant improvements to switch-mode amplifier technology. This device features analog or digitally adjustable volume control, externally set input gain, shutdown mode, SYNC input and output, mute, and industry-leading click-and-pop suppression.

The MAX9744 features extensive click-and-pop suppression circuitry that eliminates audible clicks-and-pops at startup and shutdown.

The MAX9744 features a 64-step, dual-mode (analog or I^2C) volume control and mute function. In analog volume control mode, the voltage applied to SDA/VOL sets the volume level. Two address inputs (ADDR1, ADDR2) set the volume control function between analog and I^2C mode and set the slave address. In I^2C mode, there are three selectable slave addresses allowing for multiple devices on a single bus.

The MAX9744 offers spread-spectrum and fixed-frequency modes of operation with classic PWM or filterless modulation output schemes. The filterless modulation scheme uses minimum pulse outputs when the audio inputs are at the zero crossing. As the input voltage increases or decreases, the duration of the pulse at one output increases while the other output pulse duration remains the same. This causes the net voltage across the speaker (V_{OUT+} - V_{OUT-}) to change. The minimum-width pulse topology reduces EMI and increases efficiency.

Operating Modes

Fixed-Frequency Modulation Mode

The MAX9744 features two fixed-frequency modes: 300kHz and 360kHz. Connect SYNC to GND to select 300kHz switching frequency; leave SYNC unconnected to select the 360kHz switching frequency. The MAX9744 frequency spectrum consists of the fundamental switching frequency and its associated harmonics (see the Wideband Output Spectrum graphs in the *Typical Operating Characteristics*). For applications where exact spectrum placement of the switching fundamental is important, program the switching frequency so that the harmonics do not fall within a sensitive frequency band (Table 1). Audio reproduction is not affected by changing the switching frequency.

20W Stereo Class D Speaker Amplifier with Volume Control

Spread-Spectrum Modulation Mode

The MAX9744 features a unique, patented spread-spectrum mode that flattens the wideband spectral components, improving EMI emissions that may be radiated by the speaker and cables. This mode is enabled by setting SYNC = V_{DD} (Table 1). In spread-spectrum mode, the switching frequency varies randomly by ±7.5kHz around the center frequency (300kHz). The modulation scheme remains the same, but the period of the triangle waveform changes from cycle to cycle. Instead of a large amount of spectral energy present at multiples of the switching frequency, the energy is now spread over a bandwidth that increases with frequency. Above a few megahertz, the wideband spectrum looks like white noise for EMI purposes. A proprietary amplifier topology ensures this does not corrupt the noise floor in the audio bandwidth.

External Clock Mode

The SYNC input allows the MAX9744 to be synchronized to an external clock or another Maxim Class D amplifier, creating a fully synchronous system. This minimizes clock intermodulation and allocates spectral components of the switching harmonics to insensitive frequency bands. Applying a clock signal between 1MHz and 1.6MHz to SYNC synchronizes the MAX9744. The MAX9744 Class D amplifier operates at 1/4 of the SYNC frequency. For example, if SYNC is 1.6MHz, the Class D amplifier operates at 400kHz.

The external SYNC signal can be any CMOS clock source with a 40% to 60% duty cycle. Spread-spectrum clocks work well to reduce EMI; therefore, the SYNCOUT signal from another MAX9744 in spread-spectrum mode is an excellent SYNC input.

Table 1. Operating Modes

SYNC	MODE	f_{SYNC} (kHz)	f_{SW} (kHz)
GND	Fixed-frequency modulation	1200	300
Unconnected	Fixed-frequency modulation	1440	360
V_{DD}	Spread-spectrum modulation	1200 ±30	300 ±7.5
Clocked	EXT	1000 to 1600	250 to 400

SYNCOUT allows several Maxim amplifiers to be cascaded (Figure 1). The synchronized output minimizes interference due to clock intermodulation caused by the switching spread between single devices. Using SYNCOUT and SYNC does not affect the audio performance of the MAX9744.

Filterless Modulation/PWM Modulation

The MAX9744 features two output modulation schemes: filterless modulation or classic PWM. The MAX9744 output modulation schemes are selectable through SCLK/PWM when the device is in analog mode (ADDR1 and ADDR2 = GND, Table 2) or through the I^2C interface (Table 8). Maxim's unique, filterless modulation scheme eliminates the LC filter required by traditional Class D amplifiers, reducing component count and conserving board space and system cost. Although the MAX9744 meets FCC and other EMI limits with a low-cost ferrite bead filter, many applications still may want to use a full LC-filtered output. If using a full LC filter, audio performance is best with the MAX9744 configured for classic PWM output.

Switching between schemes, the output is not click-and-pop protected. To have click-and-pop protection when switching between output schemes, the device must enter shutdown mode and be configured to the new output scheme before the startup sequence is finished.

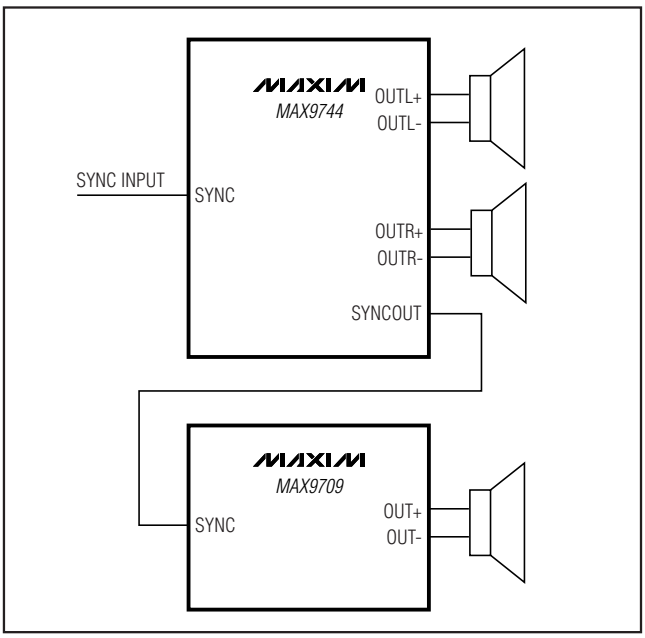


Figure 1. Cascading Two Amplifiers' External Clock Mode

Table 2. Modulation Scheme Selection

ADDR2	ADDR1	SDA/VOL	SCLK/PWM	FUNCTION
0	0	Analog volume control	0	Filterless modulation
0	0	Analog volume control	1	Classic PWM (50% duty cycle)

Efficiency

The high efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. In a Class D amplifier, the output transistors act as current-steering switches and consume negligible additional power. Any power loss associated with the Class D output stage is mostly due to the I^2R loss of the MOSFET on-resistance, and quiescent current overhead.

The theoretical best efficiency of a linear amplifier is 78% at peak output power. Under normal operating levels (typical music reproduction levels), the efficiency falls below 30%, whereas the MAX9744 exhibits > 80% efficiency under the same conditions (Figure 2).

Current Limit

When the output current exceeds the current limit, 5.5A (typ), the MAX9744 disables the outputs and initiates a 220µs startup sequence. The shutdown and startup sequence is repeated until the output fault is removed. Since the retry repetition is slow, the average supply current is low. Most applications do not enter current-limit mode unless the output is short circuited or incorrectly connected.

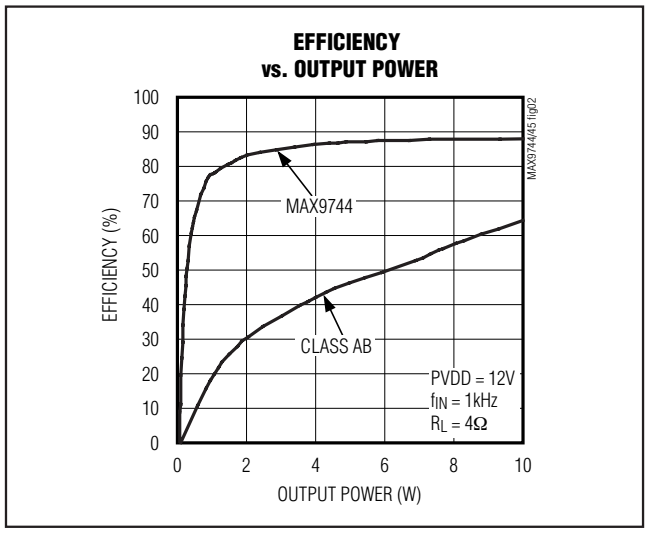


Figure 2. MAX9744 Efficiency vs. Class AB Efficiency

Thermal Shutdown

When the die temperature exceeds the thermal-shutdown threshold, +165°C (typ), the MAX9744 outputs are disabled. Normal operation resumes when the die temperature decreases by a factor equal to the thermal-shutdown threshold minus the thermal-shutdown hysteresis, (typically below +150°C). The effect of thermal shutdown is an output signal turning off for approximately 3s in most applications, depending on the thermal time constant of the audio system. Most applications should never enter thermal shutdown. Some of the possible causes of thermal shutdown are too low of a load impedance, bad thermal contact between the MAX9744's exposed pad and PCB, high ambient temperature, poor PCB layout and assembly, or excessive output overdrive.

Shutdown

The MAX9744 features a shutdown mode that reduces power consumption and extends battery life. Driving $\overline{SHDN}$ low places the device in low-power shutdown mode. Connect $\overline{SHDN}$ to digital high for normal operation. In shutdown mode, the outputs are high impedance, SYNCOUT is pulled high, BIAS voltage decays to zero, and the common-mode input voltage decays to zero. The I^2C register does not retain its contents during shutdown (MAX9744).

Mute Function

The MAX9744 features a clickless-and-popless mute mode. When the device is muted, the outputs do not stop switching; only the volume level is muted to the speaker. Mute only affects the output stage and does not shut down the device. To mute the MAX9744, drive MUTE to logic-high. MUTE should be held high during system power-up and power-down to ensure that pops caused by circuits before the MAX9744 are eliminated. To reduce clicks and pops, the device enters or exits mute at zero crossing.

20W Stereo Class D Speaker Amplifier with Volume Control

Volume Control

For maximum flexibility, the MAX9744 features volume control operation using an analog voltage input or through the I²C interface. To set the device to analog mode, connect ADDR1 and ADDR2 to GND. In analog mode, SDA/VOL is an analog input for volume control. The analog input range is ratiometric between 0.9 x V_{DD} and 0.1 x V_{DD} where 0.9 x V_{DD} = full mute and 0.1 x V_{DD} = full volume (Table 7).

Use ADDR1 and ADDR2 to select I²C mode. There are three addresses that can be chosen, allowing for multiple devices on a single bus (Table 4). In I²C mode, volume is controlled by choosing the speaker volume control register in the command byte (Table 5). There are 64 volume settings, where the lowest setting is full mute (Table 6). See the *Write Byte* section for more information on formatting data and tables to set volume levels. The default volume after power-up is position 40 (-7.1dB) (see Table 7).

I²C Interface

The MAX9744 features an I²C 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX9744 and the master at clock rates up to 400kHz. Figure 3 shows the 2-wire interface timing diagram. The MAX9744 is a receive-only slave device, relying on the master to generate the SCL signal. The MAX9744 cannot write to the SDA bus except to acknowledge the receipt of data from the master. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus.

A master device communicates to the MAX9744 by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or Repeated START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The MAX9744 SDA line operates as both an input and an open-drain output. A pullup resistor, greater than 500Ω, is required on the SDA bus. The MAX9744 SCL line operates as an input only. A pullup resistor, greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs have Schmitt trigger and filter circuits that suppress noise spikes to assure proper device operation even on a noisy bus.

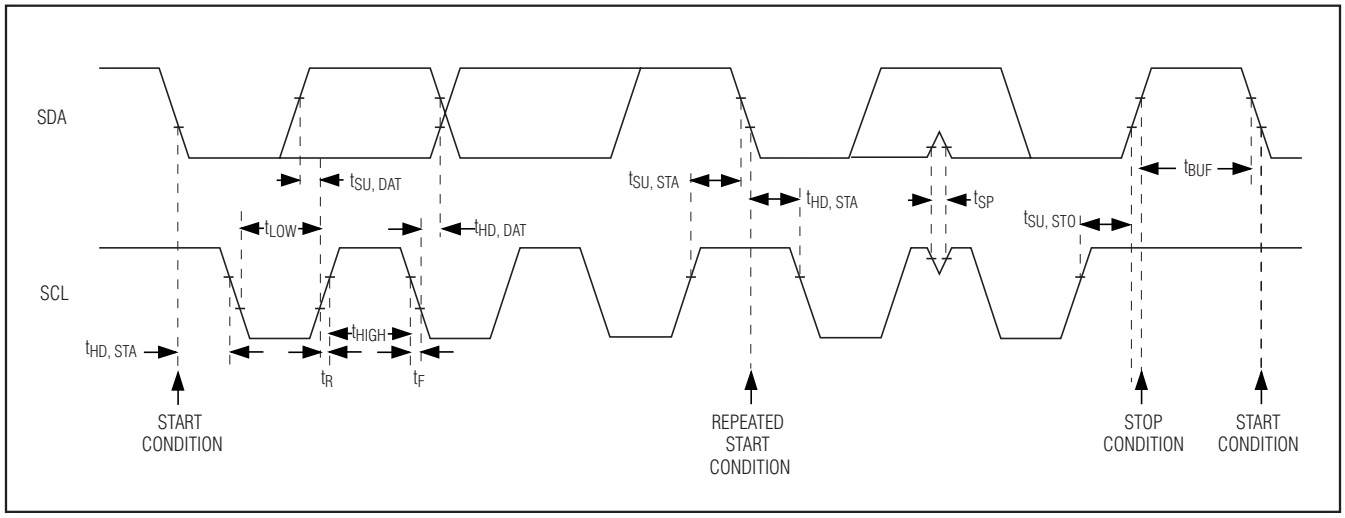


Figure 3. 2-Wire Serial-Interface Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

START and STOP Conditions

A master device initiates communication by issuing a START condition. A START condition is a high to low transition on SDA with SCL high. A STOP condition is a low to high transition on SDA while SCL is high (Figure 4). A START (S) condition from the master signals the beginning of a transmission to the MAX9744. The master terminates transmission, and frees the bus, by issuing a STOP (P) condition. The bus remains active if a Repeated START (Sr) condition is generated instead of a STOP condition.

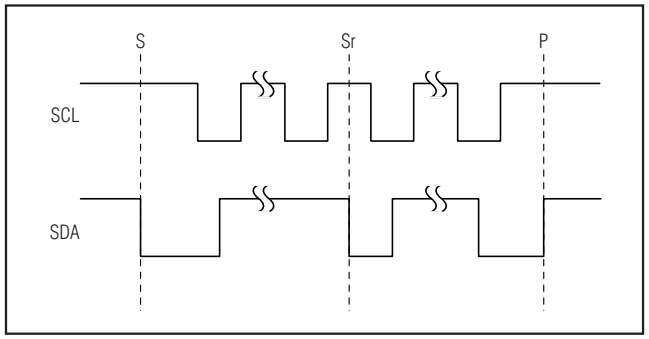


Figure 4. START, STOP, and Repeated START Conditions

Early STOP Conditions

The MAX9744 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition.

Slave Address

The slave address of the MAX9744 is 8 bits and consists of 3 fields: the first field is 5 bits wide and is fixed (10010), the second is a 2 bit field which is set through ADDR1 and ADDR2 (externally connected as logic-high or logic-low), and the third field is a R/$\overline{W}$ flag bit. Set R/$\overline{W}$ = 0 to write to the slave. A representation of the slave address is shown in Table 3.

When ADDR1 and ADDR2 are connected to GND, serial interface communication is disabled. Table 4 summarizes the slave address of the device as a function of ADDR1 and ADDR2.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9744 uses to handshake receipt of each byte of data (see Figure 5). The MAX9744 pulls down SDA during the master-generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may reattempt communication.

Table 3. Slave Address Block

SA7 (MSB)	SA6	SA5	SA4	SA3	SA2	SA1	SA0 (LSB)
1	0	0	1	0	ADDR2	ADDR1	R/$\overline{W}$

Table 4. Slave Address

ADDR2	ADDR1	SLAVE ADDRESS
0	0	I²C disabled
0	1	1001001_
1	0	1001010_
1	1	1001011_

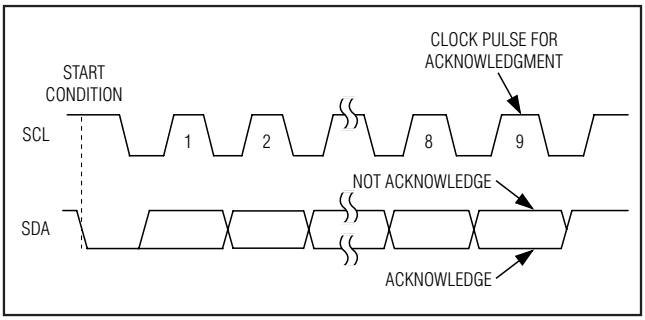


Figure 5. Acknowledge

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Write Byte

A write to the MAX9744 includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0 (see Table 3), one byte of data to the command register, and a STOP condition. Figure 6 illustrates the proper format for one frame.

A write to the MAX9744 consists of a 6-step sequence as seen below:

1) The **master** sends a START condition.
2) The **master** sends the 7 bits slave ID plus a write bit (low).
3) The addressed **slave** asserts an ACK on the data line.
4) The **master** sends 8 data bits.
5) The active **slave** asserts an ACK (or NACK) on the data line.
6) The **master** generates a stop condition.

Speaker Volume Control

The command register is used to control the volume level of the speaker amplifier. The two MSBs (A1 and A0) are set to 00, while V5–V0 is the data that is written into the addresses register to set the volume level (Tables 5 and 6).

WRITE BYTE FORMAT

S	SLAVE ADDRESS	$\overline{WR}$	ACK	DATA	ACK	P
	7 BITS	0		8 BITS		

SLAVE ADDRESS: EQUIVALENT TO CHIP-SELECT LINE OF A 3-WIRE INTERFACE.

DATA BYTE: GIVES A COMMAND.

Figure 6. Write Byte Format Example

Filterless Modulation/PWM

The MAX9744 features two output modulation schemes: filterless modulation or classic PWM, selectable through the I²C interface. Table 6 shows the register command to set the output scheme.

When switching between schemes, the output is not click-and-pop protected. To have click-and-pop protection when switching between output schemes, the device must enter shutdown mode and be configured to the new output scheme before the 220ms startup sequence is terminated.

Table 5. Data Byte Format

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
A1	A0	V5	V4	V3	V2	V1	V0

Table 6. Command Register Programming

A_0A_1	V5–V0	SETTING
00	XXXXXX	Volume level (Table 7)
01	000000	Filterless modulation
01	000001	Classic PWM

A_0A_1	V5–V0	SETTING
10	XXXXXX	Reserved
11	000100	Increased volume
11	000101	Decreased volume

Table 7. Speaker Volume Levels

V5	V4	V3	V2	V1	V0	VOLUME POSITION	SDA/VOL	VOLUME
							VOLUME INPUT VOLTAGE (V)	ATTENUATION (dB)
1	1	1	1	1	1	63	0.100 x V_{DD}	9.5
1	1	1	1	1	0	62	0.113 x V_{DD}	8.8
1	1	1	1	0	1	61	0.125 x V_{DD}	8.2
1	1	1	1	0	0	60	0.138 x V_{DD}	7.6
1	1	1	0	1	1	59	0.151 x V_{DD}	7.0
1	1	1	0	1	0	58	0.163 x V_{DD}	6.5
1	1	1	0	0	1	57	0.176 x V_{DD}	5.9
1	1	1	0	0	0	56	0.189 x V_{DD}	5.4
1	1	0	1	1	1	55	0.202 x V_{DD}	4.9
1	1	0	1	1	0	54	0.214 x V_{DD}	4.4
1	1	0	1	0	1	53	0.227 x V_{DD}	3.9
1	1	0	1	0	0	52	0.240 x V_{DD}	3.4
1	1	0	0	1	1	51	0.252 x V_{DD}	2.9
1	1	0	0	1	0	50	0.265 x V_{DD}	2.4
1	1	0	0	0	1	49	0.278 x V_{DD}	2.0
1	1	0	0	0	0	48	0.290 x V_{DD}	1.6
1	0	1	1	1	1	47	0.303 x V_{DD}	1.2
1	0	1	1	1	0	46	0.316 x V_{DD}	0.5
1	0	1	1	0	1	45	0.329 x V_{DD}	-0.5
1	0	1	1	0	0	44	0.341 x V_{DD}	-1.9
1	0	1	0	1	1	43	0.354 x V_{DD}	-3.4
1	0	1	0	1	0	42	0.367 x V_{DD}	-5.0
1	0	1	0	0	1	41	0.379 x V_{DD}	-6.0
1	0	1	0	0	0	40	0.392 x V_{DD}	-7.1
1	0	0	1	1	1	39	0.405 x V_{DD}	-8.9
1	0	0	1	1	0	38	0.417 x V_{DD}	-9.9
1	0	0	1	0	1	37	0.430 x V_{DD}	-10.9
1	0	0	1	0	0	36	0.443 x V_{DD}	-12.0
1	0	0	0	1	1	35	0.456 x V_{DD}	-13.1
1	0	0	0	1	0	34	0.468 x V_{DD}	-14.4
1	0	0	0	0	1	33	0.481 x V_{DD}	-15.4
1	0	0	0	0	0	32	0.494 x V_{DD}	-16.4

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Table 7. Speaker Volume Levels (continued)

V5	V4	V3	V2	V1	V0	VOLUME POSITION	SDA/VOL VOLUME INPUT VOLTAGE (V)	VOLUME ATTENUATION (dB)
0	1	1	1	1	1	31	0.506 x V_{DD}	-17.5
0	1	1	1	1	0	30	0.519 x V_{DD}	-19.7
0	1	1	1	0	1	29	0.532 x V_{DD}	-21.6
0	1	1	1	0	0	28	0.544 x V_{DD}	-23.5
0	1	1	0	1	1	27	0.557 x V_{DD}	-25.2
0	1	1	0	1	0	26	0.570 x V_{DD}	-27.2
0	1	1	0	0	1	25	0.583 x V_{DD}	-29.8
0	1	1	0	0	0	24	0.595 x V_{DD}	-31.5
0	1	0	1	1	1	23	0.608 x V_{DD}	-33.4
0	1	0	1	1	0	22	0.621 x V_{DD}	-36.0
0	1	0	1	0	1	21	0.633 x V_{DD}	-37.6
0	1	0	1	0	0	20	0.646 x V_{DD}	-39.6
0	1	0	0	1	1	19	0.659 x V_{DD}	-42.1
0	1	0	0	1	0	18	0.671 x V_{DD}	-43.7
0	1	0	0	0	1	17	0.684 x V_{DD}	-45.6
0	1	0	0	0	0	16	0.697 x V_{DD}	-48.1
0	0	1	1	1	1	15	0.710 x V_{DD}	-50.6
0	0	1	1	1	0	14	0.722 x V_{DD}	-54.2
0	0	1	1	0	1	13	0.735 x V_{DD}	-56.7
0	0	1	1	0	0	12	0.748 x V_{DD}	-60.2
0	0	1	0	1	1	11	0.760 x V_{DD}	-62.7
0	0	1	0	1	0	10	0.773 x V_{DD}	-66.2
0	0	1	0	0	1	9	0.786 x V_{DD}	-68.7
0	0	1	0	0	0	8	0.798 x V_{DD}	-72.2
0	0	0	1	1`	1	7	0.811 x V_{DD}	-74.7
0	0	0	1	1	0	6	0.824 x V_{DD}	-78.3
0	0	0	1	0	1	5	0.837 x V_{DD}	-80.8
0	0	0	1	0	0	4	0.849 x V_{DD}	-84.3
0	0	0	0	1	1	3	0.862 x V_{DD}	-86.8
0	0	0	0	1	0	2	0.875 x V_{DD}	-90.3
0	0	0	0	0	1	1	0.887 x V_{DD}	-92.8
0	0	0	0	0	0	0	0.900 x V_{DD}	MUTE

Applications Information

Filterless Class D Operation

The MAX9744 meets common EMC radiation limits without a filter when the speaker leads are less than approximately 10cm. Using lengths beyond 10cm is possible verifying against the appropriate EMC standard.

For longer speaker wire lengths, up to approximately 1m, use a simple ferrite bead and capacitor filter to meet EMC limits. Select a ferrite bead with 100Ω to 600Ω impedance, and rated for at least 3A. The capacitor value varies based on the ferrite bead chosen and the actual speaker lead length. Select the capacitor value based on EMC performance. See Figure 7 for the correct connections of these components.

When evaluating the device without a filter or a ferrite bead filter, include a series inductor (68µH for 8Ω load and 33µH for 4Ω load) to model the actual loudspeaker's behavior. Omitting this inductor reduces the efficiency, the THD+N performance, and the output power of the MAX9744.

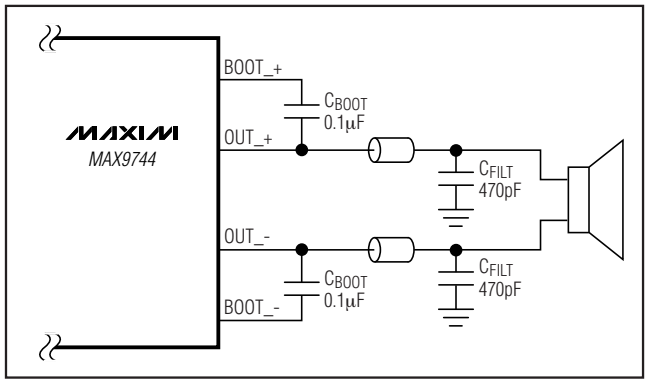

Figure 7. Ferrite Bead Filter

Inductor-Based Output Filters

Some applications use the MAX9744 with a full inductor/capacitor-based (LC) output filter. This is common for longer speaker lead lengths and to gain increased margin to EMC limits. Select the PWM output mode and use fixed-frequency modulation mode for best audio performance. See Figure 8 for the correct connections of these components.

The component selection is based on the load impedance of the speaker. Table 8 lists suggested values for a variety of load impedances.

Inductors L1 and L2 and capacitor C1 form the primary output filter. In addition to these primary filter components, other components in the filter improve its functionality. Capacitors C4 and C5 plus resistors R1 and R2 form a Zobel at the output. A Zobel corrects the output loading to compensate for the rising impedance of the loudspeaker. Without a Zobel, the filter has a peak in its response near the cutoff frequency. Capacitors C2 and C3 provide common-mode noise suppression to reduce radiated emissions.

Table 8. Suggested Values for LC filter

R_L (Ω)	L1, L2 (µH)	C1 (µF)	C2, C3 (µF)	R1, R2 (Ω)	C4, C5 (µF)
4	10	0.47	0.47	10	0.47
6	15	0.33	0.22	15	0.33
8	22	0.22	0.22	22	0.22

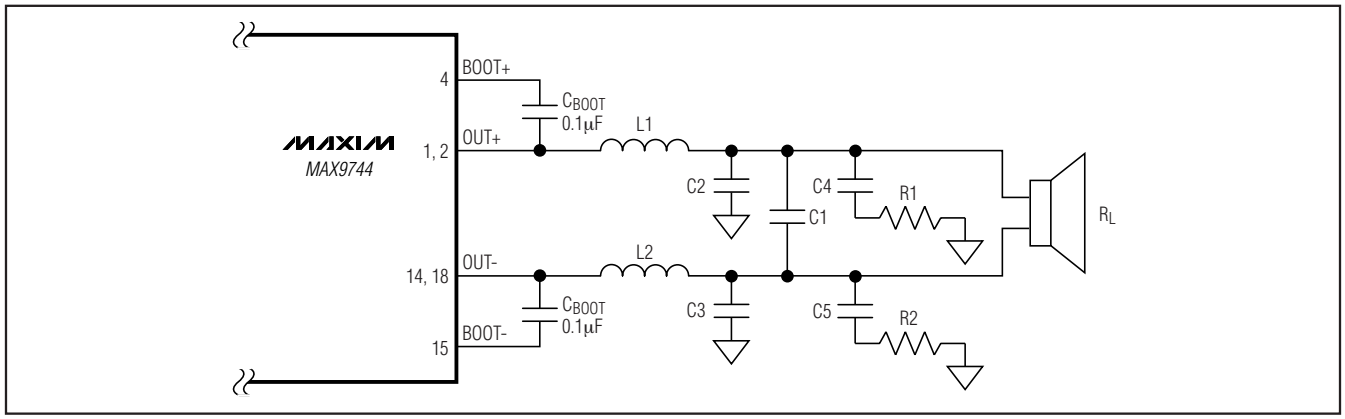

Figure 8. Output Filter for PWM Mode

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Component Selection

Gain-Setting Resistors

External feedback resistors set the gain of the MAX9744. The output stage has an internal 20dB gain in addition to the externally set input stage gain. Set the maximum gain by using resistors R_F and R_{IN} (Figure 9) as follows:

$$A_V = -30\left(\frac{R_F}{R_{IN}}\right) V/V$$

Choose R_F between 10kΩ and 50kΩ. Note that the actual gain of the amplifier is dependent on the volume level setting. For example, with the volume set to +9.5dB, the amplifier gain would be 9.5dB plus 20dB, assuming $R_{IN} = R_F$.

The input amplifier can be configured into a variety of circuits. The FB terminal is an actual operational amplifier output, allowing the MAX9744 to be configured as a summing amplifier, a filter, or an equalizer, for example.

Input Capacitor

An input capacitor (C_{IN}) in conjunction with the input impedance of the MAX9744 form a highpass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to automatically bias the signal to an optimum DC level. Assuming zero source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Choose C_{IN} that f_{-3dB} is well below the lowest frequency of interest. Use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

DC-Coupled Input

The input amplifier can accept DC-coupled inputs that are biased to the amplifier's bias voltage. DC-coupling eliminates input-coupling capacitors, reducing component count to potentially one external component. In this configuration the highpass filtering effect of the capacitors is lost, allowing low-frequency signals to be amplified.

Power Supplies

The MAX9744 features separate supplies for each portion of the device, allowing for the optimum combination of headroom power dissipation and noise immunity. The speaker amplifier is powered from PVDD and can range from 4.5V to 14V. The remainder of the device is powered by V_{DD}. Power supplies are independent of each other so sequencing is not necessary. Power may be supplied by separate sources or derived from a single higher source using a linear regulator (Figure 10).

BIAS Capacitor

BIAS is the output of the internally generated DC bias voltage. The BIAS bypass capacitor, C_{BIAS}, improves PSRR and THD+N by reducing power supply and other noise sources at the common-mode bias node, and also generates the clickless/popless, startup/shutdown, DC bias waveforms for the speaker amplifiers. Bypass BIAS with a 2.2µF capacitor to GND.

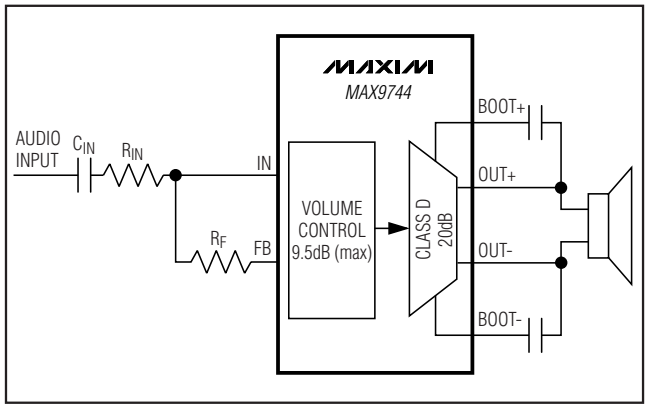


Figure 9. Setting Gain

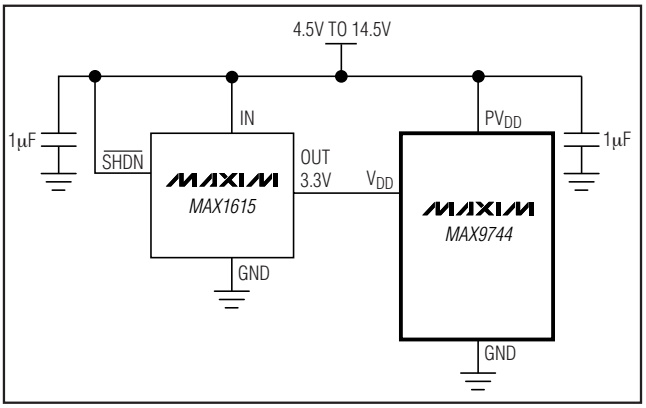


Figure 10. Using a Linear Regulator to Produce 3.3V from a Higher Power Supply

Supply Bypassing, Layout, and Grounding

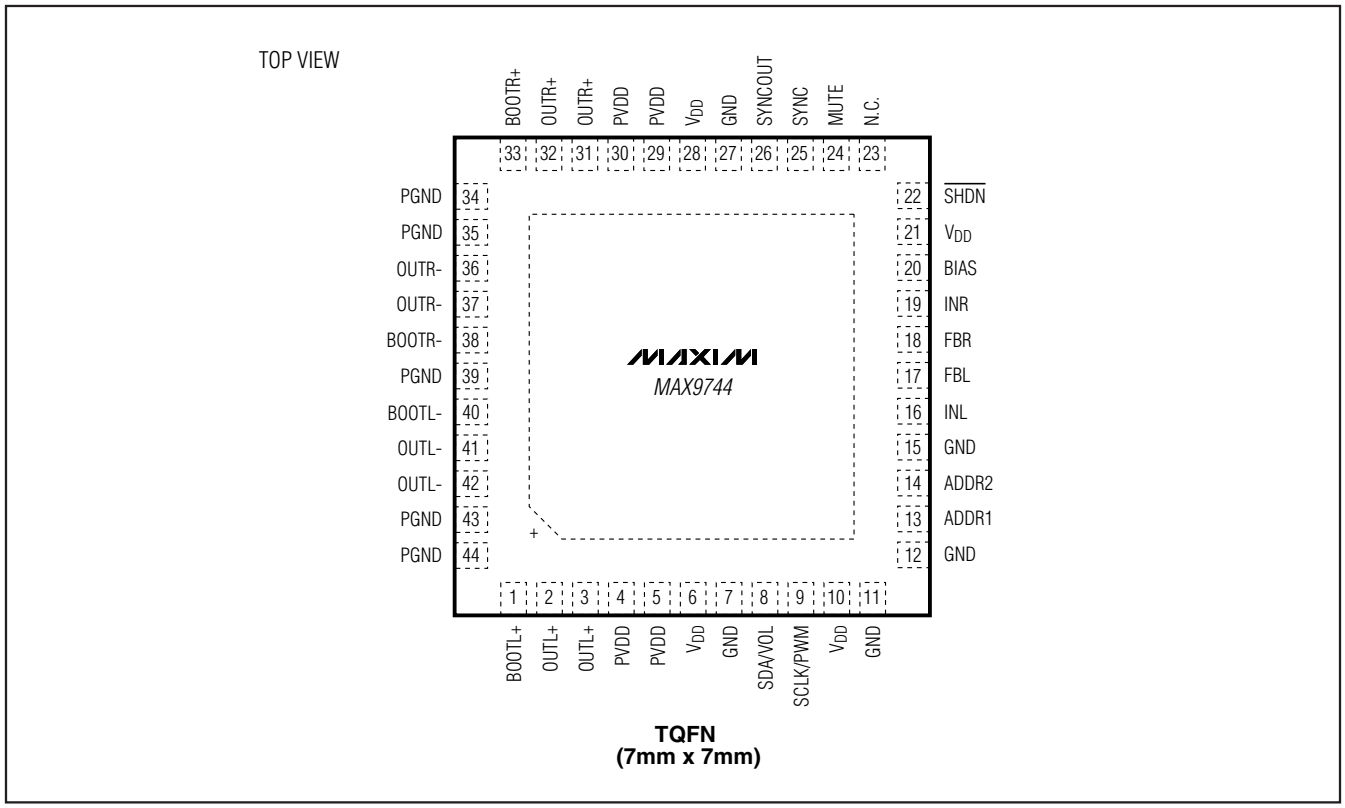
Proper layout and grounding are essential for optimum performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance. Large traces also aid in moving heat away from the package. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents any switching noise from coupling into the audio signal. Connect PGND and GND together at a single point on the PCB. Route all traces that carry switching transients away from GND and the traces/components in the audio signal path.

Connect all PVDD power supplies together and bypass with a 1µF capacitor to PGND. Connect all V_{DD} power supplies together and bypass with a 1µF capacitor to GND. Place a bulk capacitor between PVDD and PGND if needed.

Use large, low-resistance output traces. Current drawn from the outputs increase as load impedance decreases. High output trace resistance decreases the power delivered to the load. Large output, supply, and GND traces allow more heat to move from the MAX9744 to the air, decreasing the thermal impedance of the circuit.

The MAX9744 thin QFN package features an exposed thermal pad on its underside. This pad lowers the package's thermal resistance by providing a direct heat conduction path from the die to the PCB. Connect the exposed thermal pad to PGND by using a large pad and multiple vias to the PGND plane. The exposed pad must be connected to PGND for proper device operation.

Pin Configuration



TQFN
(7mm x 7mm)

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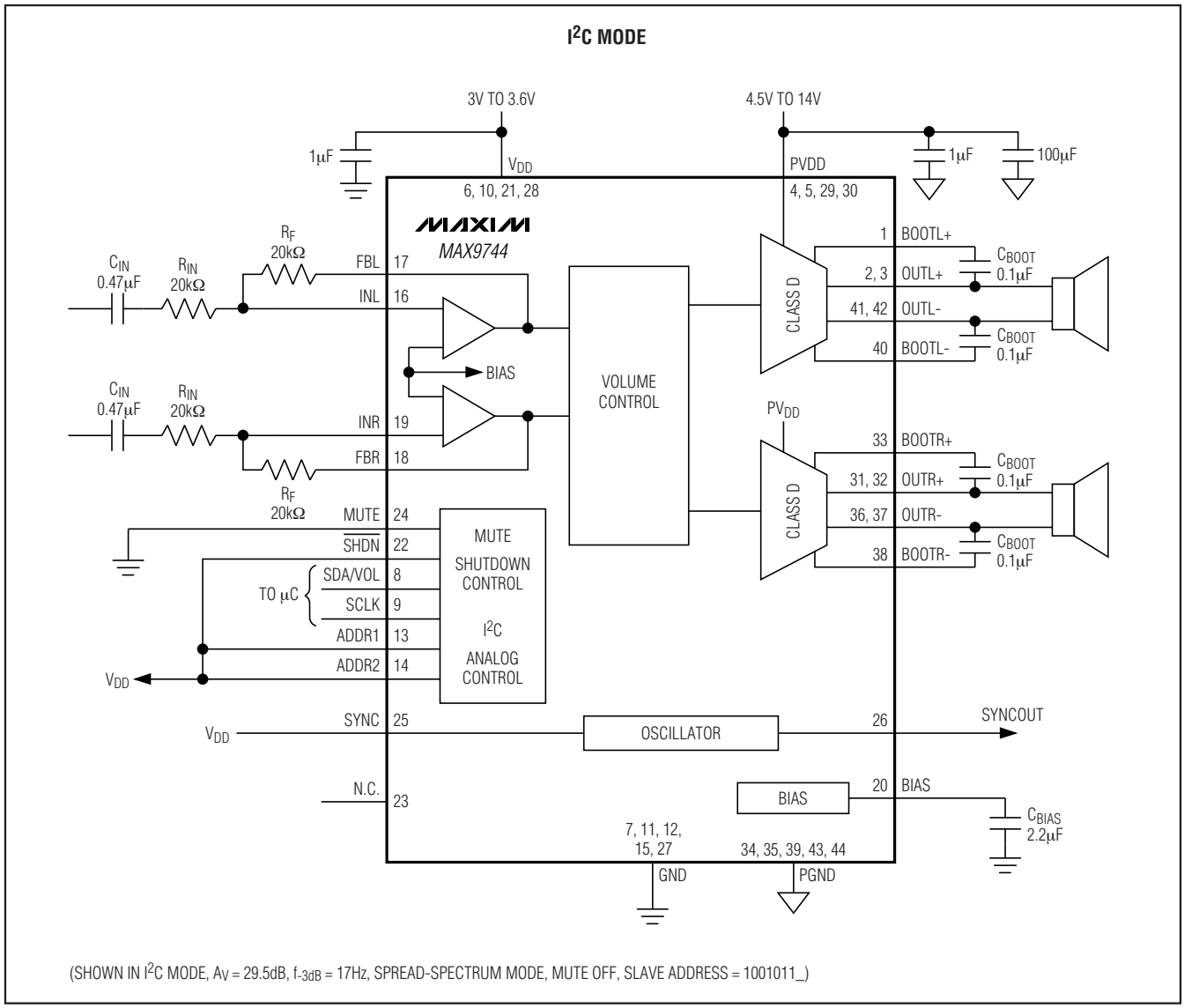
Functional Diagrams/Typical Application Circuits



(SHOWN IN I²C MODE, A_V = 29.5dB, f_{-3dB} = 17Hz, SPREAD-SPECTRUM MODE, MUTE OFF, SLAVE ADDRESS = 1001011_)

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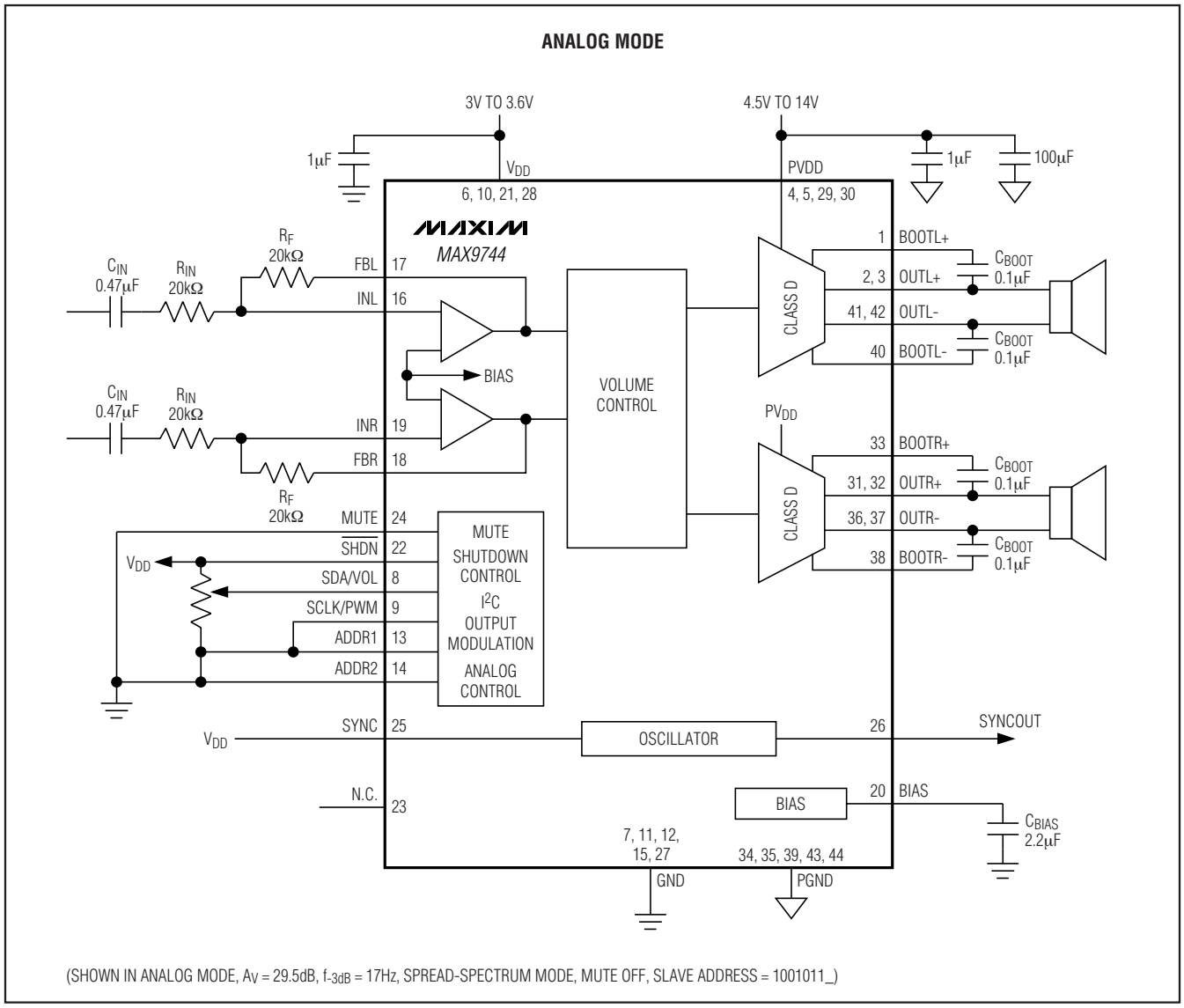
Functional Diagrams/Typical Application Circuits (continued)



(SHOWN IN ANALOG MODE, A_V = 29.5dB, f_{-3dB} = 17Hz, SPREAD-SPECTRUM MODE, MUTE OFF, SLAVE ADDRESS = 1001011_)

Chip Information

PROCESS: BICMOS

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
44 TQFN-EP	T4477-3	**21-0144**