

LVDS Dual 2x2 Crosspoint/Repeater Switch
Features

- Dual 2x2 Crosspoint/Repeater Switch
- Meets or Exceeds the Requirements of ANSI TIA/EIA-644-1995
- Designed for Signaling Rates up to 650 Mbit/s (325 MHz)
- Operates from a 3.3V Supply: -40°C to 85°C
- Low Voltage Differential Signaling with Output Voltages of $\pm 350\text{mV}$ into:
 - 100 Ohm load (PI90LV024)
 - 50 Ohm load Bus LVDS Signaling (PI90LVB024)
- Accepts $\pm 350\text{mV}$ differential inputs
- Wide common mode input range: 0.2V to 2.7V
- Output drivers are high impedance when disabled or when $V_{CC} \leq 1.5\text{V}$
- Inputs are open, short, and terminated fail safe
- Propagation Delay Time: 3.5ns
- ESD protection is 10kV on bus pins
- Bus Pins are High Impedance when disabled or with V_{CC} less than 1.5V
- TTL Inputs are 5V Tolerant
- Power Dissipation at 400Mbit/s of 250mW
- Available Packaging: 28-pin QSOP, 28-pin TSSOP

Description

The PI90LV024 and PI90LVB024 are monolithic dual 2x2 asynchronous crosspoint/repeater switches. The crosspoint function is based on a multiplexer tree architecture. Each 2x2 switch can be considered as a pair of 2:1 multiplexers that share the same inputs. The signal path through each switch is fully differential with minimal propagation delay. The signal path is unregistered, so no clock is required for the data inputs. The signal line drivers and receivers use Low Voltage Differential Signaling (LVDS) to achieve signaling rates as high as 650 Mbps.

The LVDS standard provides a minimum differential output voltage magnitude of 247mV into a 100 Ohm load and receipt of 100mV signals with up to 1V of ground potential difference between a transmitter and receiver. The PI90LVB024 doubles the output drive current to achieve Bus LVDS signaling levels with a 50 Ohm load.

The intended application of these devices is for loop-through and redundant channel switching for both point-to-point base-band (PI90LV024) and multipoint (PI90LVB024) data transmissions over controlled impedance media. The package pin assignments enables easy routing for applications requiring signal feedback.

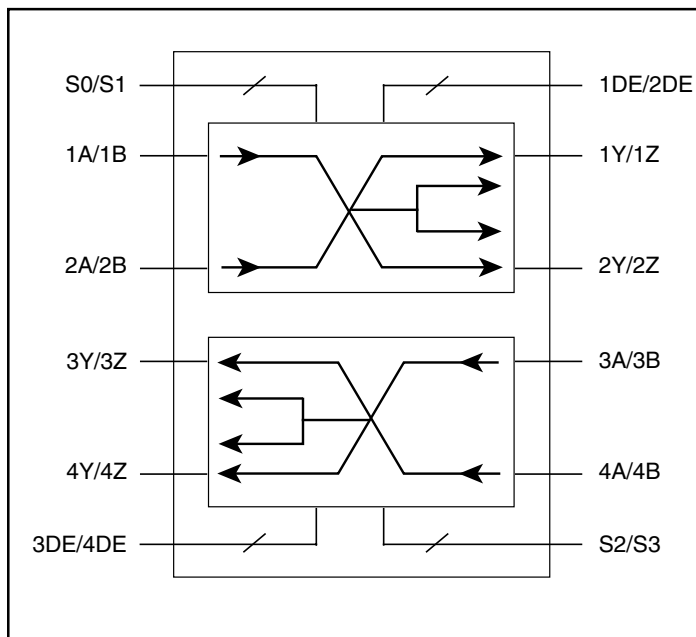
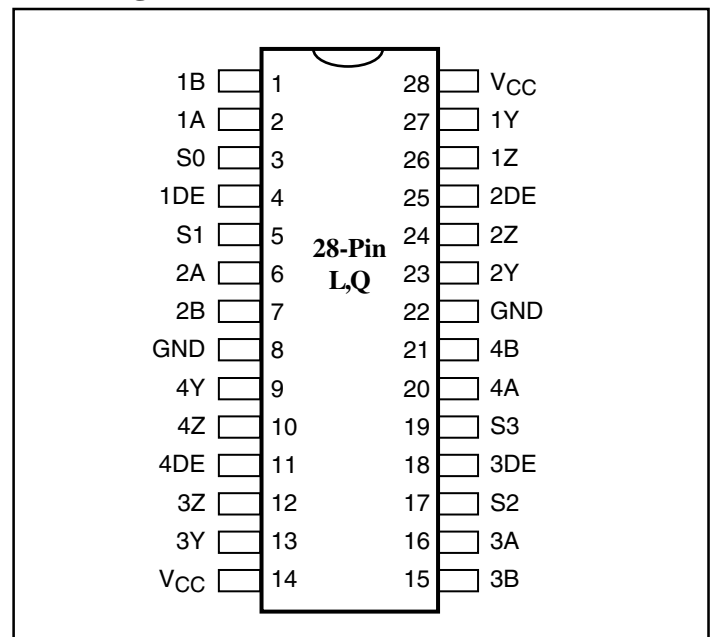
Block Diagram

Pin Configuration


Table 1. MUX Truth Table

Input		Output		Function
S3,S1	S2,S0	1Y/1Z-3Y/3Z	2Y/2Z-4Y/4Z	
0	0	1A/1B - 3A/3B	1A/1B - 3A/3B	Splitter
0	1	2A/2B - 4A/4B	2A/2B - 4A/4B	Splitter
1	0	1A/1B - 3A/3B	2A/2B - 4A/4B	Router
1	1	2A/2B - 4A/4B	1A/1B - 3A/3B	Router

Note: Setting nDE to 0 will set Output nY/nZ to High Impedance.

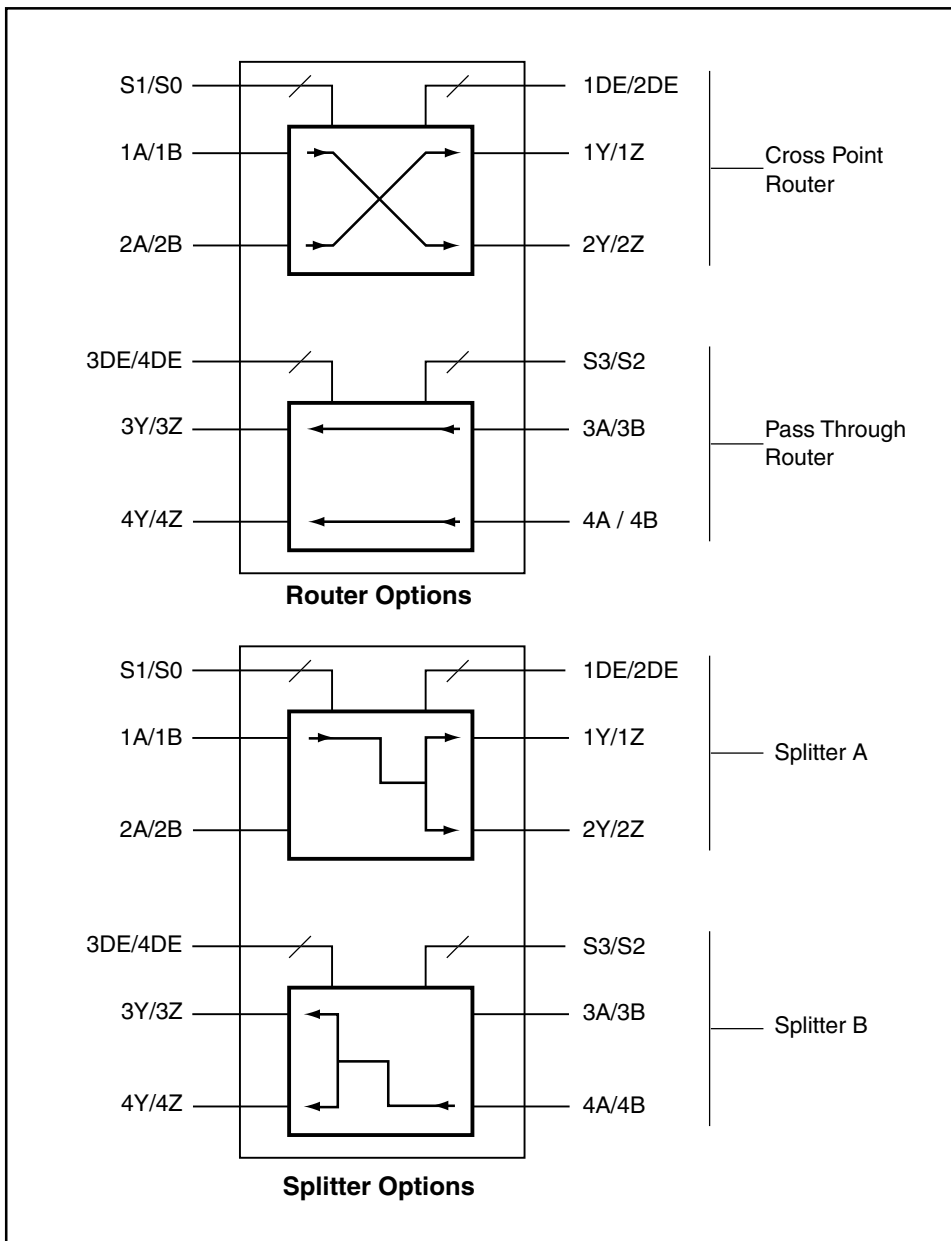


Figure 1. Possible Signal Routing

Absolute Maximum Ratings Over Operating Free-Air Temperature †

Supply Voltage Range, $V_{CC}^{(1)}$	-0.5V to 4V
Voltage Range (DE, S0, S1)	-0.5 to 6V
Input Voltage Range, V_I (A or B)	-0.5V to $V_{CC} + 0.5V$
Electrostatic Discharge: A, B, Y, Z, and GND ⁽²⁾	Class 3, A: 16kV, B: 600V
All Pins	Class 3, A: 7kV, B: 500V
Storage Temperature Range	-65°C to 150°C
Lead Temperature 1, 6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability.

Notes:

1. All voltage values, except differential I/O bus voltages, are with respect to ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7

Recommended Operating Conditions

	Min.	Nom.	Max.	Units
Supply Voltage, V_{CC}	3.0	3.3	3.6	V
High-Level Input Voltage, V_{IH}	2			
Low-Level Input Voltage, V_{IL}				
Magnitude of Differential Input Voltage $ V_{ID} $	0.1		0.6	
Common-Mode input Voltage, V_{IC} (see Figure 2)	$\frac{ V_{ID} }{2}$		$2.4 - \frac{ V_{ID} }{2}$	
			$V_{CC} - 0.8$	
Operating free-air temperature, T_A	-40		85	°C

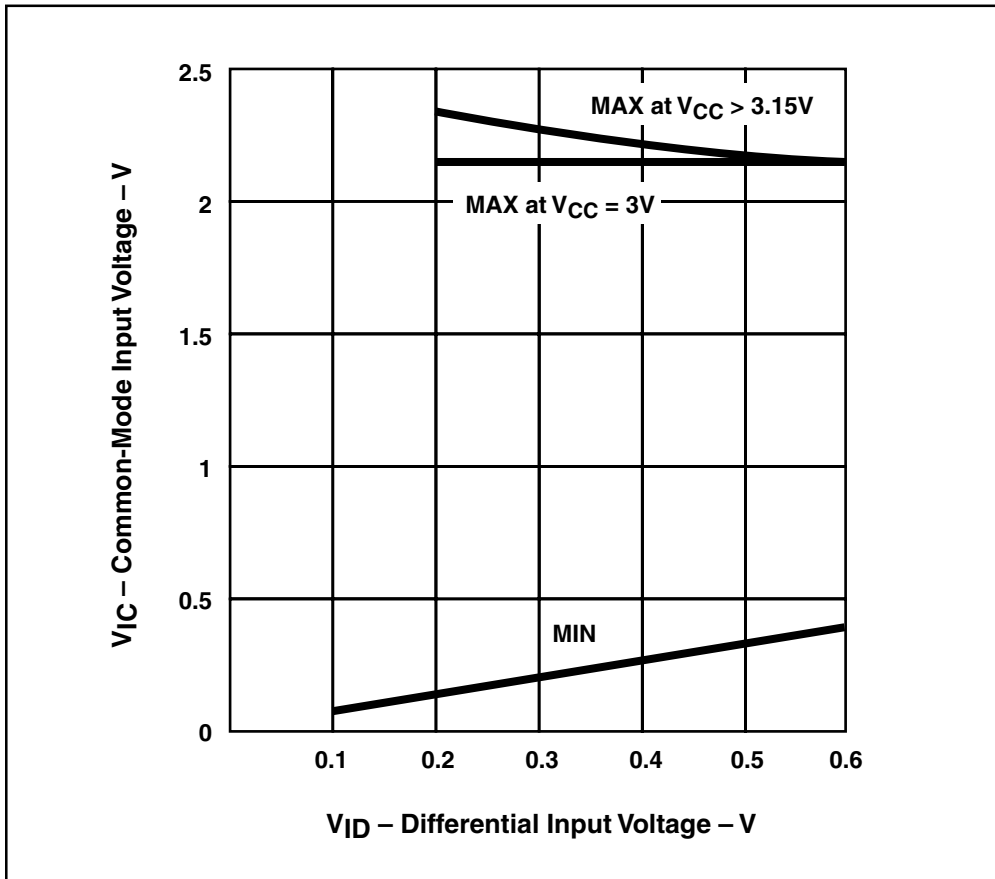


Figure 2. Common-Mode Input Voltage vs. Differential Voltage

Receiver Electrical Characteristics Over Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Units
V_{ITH+}	Positive-going differential input voltage threshold	$V_{CM} = 1.2V$			100	mV
V_{ITH-}	Negative-going differential input voltage threshold		-100			
I_I	Input current (A or B inputs)	$V_I = 0V$	-2		-20	μA
		$V_I = 2.4V$	-1.2			
I_I (OFF)	Power-off input current (A or B inputs)	$V_{CC} = 0V$			20	

Receiver / Driver Electrical Characteristics Over Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Units	
V _{OD}	Differential output voltage magnitude	R _L = 100 Ohm (LV024)	See Fig. 3	247	440	590	mV
ΔV _{OD}	Change in differential output voltage magnitude between logic states			-50		50	
V _{OC(SS)}	Steady-state common-mode output voltage	R _L = 50 Ohm (LVB024)	See Fig. 4	1.125		1.375	V
ΔV _{OC(SS)}	Change in steady-state common-mode output voltage between logic states			-50	3	50	mV
V _{OC(PP)}	Peak-to-peak common-mode output voltage					150	
I _{CC}	Supply current	No Load			16	24	mA
		R _L = 100 Ohm (LV024)			26	40	
		R _L = 50 Ohm (LVB024)			42	54	
		Both Channels Disabled			6	12	
I _H	High-level input current	DE	V _{IH} = 5			40	nA
		S1, S2, S3, S4				-3	μA
I _{IL}	Low-level input current	DE	V _{IL} = 0.8V			-20	nA
		S1, S2, S3, S4				10	μA
I _{OS}	Short-circuit output current	V _{OY} or V _{OZ} = 0V, V _{OD} = 0V (LV024)				-10	mA
		V _{OY} or V _{OZ} = 0V, V _{OD} = 0V (LVB024)				-10	
		V _{OY} or V _{OZ} = 0V, V _{OD} = 0V (LVB024)				-10	
		V _{OY} or V _{OZ} = 0V, V _{OD} = 0V (LVB024)				-10	
I _{OZ}	High-Impedance output current	V _{OD} = 600mV			1.5	±25	nA
		V _O = 0V or V _{CC}			1.5	±25	
I _{O(OFF)}	Power-off output current	V _{CC} = 0V, V _O = 3.6V			1.5	±40	
C _{IN}	Input capacitance				3		pF
		S0-S3, 1DE-40DE			8		pF

Note:

1. All typical values are at 25°C and with a 3.3 supply

Differential Receiver to Driver Switching Characteristics Over Recommended Operating Conditions

(unless otherwise noted)

Symbol	Parameter		Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Units
t _{PLH}	Differential propagation delay, low-to-high		C _L = 10pF (See Fig. 5)		4.0	6.0	ns
t _{PHL}	Differential propagation delay, high-to-low				4.0	6.0	
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})				0.5	–	
t _r	Transition, low-to-high	PI90LV024			1.0	1.5	
t _r	Transition, low-to-high	PI90LVB024			0.8	1.3	
t _f	Transition, high-to-low	PI90LV024			1.0	1.5	
t _f	Transition, high-to-low	PI90LVB024			0.8	1.3	
t _{PHZ}	Propagation delay time, high-level-to-high-impedance output		(See Fig. 6)		4.0	10	
t _{PLZ}	Propagation delay time, low-level-to-high-impedance output				4.3	10	
t _{PZH}	Propagation delay time, high-impedance-to-high-level output				3.0	10	
t _{PZL}	Propagation delay time, high-impedance-to-low-level output				2.0	10	
t _{PHL_R1_Dx}	Channel-to-channel skew, receiver to driver ⁽²⁾				95		ps
t _{PLH_R1_Dx}					95		
t _{PHL_R2_Dx}					95		
t _{PLH_R2_Dx}					95		

Notes:

1. All typical values are at 25°C and with a 3.3 supply
2. These parametric values are measured over supply voltage and temperature ranges recommended for the device

Parameter Measurement Information

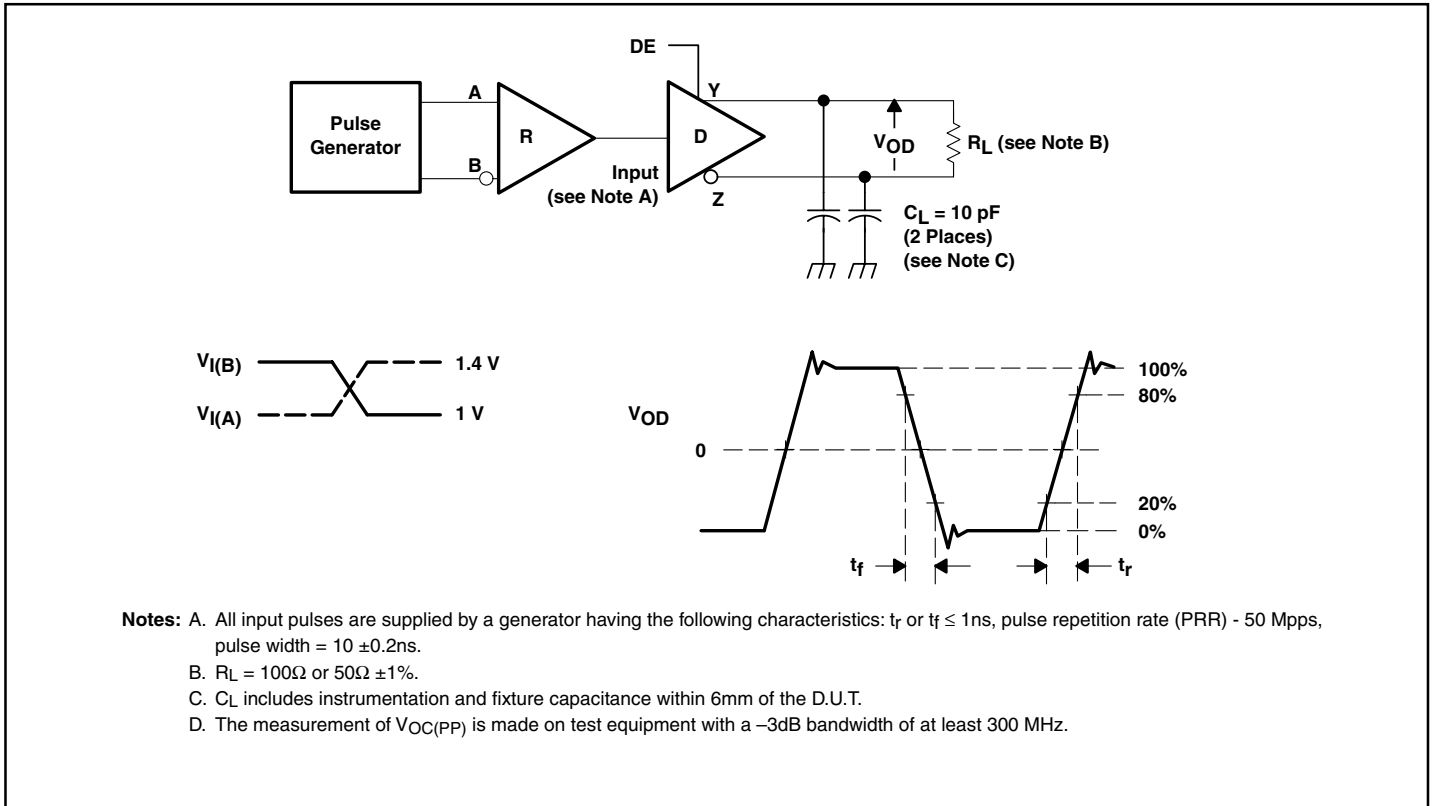


Figure 3. Test Circuit and Voltage Definitions for the Differential Output Signal

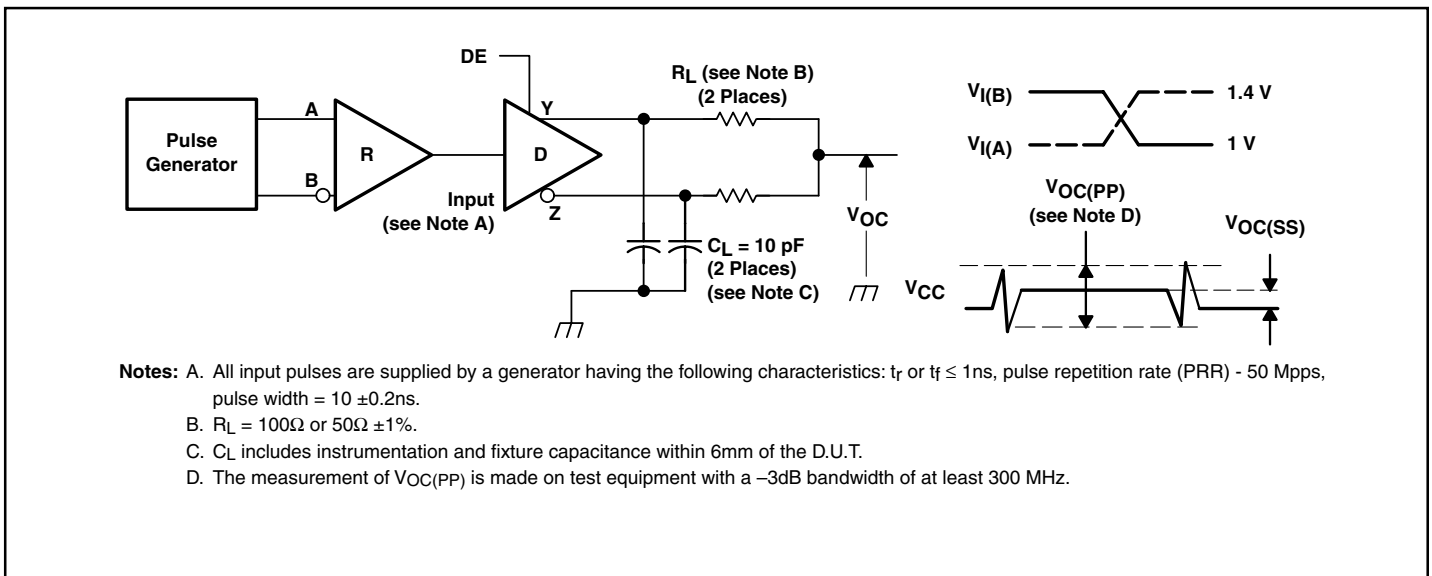


Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

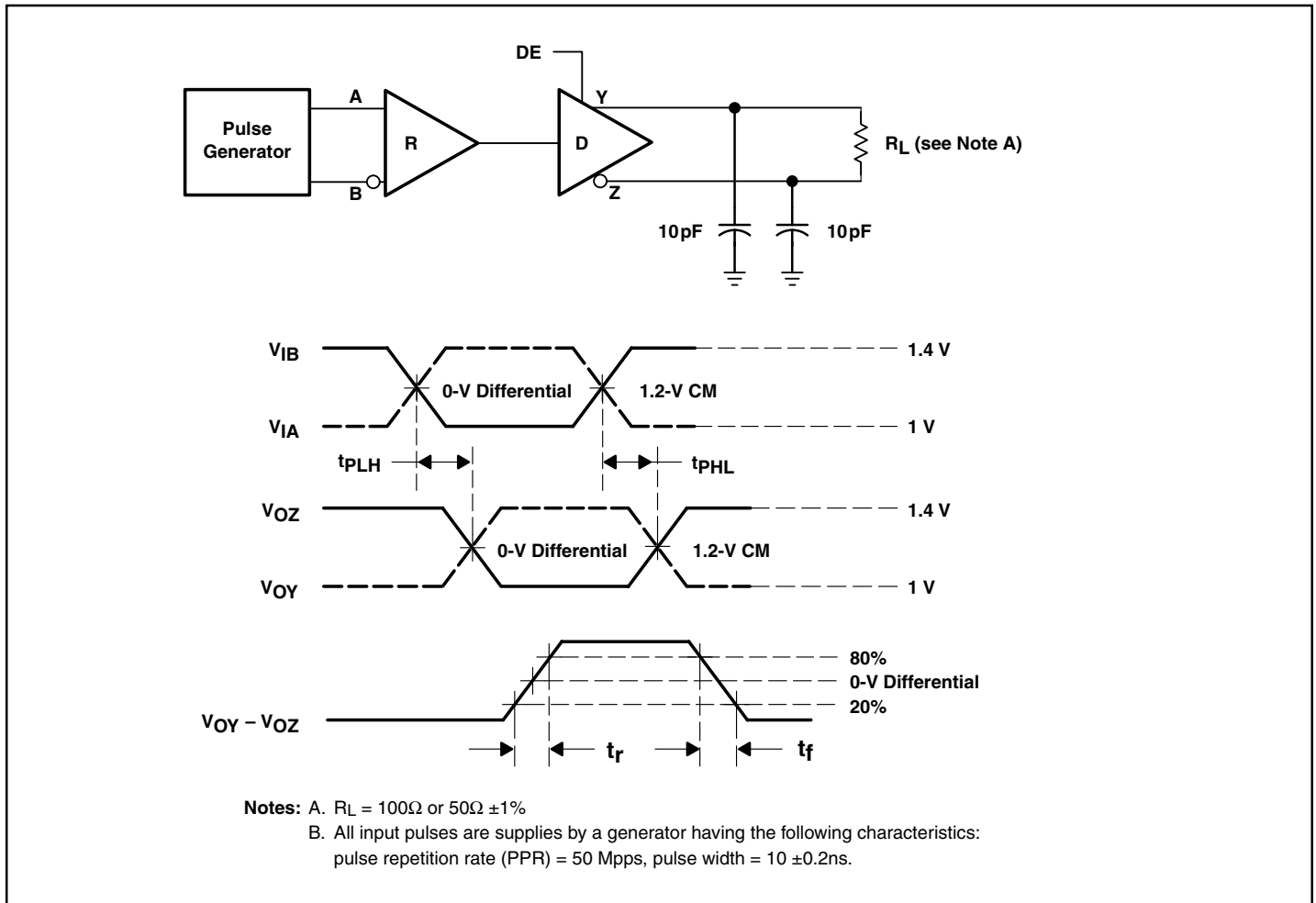


Figure 5. Differential Receiver to Driver Propagation Delay and Driver Transition Time Waveforms

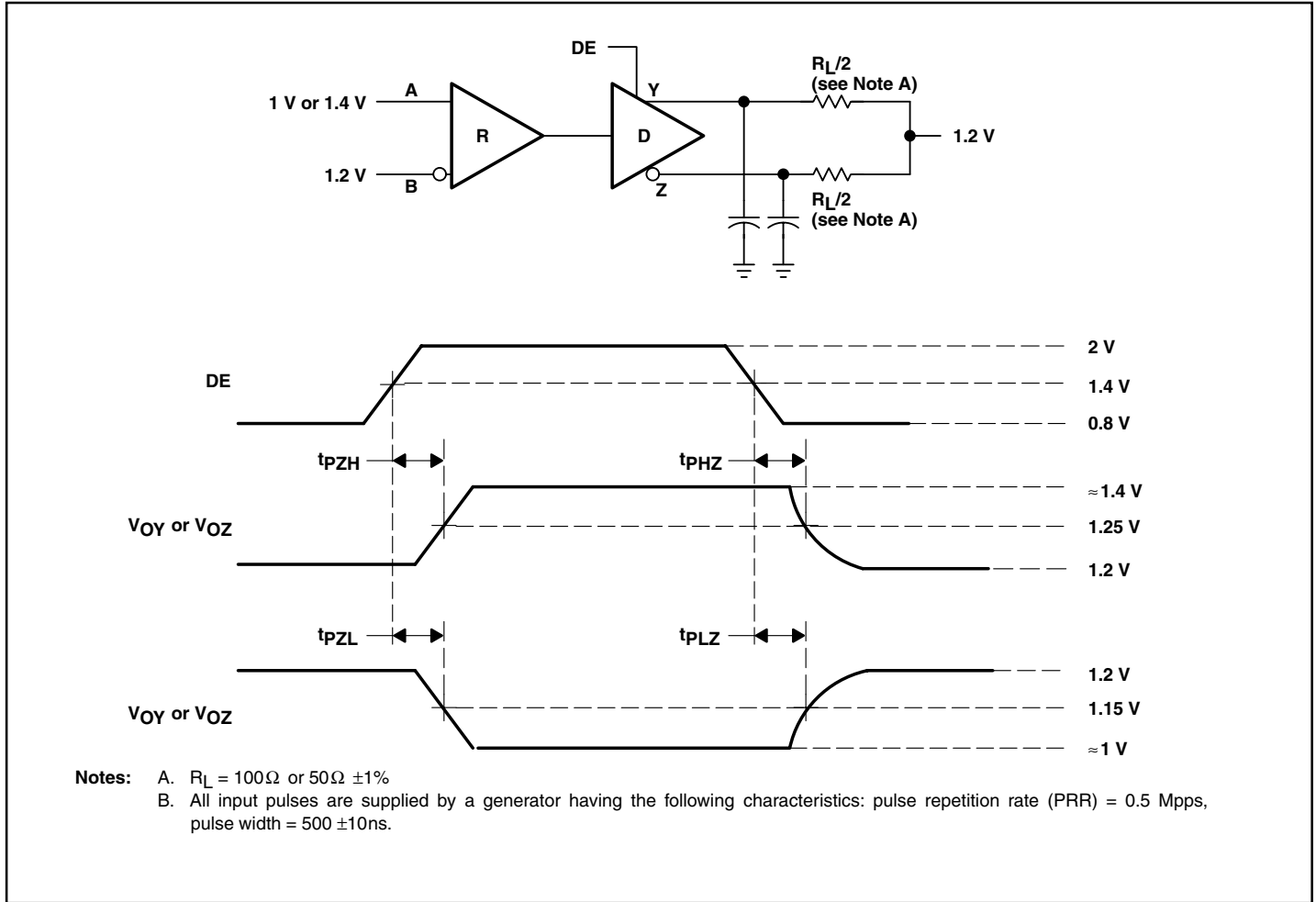
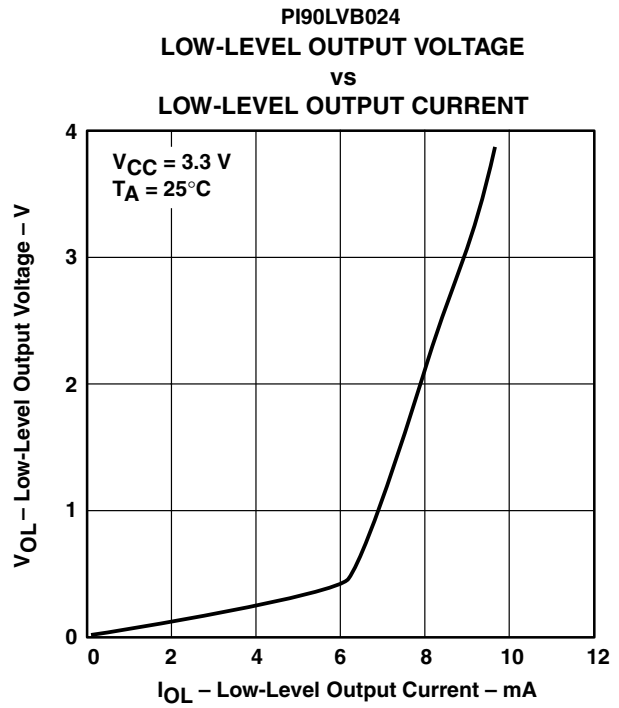
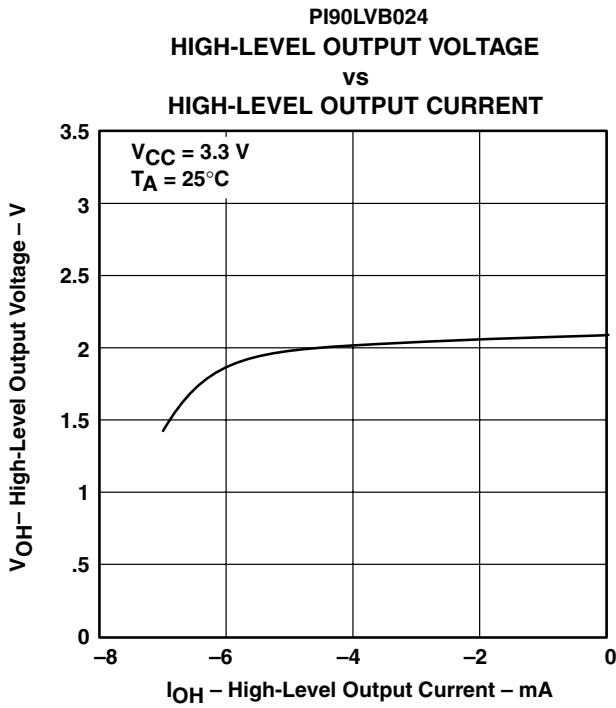
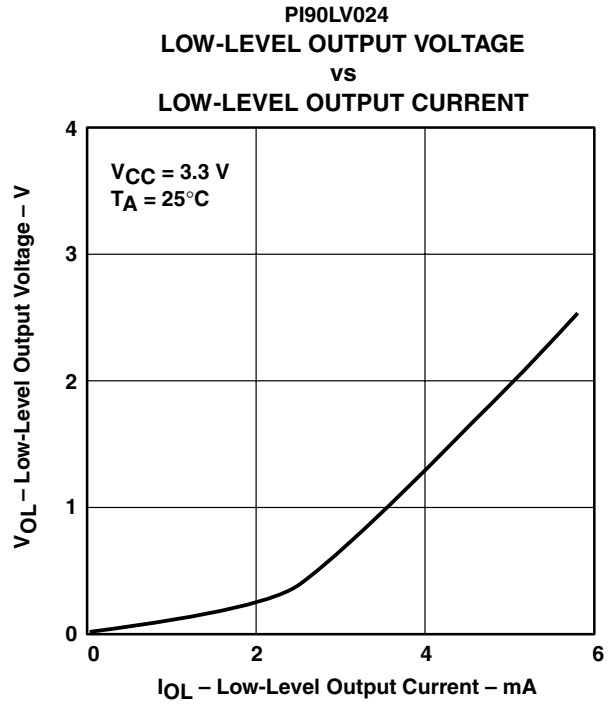
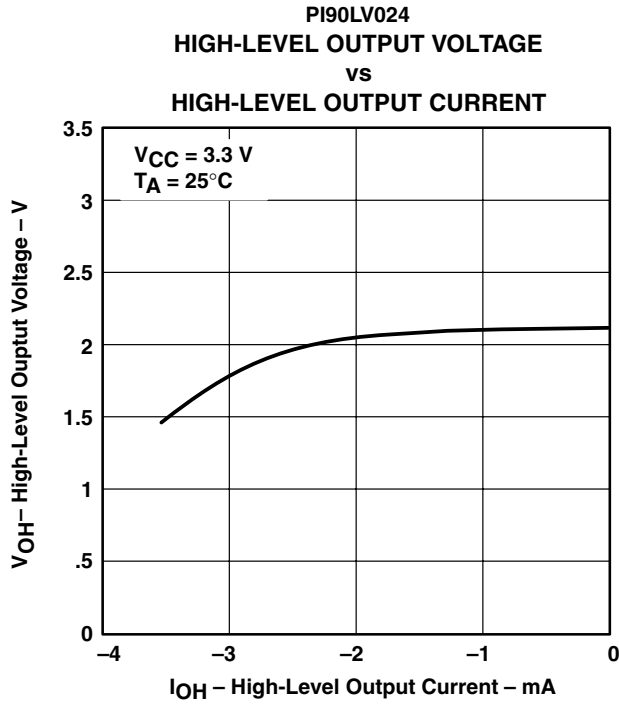
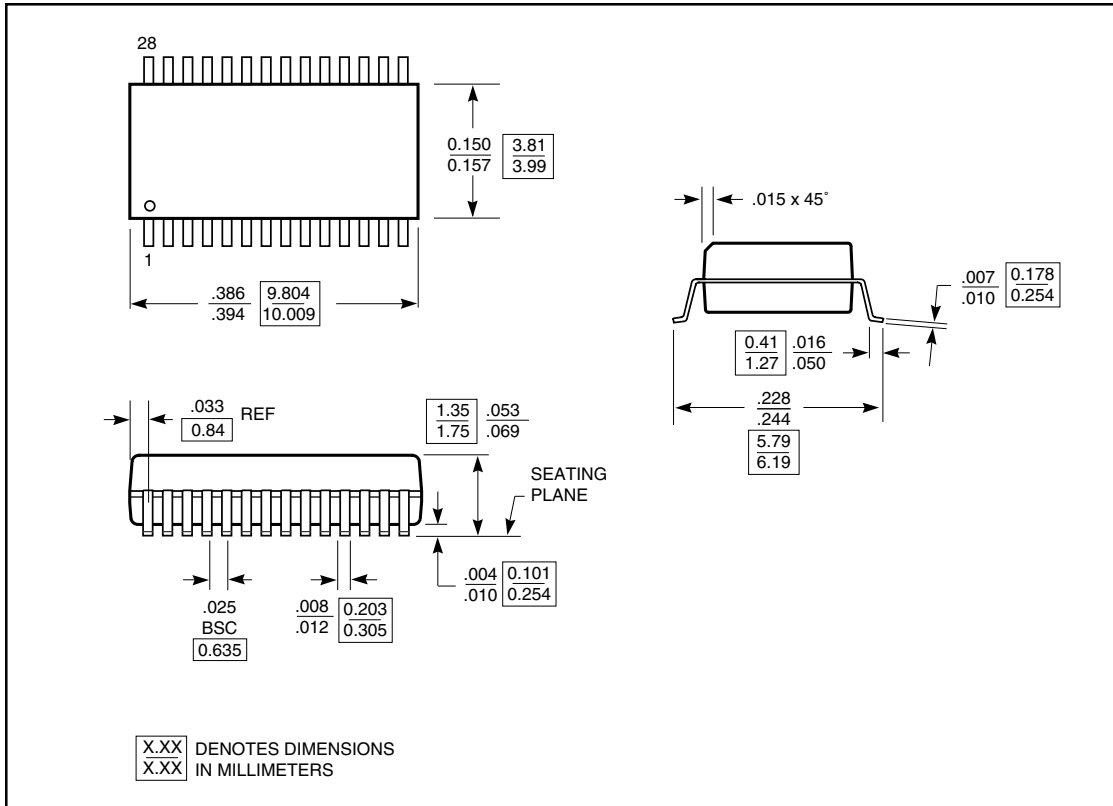


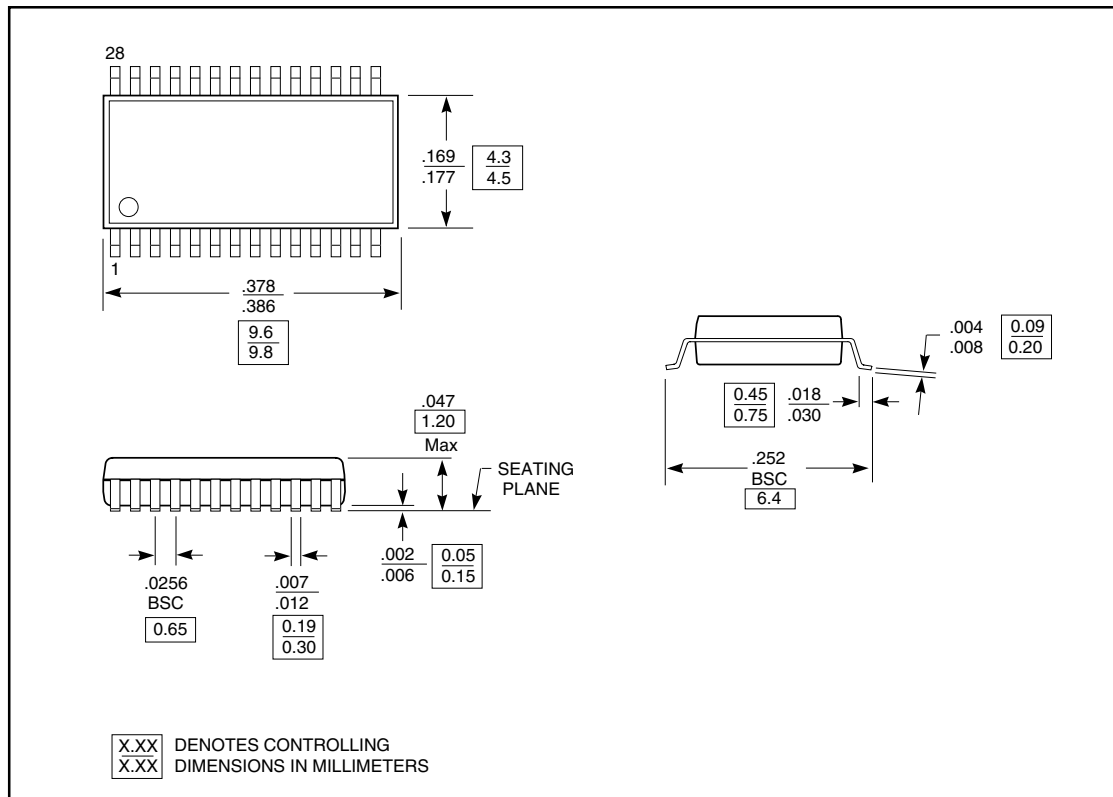
Figure 6. Enable and Disable Timing Circuit

Typical Characteristics


Packaging Mechanical: 28-Pin QSOP



Packaging Mechanical: 28-Pin TSSOP





Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
PI90LV024Q	Q28	28-pin 150-mil SOIC	-40°C to 85°C
PI90LV024L	L28	28-pin 170-mil TSSOP	
PI90LVB024Q	Q28	28-pin 150-mil SOIC	
PI90LVB024L	L28	28-pin 170-mil TSSOP	

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