Features

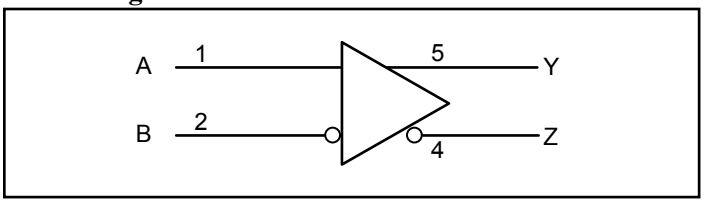
- Complies with ANSI/TIA/EIA-644-A LVDS standard
- LVDS receiver inputs accept LVPECL signals
- Low jitter 660 Mbps fully differential data path
- Bus-Terminal ESD exceeds 2kV
- Single +3.3V supply voltage operation
- Receiver Differential Input Voltage Threshold < ±100mV
- Receiver open-circuit failsafe
- Low-Voltage Differential Signaling with typical Output Voltages of 350mV into:
  – 100Ω Load (PI90LV03)
  – 50Ω Load (PI90LVB03)
- Typical Propagation Delay Times of 1.5ns
- Typical Power Dissipation of 20mW @ 200 MHz
- Outputs are High Impedance with V_{CC} < 1.5V
- Industrial Temperature Range: –40°C to 85°C
- Packaging:
  - 6-pin space-saving SOT-23 (T)

Function Table

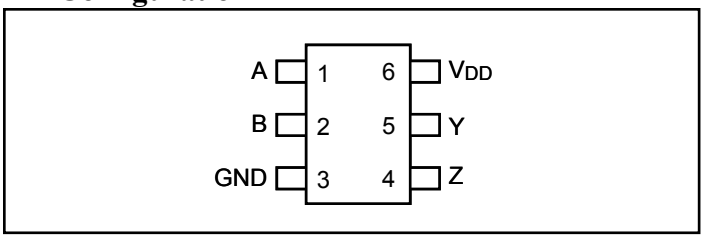
Inputs	Outputs
$V_{ID} = V_A - V_B$	$V_Y - V_Z$
$V_{ID} > 50mV$	H
$50mV < V_{ID} < 50mV$	X
$V_{ID} \leq -50mV$	L
Open	H

Notes:
1. H = high level; L = low level; X = indeterminate

Block Diagram



Pin Configuration



Description

PI90LV03 and PI90LVB03 are single LVDS Repeaters that use low-voltage differential signaling (LVDS) to support data rates up to 660 Mbps. The PI90LVB03 features high-drive output. Both products are designed for applications requiring high-speed, low-power consumption, low-noise generation, and a small package.

The LVDS Repeaters take an LVDS input signal and provide an LVDS output to address various interface logic requirements such as signal isolation, repeater, stub length, and Optical Transceiver Modules. In many large systems, signals are distributed across backplanes, and the distance between the transmission line and the unterminated receivers are one of the limiting factors for system speed. The buffers can be used to reduce the 'stub length' by strategic device placement along the trace length. They can improve system performance by allowing the receiver to be placed very close to the main transmission line or very close to the connector on the card. Longer traces to the LVDS receiver can then be placed after the buffer.

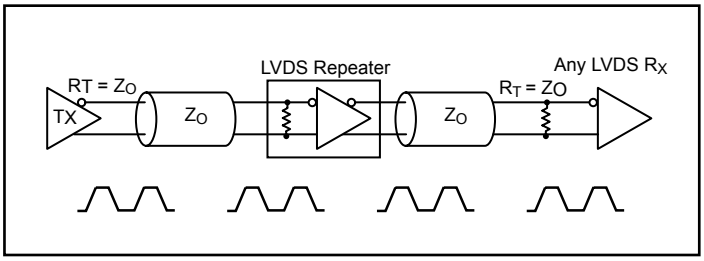
The buffer's wide input dynamic range enables them to receive differential signals from LVPECL and LVDS sources. The devices can be used as compact high-speed serial translators between LVPECL and LVDS data lines. The differential translation provides a simple way to mix and match Optical Transceiver ICs from various vendors without redesigning the interfaces.

Applications

The PI90LV03 and PI90LVB03 provide differential translation between LVDS and PECL devices for high-speed, point-to-point interface and telecom applications:

– ATM
– SONET/SDH
– Switches
– Routers
– Add-Drop Multiplexers

High-Speed Differential Cable Repeater Application



Absolute Maximum Ratings Over Operating Free-Air Temperature (unless otherwise noted)(2)

Supply Voltage Range, V_{CC}(1)	–0.5V to 4V
Voltage Range (A, B , or R_{OUT})	–0.5 to V_{CC} +0.5V
ESD rating (HBIN, 1.5kΩ, 100pF)	≥2KV
Storage Temperature Range	–65°C to 150°C
Lead Temperature 1.6 mm (1/16 inch) from case for 10 seconds	250°C

Notes:
1. All voltage values, except differential I/O bus voltages, are with respect to ground terminal.
2. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability.

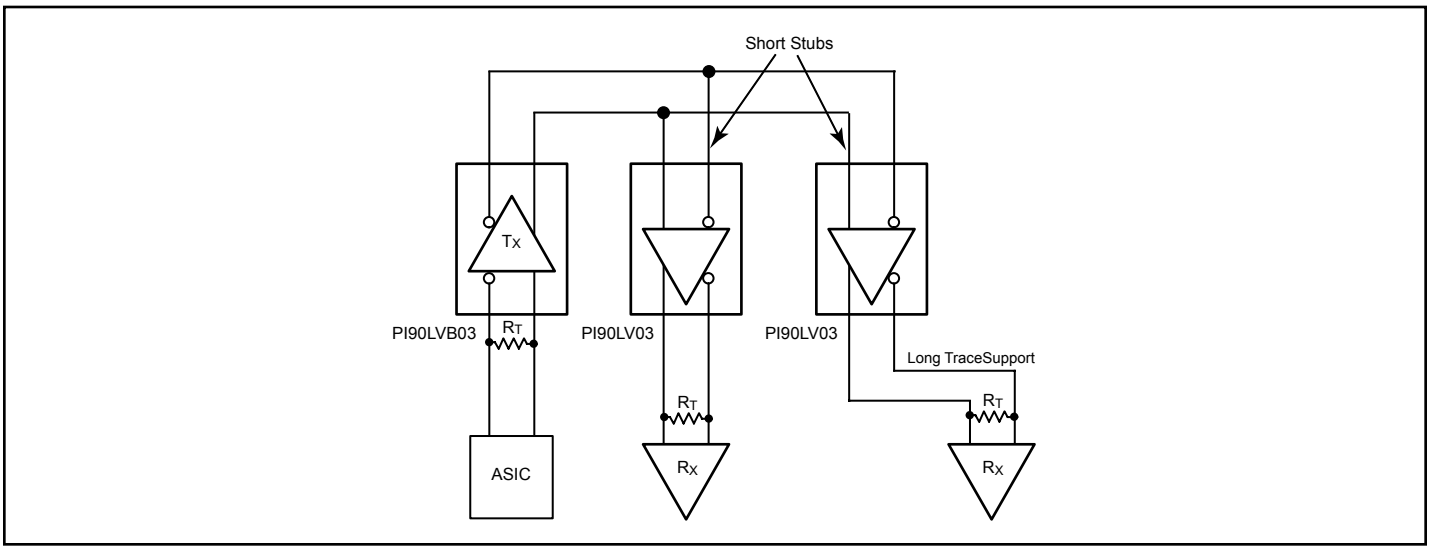


Figure 2. Backplance Stub-Hider Application

Dissipation Rating Table

Package	$T_A \leq 25°C$ Power Rating	Derating Factor Above $T_A = 25°C$	$T_A = 85°C$ Power Rating
6-pin SOT-23 (T)	385mW	3.1mW/°C	200mW

Notes:
1. This is the inverse of the junction-to-ambient thermal vsistance when board-mounted (low-K) and with no air flow.

Recommended Operating Conditions

Symbol	Paramters	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
$\lvert V_{ID} \rvert$	Magnitude of differential Voltage	0.1		0.6	
V_{IC}	Common-Mode Intput Voltage(6)	0		$2.0 - \frac{\lvert V_{ID} \rvert}{2}$	
T_A	Operating Free-air Temperature	-40		85	°C

Common-Mode Input Voltage vs. Differenital Input Voltage

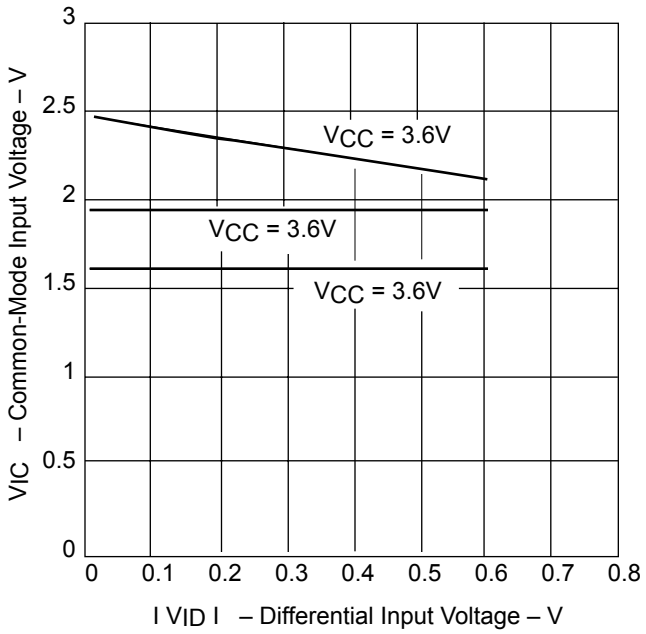


Figure 3. V_{IC} vs. V_{ID} and V_{CC}

Note:
1. All typical values are at 25°C and with a 3.3V supply.

Electrical Characteristics over Recommended Operating Conditions (unless otherwise noted)**.**

Symbol	Parameter	Test Condition		Min.	Typ.(1)	Max.	Units
V_{ITH+}	Positive-going differential input voltage threshold	See figures 3 and 4 and table 1				50	mV
V_{ITH-}	Negative-going differential input voltage threshold			-50			
I_I	Input Current (A or B inputs)	V_I - 0V				±20	µA
		V_I = 2.4V or V_{CC} -0.8		-1.2			
I_{ID}	High-level input current (I_{IA} - I_{IB})	V_{IA} = 0V, V_{IB} = 0.1V V_{IA} = 2.4V, V_{IB} = 2.3V				±2	
$\lvert V_{OD} \rvert$	Differential output voltage magnitude	R_L = 100Ω (LV03); R_L = 50Ω (LVB03); See Figure 4		247	350	454	mV
$\Delta \lvert V_{OD} \rvert$	Change in differential output voltage magnitude			-50		50	
$V_{OC(SS)}$	Steady-State common-mode output voltage	See Figure 5		1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in Steady-State common-mode output voltage between logic states			-50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				25	100	
I_{CC}	Supply Current	V_I = 0V or V_{CC} No load			7	9	mA
		V_I = 0V or V_{CC}, R_L = 100Ω (LV03)			9.5	12.5	
		V_I = 0V or V_{CC}, R_L = 50Ω (LVB03)			18	25	
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0V	LV03		3	10	
			LVB03		6	20	
		V_{OD} = 0V	LV03			10	
			LVB03			20	
$I_{O(OFF)}$	Power-off output current	V_{CC} = 0V, V_O = 3.6V				±1	µA
C_I	Input load capacitance				3		pF

Receiver Switching Characteristics over Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Propagation delay, low to high level outputs	LV03 R_L = 100Ω, LVB03 R_L = 50Ω; C_L = 10pF See Figure 6		1.4	6	ns
t_{PHL}	Propagation delay, high to low level outputs			1.4	6	
t_R	Output signal rise time			0.5	1	
t_F	Output signal fall time			0.5	1	
$t_{sk(p)}$	Pulse skew (| t_{PHL} - t_{PLH} |)(2)			50		ps
t_{skpp}	Part-to-part skew			1.5		ns
f_{max}	Maximum throughtput data rate(3)			660		mbps

Notes:
1. All typical values are at 25°C and with a 3.3V supply
2. $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.
3. f_{max} generator input conditions: 50% duty cycle, 200mV, Output criteteria: 45% to 55% duty cycle, $V_{OD} \geq 250mV$

Parameter Measurement Information

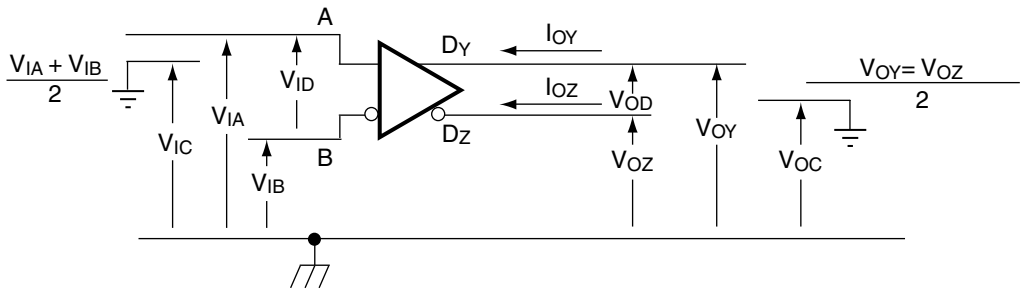


Figure 4. Voltage Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

Applied Voltages (V)		Resulting Differenital Input Votlages (mV)	Resulting Common-Mode Input Voltages (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25	1.20	50	1.2
1.15	1.20	-50	1.2
2.4	2.35	50	2.35
2.3	2.35	-50	2.35
0.05	0	50	0.05
0	0.05	-50	0.05
1.5	0.9	600	1.2
0.9	1.5	-600	1.2
2.4	1.8	600	2.1
1.8	2.4	-600	2.1
0.6	0	600	0.3
0	0.6	-600	0.3

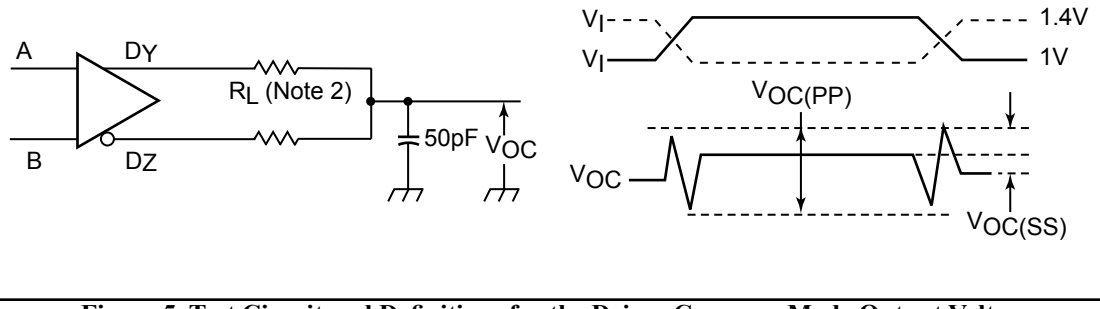


Figure 5. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

Notes:

1. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ns, Pulse Repetition Rate (PPR) = 0.5 Mpps, pulse width = 500 ±10ns. C_L includes instrumentation and fixture capacitance within 0.06m of the D.U.T. The test measurement of $V_{OC(PP)}$ is made on test equipment with a –3dB bandwidth of at least 300MHz.
2. R_L = 49.9Ω ±1% for PI90LV03 or 24.9Ω ±1% for PI90LVB03.
3. To verify output max signaling rate , the output signal transition time (t_r/t_f) should not exceed 0.76ns.

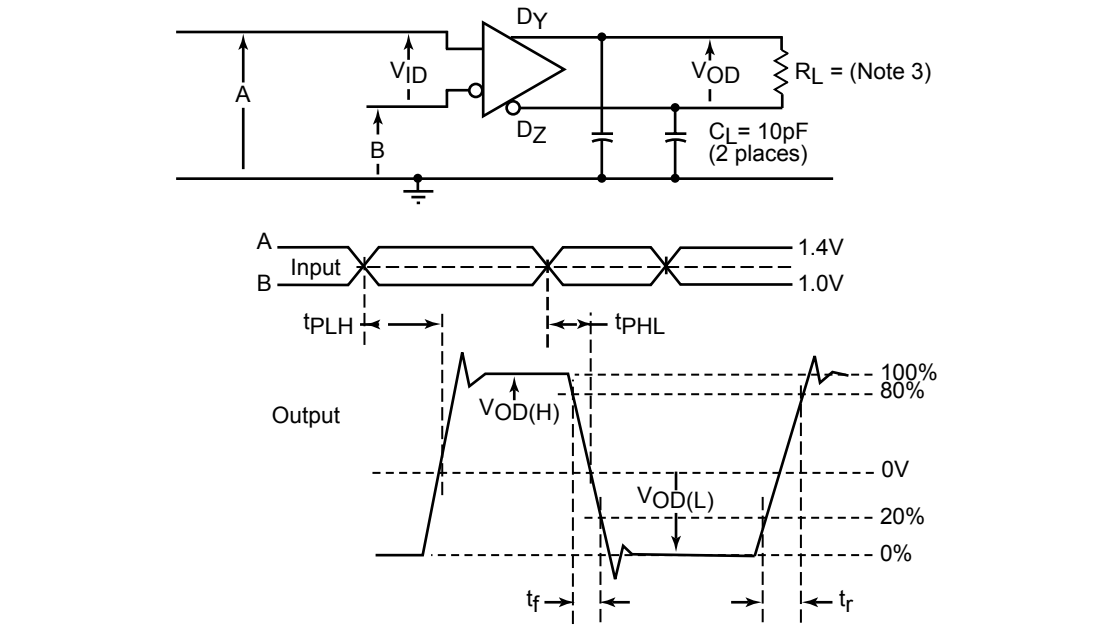
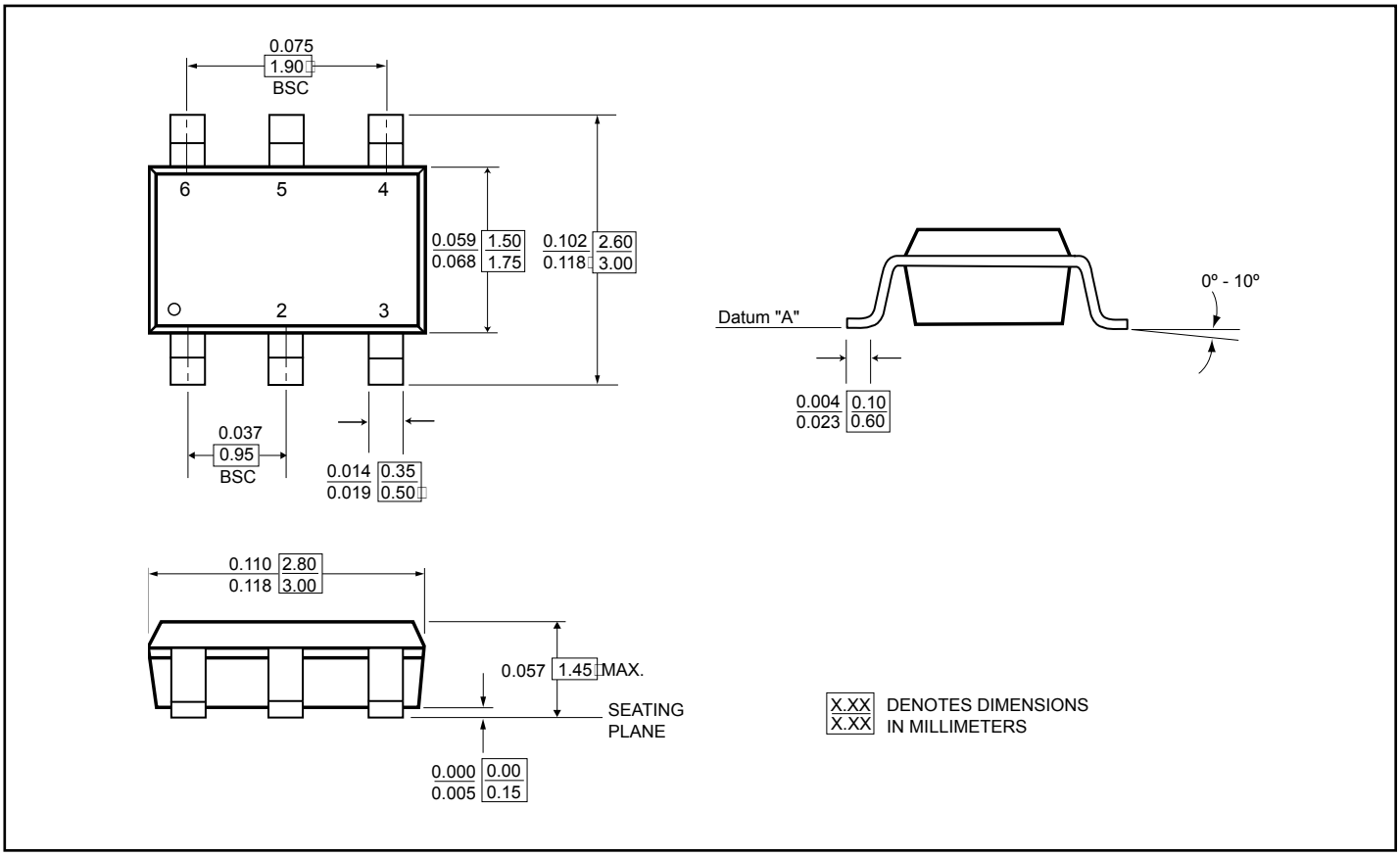


Figure 6. Test Circuit and Definitions

Notes:

1. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ns, Pulse Repetition Rate (PPR) = 50 Mpps, pulse width = 10 ±0.2ns. C_L includes instrumentation and fixture capacitance within 0.06m of the D.U.T.
2. This point is 1.4V with V_{CC} = 3.3V or 1.2V with V_{CC} = 2.7V.
3. R_L = 100Ω ±1% for PI90LV03 or 50Ω ±1% for PI90LVB03.

Packaging Mechanical: 6-Pin SOT (T)



Ordering Information

Ordering Code	Package Code	Package Description	Top Marking
PI90LV03TX	T	6-pin SOT-23	L9
PI90LV03TEX	T	Pb-free & Green, 6-pin SOT-23	LC
PI90LVB03TX	T	6-pin SOT-23	LA
PI90LVB03TEX	T	Pb-free & Green, 6-pin SOT-23	LD

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. X = Tape and reel