

Features

- Meets or Exceeds the Requirements of ANSI TIA/EIA-644-1995
- Designed for Signaling Rates up to 650 Mbit/s (325 MHz)
- Operates from a 3.3V Supply: -40°C to $+85^{\circ}\text{C}$
- Low Voltage Differential Signaling with Output Voltages of $\pm 350\text{mV}$ into:
 - 100 Ohm load (PI90LV022)
 - 50 Ohm load Bus LVDS Signaling (PI90LVB022)
- Accepts $\pm 350\text{mV}$ differential inputs
- Wide common mode input voltage range: 0.2V to 2.7V
- Output drivers are high impedance when disabled or when $V_{CC} \leq 1.5\text{V}$
- Inputs are open, short, and terminated fail safe
- Propagation Delay Time: 3.5ns
- ESD protection is 10kV on bus pins
- Bus Pins are High Impedance when disabled or with V_{CC} less than 1.5V
- TTL Inputs are 5V I/O Tolerant
- Power Dissipation at 400Mbit/s less than 150mW
- Industrial temperature rating
- Packaging (Pb-free & Green available):
 - 16-pin SOIC (W)
 - 16-pin TSSOP (L)

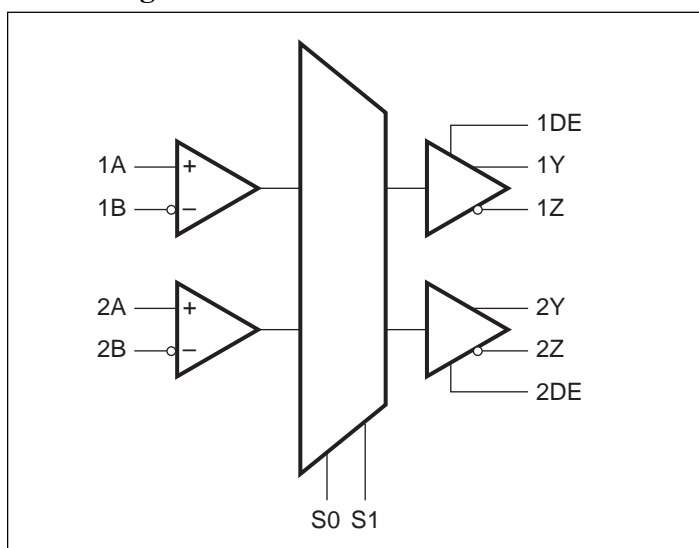
Description

The PI90LV022 and PI90LVB022 are differential line drivers and receivers that use Low Voltage Differential Signaling (LVDS) to achieve signaling rates as high as 650 Mbps. The receiver outputs can be switched to either or both drivers through the multiplexer control signals S0 and S1. This allows the flexibility to perform splitter or signal routing functions with a single device.

The LVDS standard provides a minimum differential output voltage magnitude of 247mV into a 100 Ohm load and receipt of 100mV DC signals with up to 1V of ground potential difference between a transmitter and receiver. The PI90LVB022 doubles the output drive current to achieve Bus LVDS signaling levels with a 50 Ohm load. A doubly terminated Bus LVDS line enables multi-point configurations. Switching between channels does not create false transitions on the outputs.

The intended application of these devices and signaling technique is for both point-to-point base-band (PI90LV022) and multipoint (PI90LVB022) data transmissions over controlled impedance media.

Block Diagram



Pin Configuration

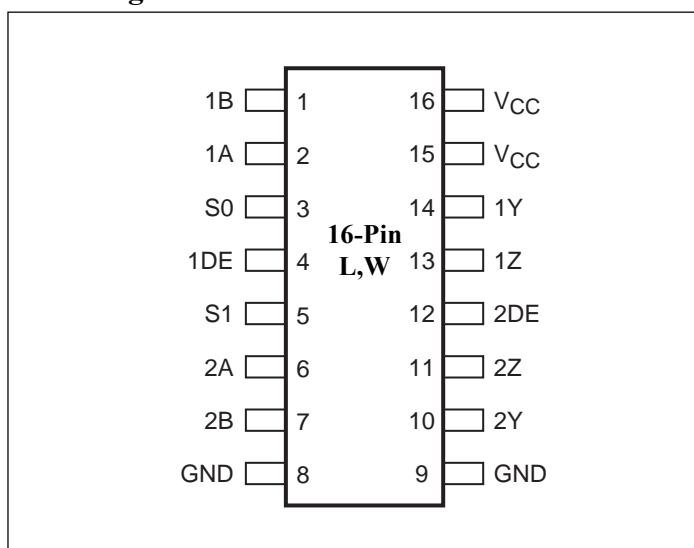


Table 1. MUX Truth Table

INPUT		OUTPUT		FUNCTION
S1	S0	1Y/1Z	2Y/2Z	
0	0	1A/1B	1A/1B	Splitter
0	1	2A/2B	2A/2B	Splitter
1	0	1A/1B	2A/2B	Router
1	1	2A/2B	1A/1B	Router

Note: Setting nDE to 0 will set Output nY/nZ to High Impedance.

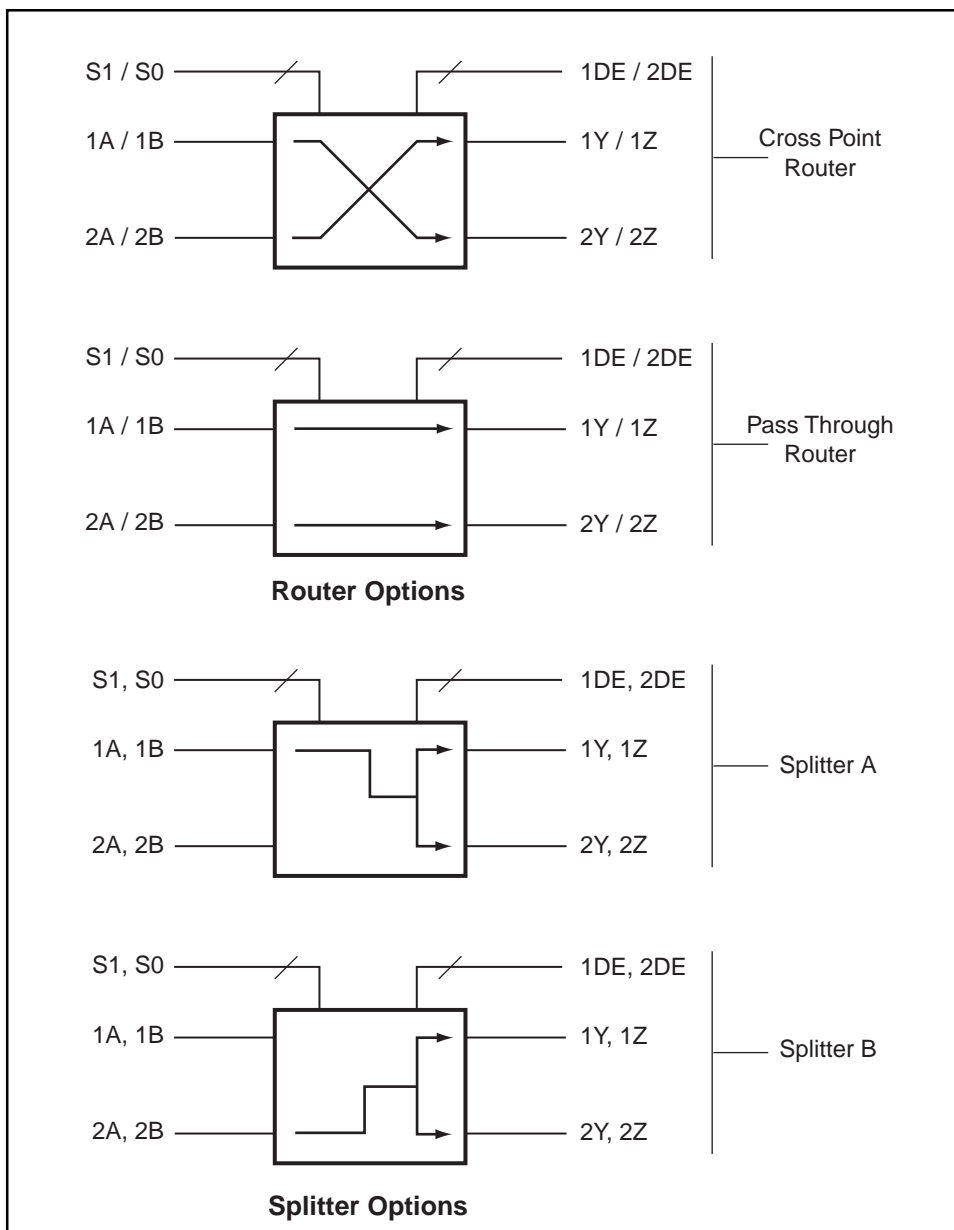


Figure 1. Possible Signal Routing

Absolute Maximum Ratings Over Operating Free-Air Temperature[†]

Supply Voltage Range, $V_{CC}^{(1)}$	-0.5V to 4V
Voltage Range (DE, S0, S1)	-0.5 to 6V
Input Voltage Range, V_I (A or B)	-0.5V to $V_{CC} + 0.5V$
Electrostatic Discharge: A, B, Y, Z, and GND ⁽²⁾	Class 3, A: 16kV, B:600V
All Pins	Class 3, A: 7kV, B:500V
Storage Temperature Range	-65°C to 150°C
Lead Temperature 1, 6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability.

Notes:

1. All voltage values, except differential I/O bus voltages, are with respect to ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7

Recommended Operating Conditions

		Min.	Nom.	Max.	Units
Supply Voltage, V_{CC}		3.0	3.3	3.6	V
High-Level Input Voltage, V_{IH}	S0, S1, 1DE, 2DE	2			
Low-Level Input Voltage, V_{IL}	S0, S1, 1DE, 2DE			0.8	
Magnitude of Differential Input Voltage $ V_{ID} $		0.1		0.6	
Common-Mode input Voltage, V_{IC} (see Figure 2)		$\frac{ V_{ID} }{2}$		$2.4 - \frac{ V_{ID} }{2}$	
				$V_{CC} - 0.8$	
Operating free-air temperature, T_A		-40		85	°C

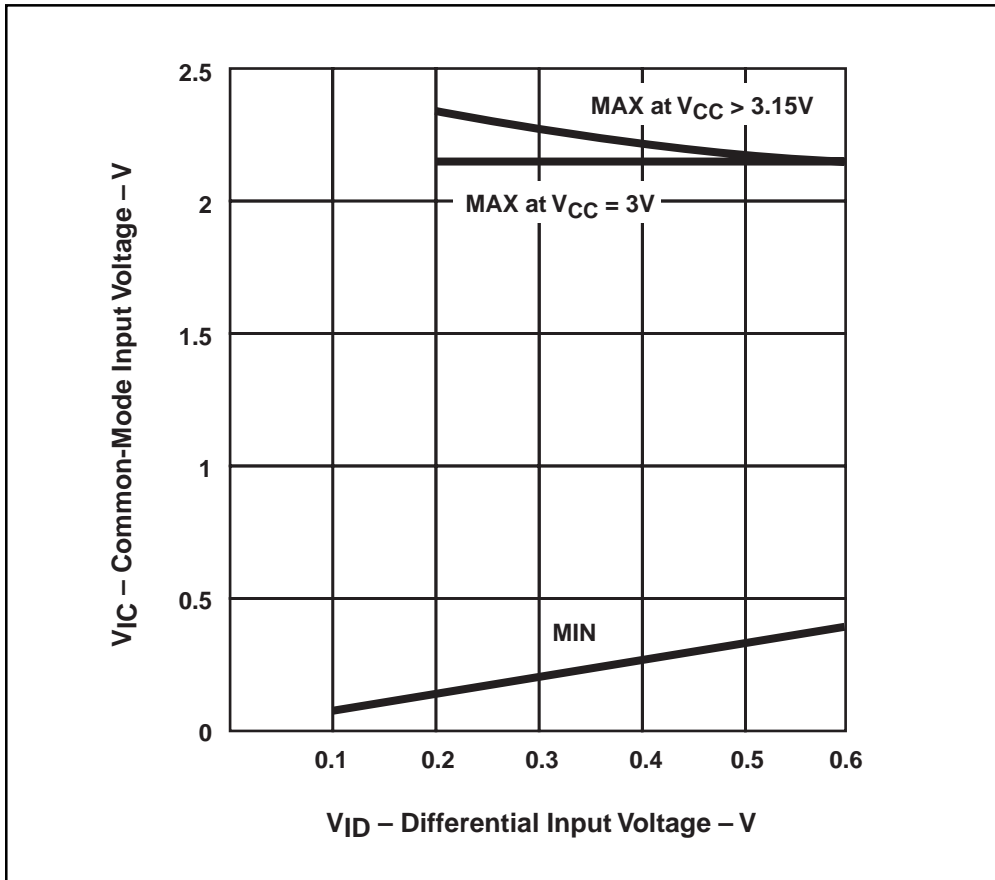


Figure 2. Common-Mode Input Voltage vs. Differential Voltage

Receiver Electrical Characteristics Over Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Units
V_{ITH+}	Positive-going differential input voltage threshold	$V_{CM} = 1.2V$			100	mV
V_{ITH-}	Negative-going differential input voltage threshold		-100			
I_I	Input current (A or B inputs)	$V_I = 0V$	-2		-20	μA
		$V_I = 2.4V$	-1.2			
$I_I (OFF)$	Power-off input current (A or B inputs)	$V_{CC} = 0V$			20	

Receiver/Driver Electrical Characteristics Over Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter		Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Units
V_{OD}	Differential output voltage magnitude		$R_L = 100 \text{ Ohm}$ (LV022)	See Fig. 3	247	440	590	mV
ΔV_{OD}	Change in differential output voltage magnitude between logic states				-50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage		$R_L = 50 \text{ Ohm}$ (LVB022)	See Fig. 4	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states				-50	3	50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage						150	
I_{CC}	Supply current		No Load			8	12	mA
			$R_L = 100 \text{ Ohm}$ (LV022)			13	20	
			$R_L = 50 \text{ Ohm}$ (LVB022)			21	27	
			Both Channels Disabled			3	6	
I_{IH}	High-level input current	DE	$V_{IH} = 5$				40	nA
		S0, S1					-3	μA
I_{IL}	Low-level input current	DE	$V_{IL} = 0.8\text{V}$				-20	nA
		S0, S1					10	μA
I_{OS}	Short-circuit output current		$V_{OY} \text{ or } V_{OZ} = 0\text{V},$ $V_{OD} = 0\text{V}$ (LV022)				-10	mA
							-10	
			$V_{OY} \text{ or } V_{OZ} = 0\text{V},$ $V_{OD} = 0\text{V}$ (LVB022)				-10	
							-10	
I_{OZ}	High-Impedance output current		$V_{OD} = 600\text{mV}$			1.5	± 25	nA
			$V_O = 0\text{V}$ or V_{CC}			1.5	± 25	
			$V_{CC} = 0\text{V}, V_O = 3.6\text{V}$			1.5	± 40	
$I_{O(OFF)}$	Power-off output current					1.5	± 40	
C_{IN}	Input capacitance					3		pF
			S0, S1, 1DE, 2DE			8		

Note:

1. All typical values are at 25°C and with a 3.3 supply

Differential Receiver to Driver Switching Characteristics Over Recommended Operating Conditions

(unless otherwise noted)

Symbol	Parameter		Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Units
t _{PLH}	Differential propagation delay, low-to-high		C _L = 10pF (See Fig. 5)		4.0	6.0	ns
t _{PHL}	Differential propagation delay, high-to-low				4.0	6.0	
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})				0.2	–	
t _r	Transition, low-to-high	PI90LV022			0.9	1.5	
t _r	Transition, low-to-high	PI90LVB022			0.6	1.3	
t _r	Transition, high-to-low	PI90LV022			0.8	1.5	
t _r	Transition, high-to-low	PI90LVB022			0.5	1.3	
t _{PHZ}	Propagation delay time, high-level-to-high-impedance output		(See Fig. 6)		4.0	10	
t _{PLZ}	Propagation delay time, low-level-to-high-impedance output				4.3	10	
t _{PZH}	Propagation delay time, high-impedance-to-high-level output				3.0	10	
t _{PZL}	Propagation delay time, high-impedance-to-low-level output				2.0	10	
t _{PHL_R1_Dx}	Channel-to-channel skew, receiver to driver ⁽²⁾				95		ps
t _{PLH_R1_Dx}					95		
t _{PHL_R2_Dx}					95		
t _{PLH_R2_Dx}					95		

Notes:

1. All typical values are at 25°C and with a 3.3 supply.
2. These parametric values are measured over supply voltage and temperature ranges recommended for the device.

Parameter Measurement Information

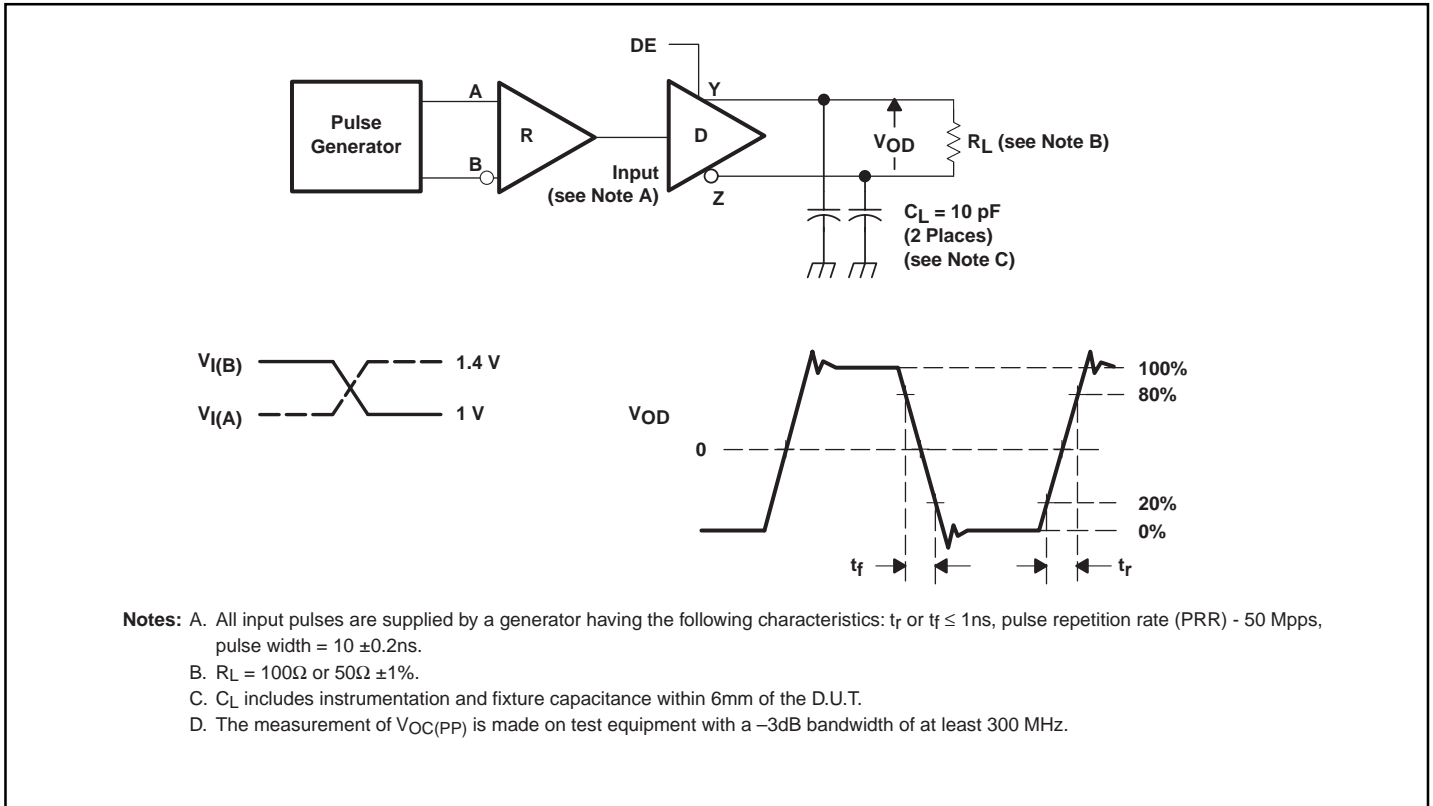


Figure 3. Test Circuit and Voltage Definitions for the Differential Output Signal

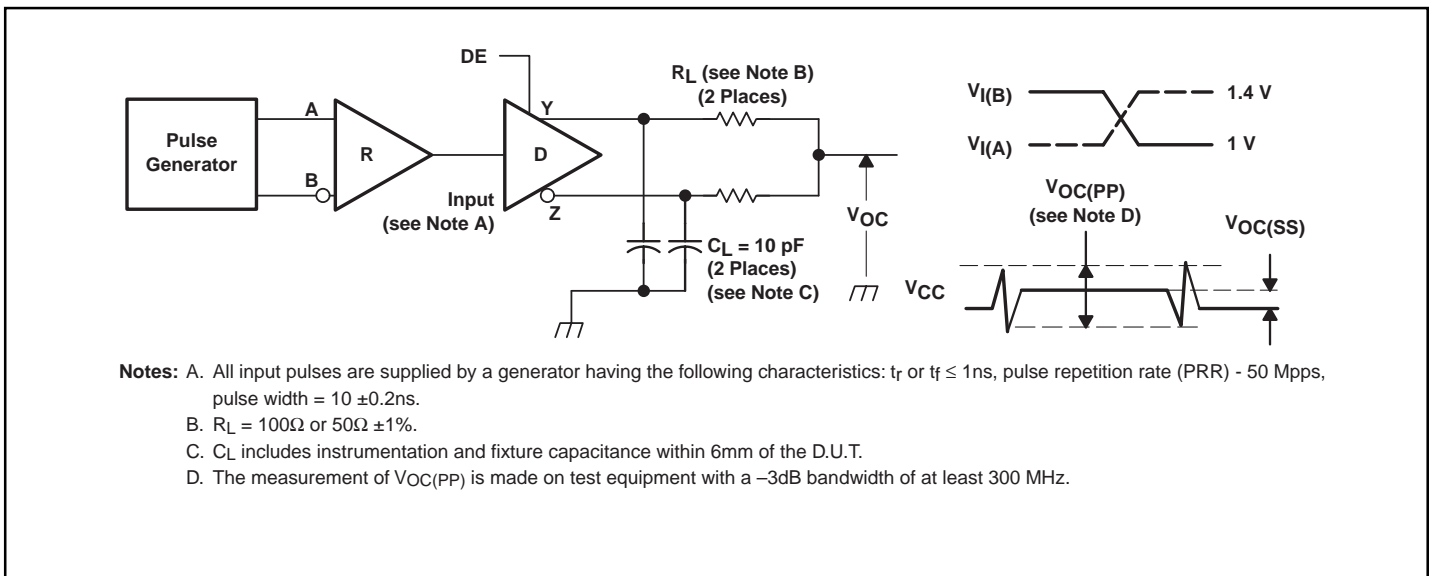


Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

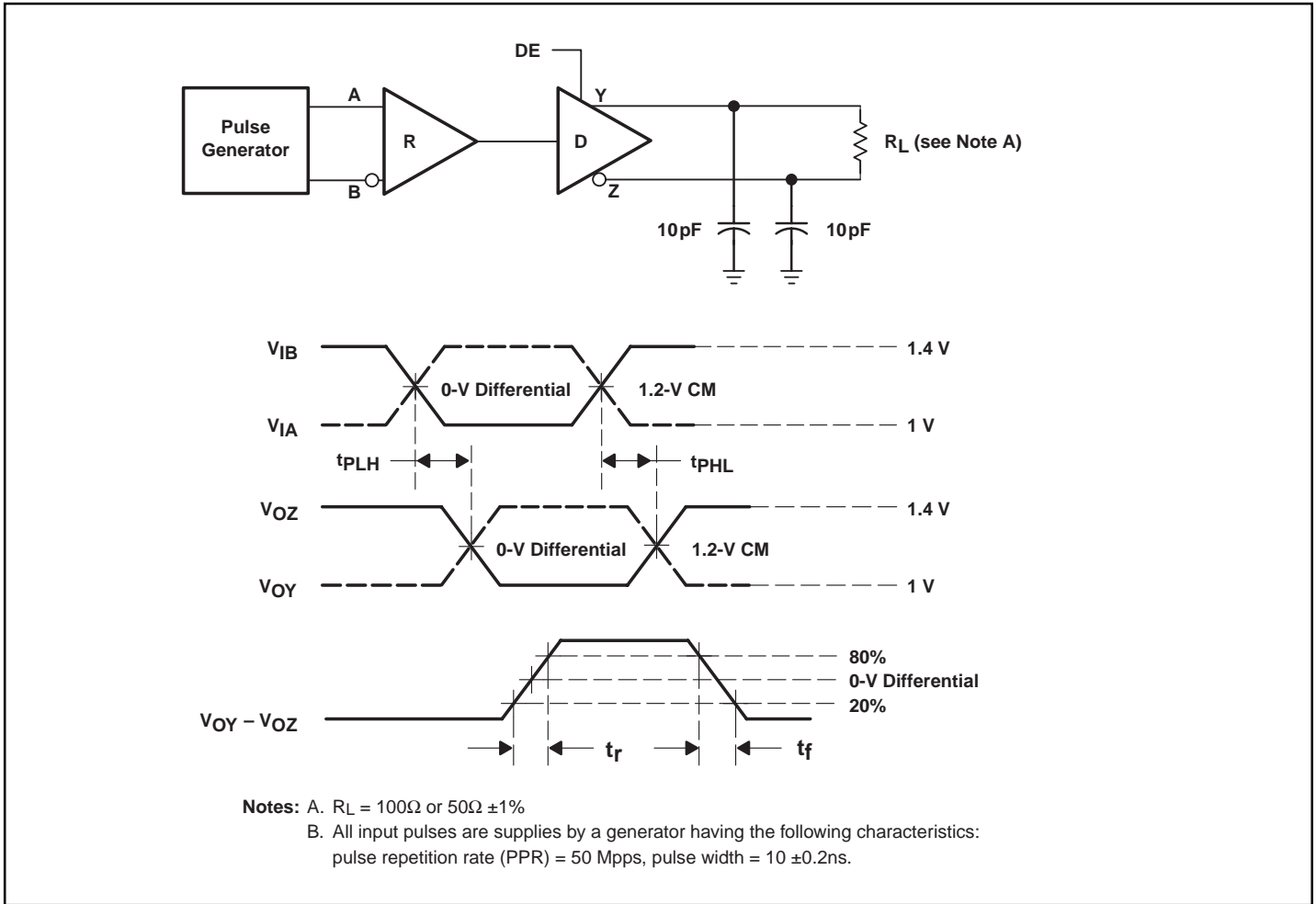


Figure 5. Differential Receiver to Driver Propagation Delay and Driver Transition Time Waveforms

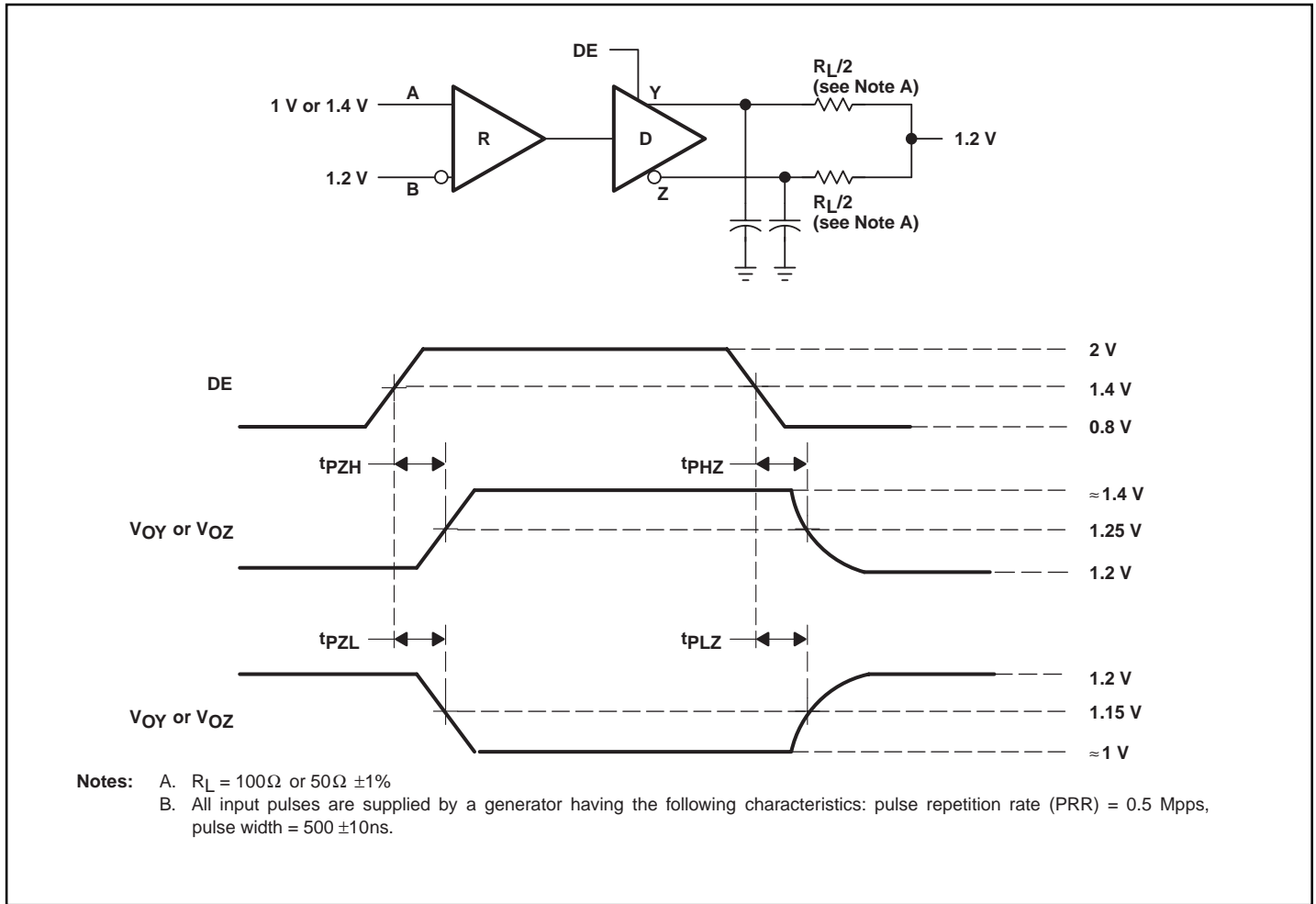
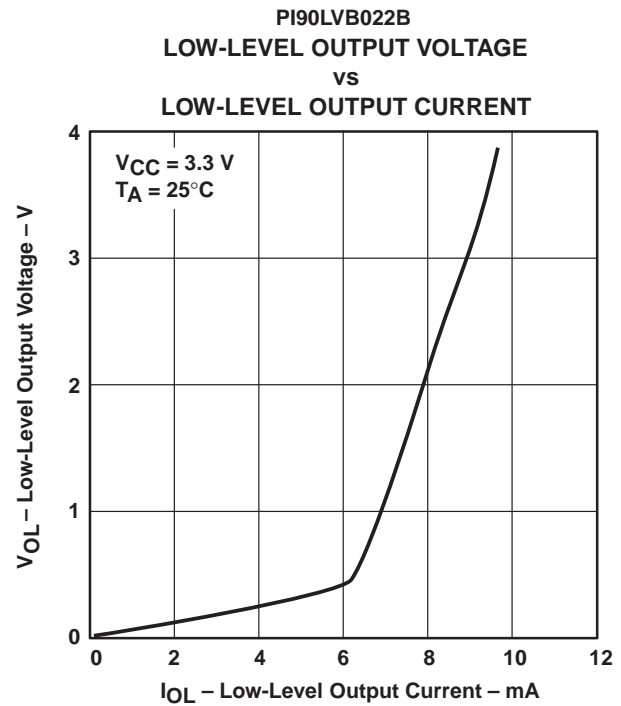
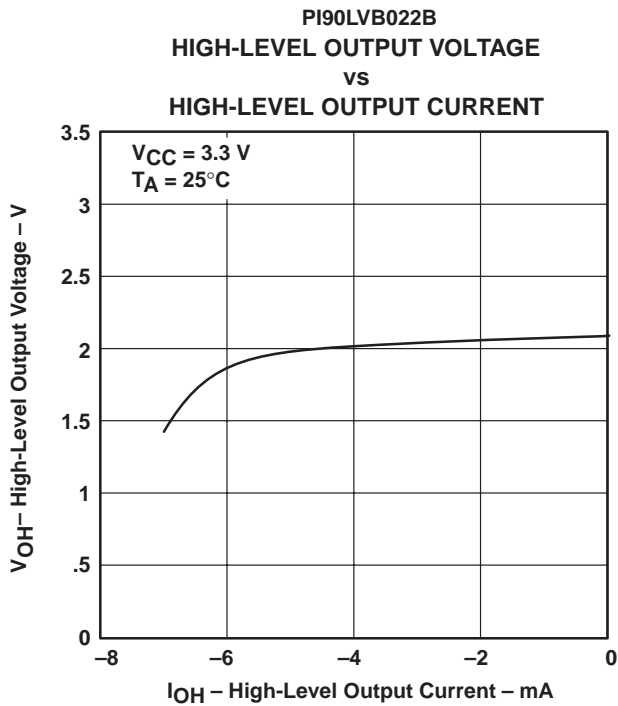
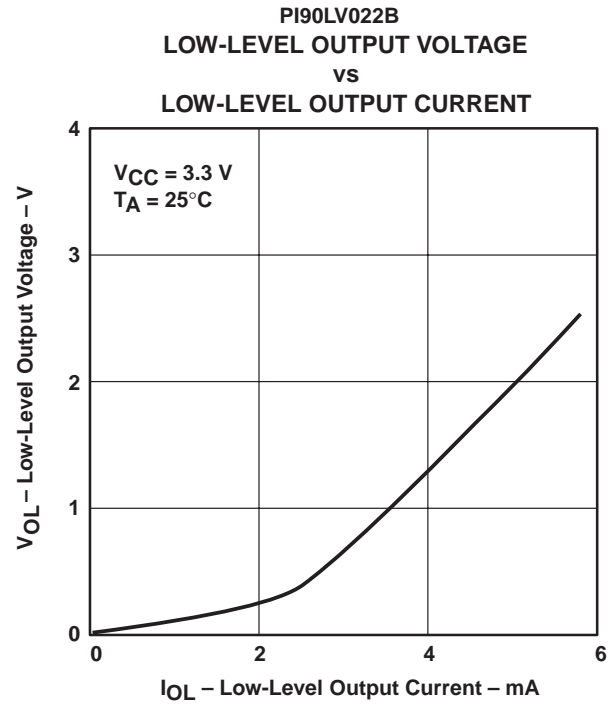
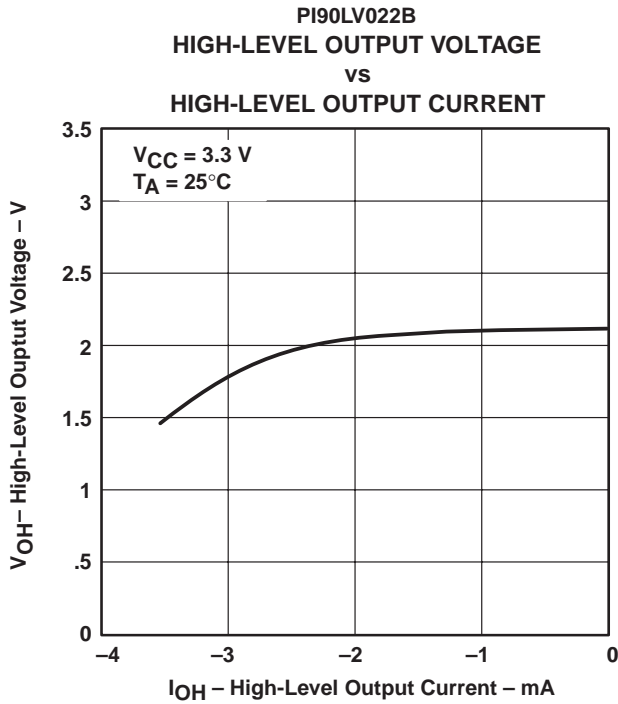
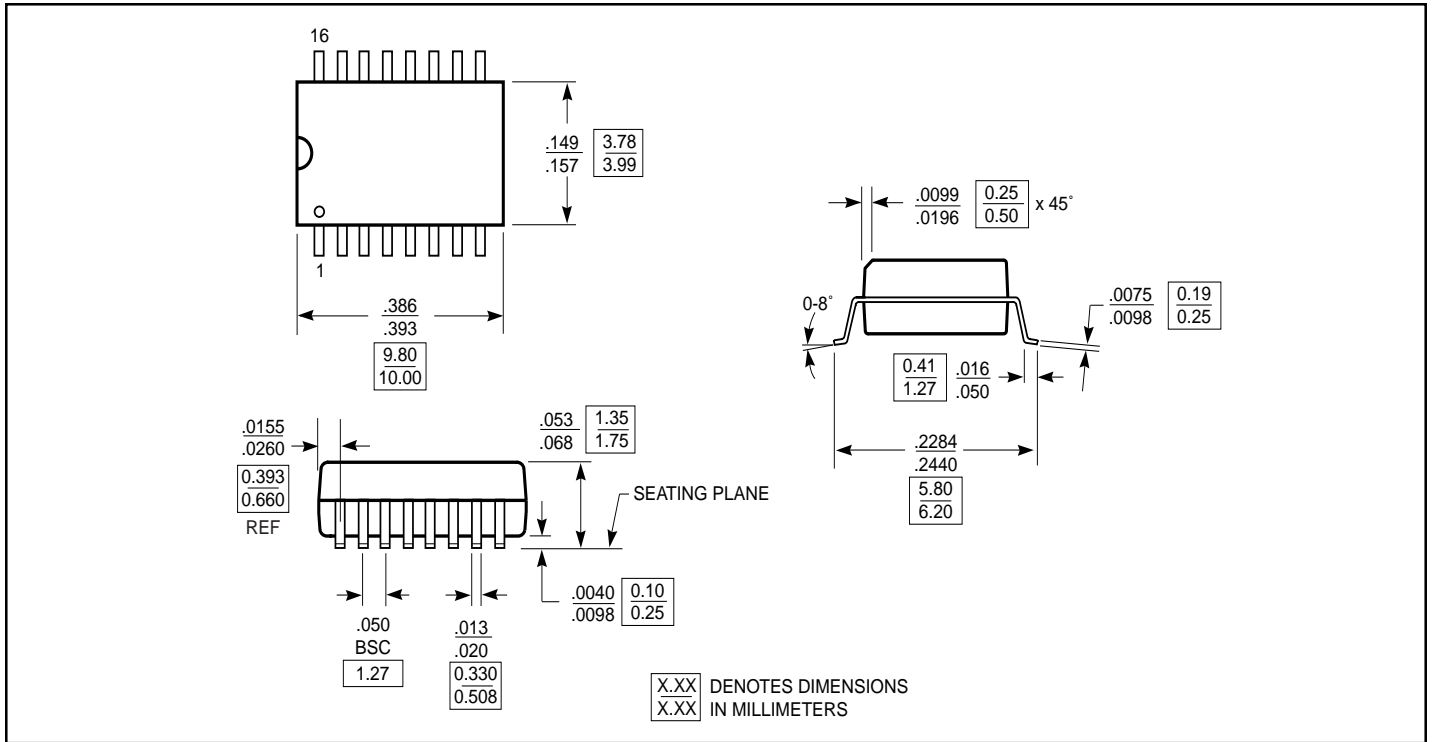


Figure 6. Enable and Disable Timing Circuit

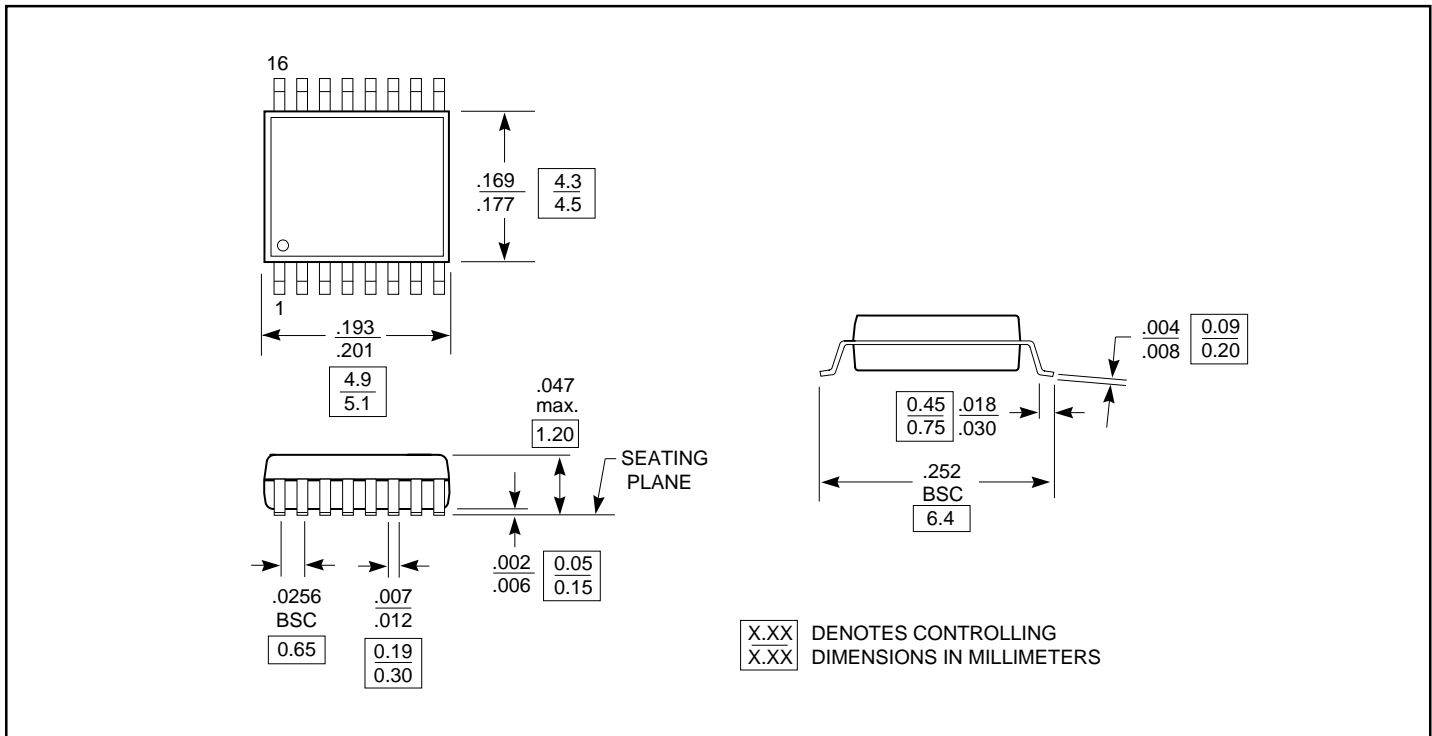
Typical Characteristics



Packaging Mechanical: 16-Pin SOIC (W)



Packaging Mechanical: 16-Pin TSSOP (L)



Ordering Information

Ordering Code	Package Code	Package Description
PI90LV022W	W	16-pin 150-mil SOIC
PI90LV022WE	W	Pb-free & Green, 16-pin 150-mil SOIC
PI90LV022L	L	16-pin 173-mil TSSOP
PI90LV022LE	L	Pb-free & Green, 16-pin 173-mil TSSOP
PI90LVB022W	W	16-pin 150-mil SOIC
PI90LVB022WE	W	Pb-free & Green, 16-pin 150-mil SOIC
PI90LVB022L	L	16-pin 173-mil TSSOP
PI90LV0B22LE	L	Pb-free & Green, 16-pin 173-mil TSSOP

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/