

**3V LVDS High-Speed  
Differential Line Receivers**

**Features**

- Signaling Rates >400Mbps (200 MHz)
- Single 3.3V Power Supply Design
- Accepts  $\pm 350\text{mV}$  (typical) Differential Swing
- Maximum Differential Skew of 0.35ns
- Maximum Propagation Delay of 3.3ns
- Low Voltage TTL (LVTTTL) Outputs
- Industrial Temperature Operating Range:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- Open, Short, and Terminated Fail Safe
- Meets or Exceeds IEEE 1596.3 SCI Standard
- Meets or Exceeds ANSI/TIA/EIA-644 LVDS Standard
- Packaging (Pb-free & Green available):  
- SOIC, TSSOP, and MSOP

**Description**

The PI90LV032A, PI90LV028A, and PI90LV018A are differential line receivers that use low-voltage differential signaling (LVDS) to support data rates in excess of 400 Mbps. These products are designed for applications requiring high-speed, low-power consumption and low noise generation.

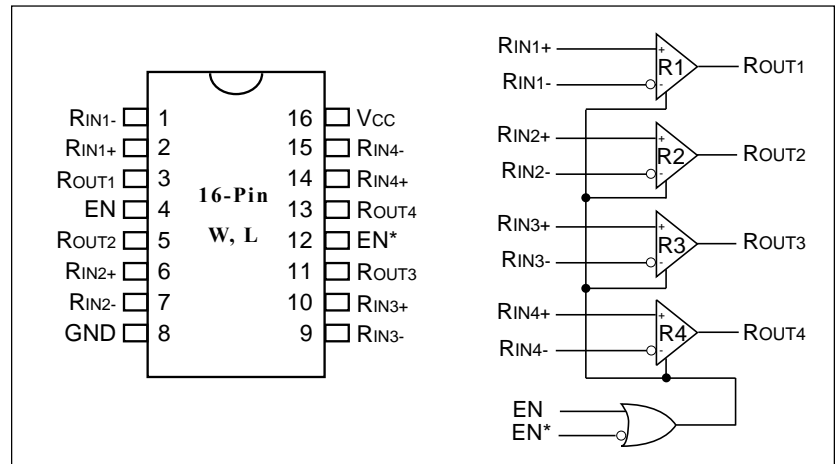
A differential input signal (350mV) is translated by the device to 3V CMOS output level. Exclusive to the PI90LV032A quad receiver is a power-down mode that Three-states the outputs and places the device in a low-power idle state (40mW typical).

**Applications**

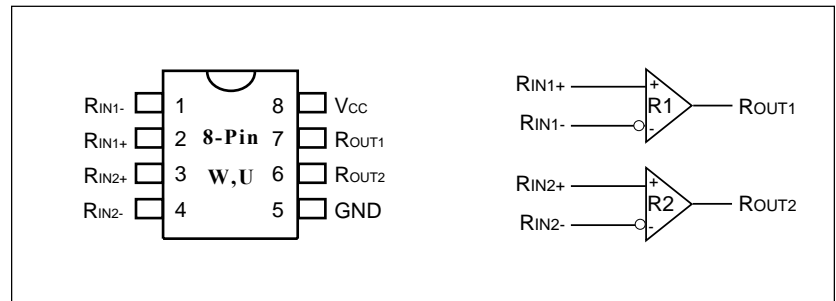
Applications include point-to-point and multidrop baseband data transmission over controlled impedance media of approximately 100 Ohms. The transmission media can be printed circuit board traces, backplanes, or cables.

The PI90LV032A, PI90LV028A, PI90LV018A and companion line drivers (PI90LV031A, PI90LV027A, and PI90LV017A) provide new alternatives to RS-232, PECL, and ECL devices for high-speed, point-to-point interface applications.

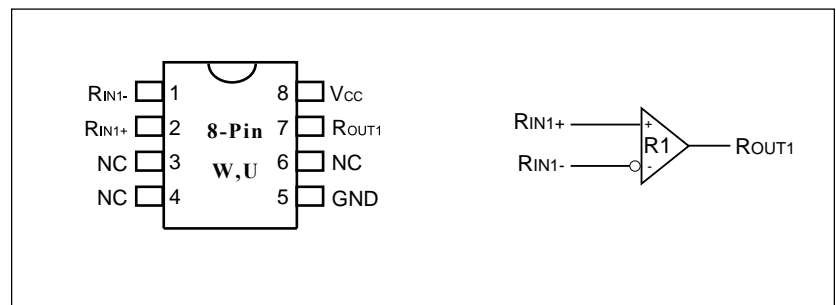
**PI90LV032A**



**PI90LV028A**



**PI90LV018A**



## Function Tables

### PI90LV032A

Enables		Inputs		Output
EN	EN*	R <sub>IN+</sub>	R <sub>IN-</sub>	R <sub>OUT</sub>
H	X	H	L	H
H	X	L	H	L
X	L	H	L	H
X	L	L	H	L
L	H	X	X	Z

### PI90LV028A

Inputs		Output
R <sub>IN+</sub>	R <sub>IN-</sub>	R <sub>OUT</sub>
H	L	H
L	H	L

### PI90LV018A

Inputs		Output
R <sub>IN+</sub>	R <sub>IN-</sub>	R <sub>OUT</sub>
H	L	H
L	H	L

## Recommended Operating Conditions

	Min.	Typ.	Max.	Units
Supply Voltage (V <sub>CC</sub> )	+3.0	+3.3	+3.6	V
Receiver Input Voltage	GND		+3.0	
Operating Free Air Temperature (T <sub>A</sub> )	-40	+25	+85	°C

## Pin Descriptions

Name	Description
R <sub>OUT</sub>	TTL/CMOS receiver output pins
R <sub>IN+</sub>	Non-inverting receiver input pins
R <sub>IN-</sub>	Inverting receiver input pins
GND	Ground pin
V <sub>CC</sub>	Positive power supply pin, +3.3V ±10%

## Absolute Maximum Ratings (see Note 1, Page 4)

Supply Voltage (V <sub>CC</sub> )	-0.3V to +4.0V
Input Voltage (R <sub>IN+</sub> , R <sub>IN-</sub> )	-0.3V to +3.9V
Enable Input Voltage (EN, EN*)	-0.3V to (V <sub>CC</sub> +0.3V)
Output Voltage (R <sub>OUT</sub> )	-0.3V to (V <sub>CC</sub> +0.3V)
S Package	750mW
Derate S Package	8.2mW/°C above +25°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range Soldering (4s)	+260°C
Maximum Junction Temperature	+150°C
ESD Rating	≥6kV

### Note:

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Electrical Characteristics**

Over supply voltage and operating temperature ranges, unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions	Pin	Min.	Typ.	Max.	Units	
$V_{TH}$	Differential Input High Threshold	$V_{cm} = +1.2V(12)$	$R_{IN+}, R_{IN-}$		+20	+100	mV	
$V_{TL}$	Differential Input Low Threshold			-100	-20			
$V_{CMR}$	Common-Mode Voltage Range	$V_{ID} = 200mV$ peak-to-peak(5)		0.1		2.3	V	
$I_{IN}$	Input Current	$V_{IN} = +2.8V$		$V_{CC} = +3.6$ or $0V$	-10	$\pm 1$	+10	$\mu A$
		$V_{IN} = 0V$			-10	$\pm 1$	+10	
		$V_{IN} = +3.6V$		$V_{CC} = 0V$	-20		+20	
$V_{OH}$	Output High Voltage	$I_{OH} = -0.4mA, V_{ID} = +200mV$	$R_{OUT}$	2.7	3.0		V	
		$I_{OH} = -0.4mA$ , Input terminated		2.7	3.0			
		$I_{OH} = -0.4mA$ , Input shorted		2.7	3.0			
$V_{OL}$	Output Low Voltage	$I_{OL} = 2mA, V_{ID} = -200mV$			0.1	0.25		
$I_{OS}$	Output Short Circuit Current	Enabled, $V_{out} = 0V(10)$		-15	-48	-120		mA
$I_{OZ}$	Output Three-State Current	Disabled, $V_{OUT} = 0V$ or $V_{CC}$		-10	$\pm 1$	+10		$\mu A$
$V_{IH}$	Input High Voltage		$EN, EN^*$	2.0		$V_{CC}$	V	
$V_{IL}$	Input Low Voltage			GND		0.8		
$I_I$	Input Current	$V_{IN} = 0V$ or $V_{CC}$ , Other Input = $V_{CC}$ or GND		-10	$\pm 1$	+10	$\mu A$	
$V_{CL}$	Input Clamp Voltage	$I_{CL} = -18mA$		-1.5	-0.8		V	
$I_{CC}$	No Load Supply Current Receivers Enabled	$EN, EN^* = V_{CC}$ or GND, Inputs Open	$V_{CC}$		10	15	mA	
		$EN, EN^* = 2.4V$ or $0.5V$ , Inputs Open			10	15		
$I_{CCZ}$	No Load Supply Current Receivers Disabled	$EN = GND, EN^* = V_{CC}$ , Inputs Open			7	10		

## Switching Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified. (Notes 3,4,7,8)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t <sub>PHLD</sub>	Differential Propagation Delay High to Low (V <sub>CM</sub> = 1.2V)	C <sub>L</sub> = 10pF V <sub>ID</sub> = 200mV (Figures 1 & 2)	1.8		4.7	ns
t <sub>PLHD</sub>	Differential Propagation Delay Low to High (V <sub>CM</sub> = 1.2V)		1.8		4.7	
t <sub>SKD1</sub>	Differential Pulse Skew   t <sub>PHLD</sub> - t <sub>PLHD</sub>   <sup>(6)</sup>		0	0.1	0.35	
t <sub>SKD2</sub>	Differential Channel-to-Channel Skew-same device <sup>(7)</sup>		0	0.1	0.5	
t <sub>SKD3</sub>	Differential Part-to-Part Skew <sup>(8)</sup>				1.0	
t <sub>SKD4</sub>	Differential Part-to-Part Skew <sup>(9)</sup>				1.5	
t <sub>TLH</sub>	Rise Time			0.35	1.2	
t <sub>THL</sub>	Fall Time		0.35	1.2		
t <sub>PHZ</sub>	Disable Time High to Z	R <sub>L</sub> = 2KΩ		8	12	
t <sub>PLZ</sub>	Disable Time Low to Z	C <sub>L</sub> = 10pF (Figures 3 & 4)		6	12	
t <sub>PZH</sub>	Enable Time Z to High			11	17	
t <sub>PZL</sub>	Enable Time Z to Low			11	17	
t <sub>MAX</sub>	Maximum Operating Frequency <sup>(13)</sup>	All channels switching	200	250		MHz

### Notes:

- “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” specifies conditions of device operation.
- Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.
- All typicals are given for: V<sub>CC</sub> = +3.3V, T<sub>A</sub> = +25°C.
- Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z<sub>O</sub> = 50Ω, t<sub>R</sub> and t<sub>F</sub> (0% to 100%) ≤ 3ns for R<sub>IN</sub>.
- The VCMR range is reduced for larger VID. Example : if VID = 400mV, the VCMR is 0.2V to 2.2V. The fail-safe condition with inputs shorted is valid over a common-mode range of 0V to 2.3V. A VID up to V<sub>CC</sub> - 0V may be applied to the R<sub>IN+</sub> / R<sub>IN-</sub> inputs with the Common-Mode voltage set to V<sub>CC</sub>/2. Propagation delay and Differential Pulse skew decrease when VID is increased from 200mV to 400mV. Skew specifications apply for 200mV ≤ VID ≤ 800mV over the common mode range.
- tskd1 is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
- t<sub>SKD2</sub>, Channel-to-Channel Skew, is defined as the difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.
- t<sub>SKD3</sub>, Part-to-Part Skew, is the differential Channel-to-Channel skew of any event between devices. This specification applies to devices at the same V<sub>CC</sub>, and within 5°C of each other within the operating temperature range.
- t<sub>SKD4</sub>, Part-to-Part Skew, is the differential Channel-to-Channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. tskd4 is defined as I<sub>Max</sub> - Mini differential propagation delay.
- Output short circuit current (I<sub>OS</sub>) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.
- C<sub>L</sub> includes probe and jig capacitance.
- V<sub>CC</sub> is always higher than R<sub>IN+</sub> and R<sub>IN-</sub> voltage. R<sub>IN-</sub> and R<sub>IN+</sub> are allowed to have a voltage range -0.2V to V<sub>CC</sub> - VID/2. However, to be compliant with AC specifications, the common voltage range 0.1V to 2.3V.
- f<sub>max</sub> generator input conditions: t<sub>R</sub> = t<sub>F</sub> < 1ns, (0% to 100%), 50% duty cycle, differential (1.05V to 1.35V peak to peak). Output Criteria: duty cycle = 60%/40%, V<sub>OL</sub> (max 0.4V), V<sub>OH</sub> (min 2.7V), Load = 10pF (stray plus probes).

Parameter Measurement Information

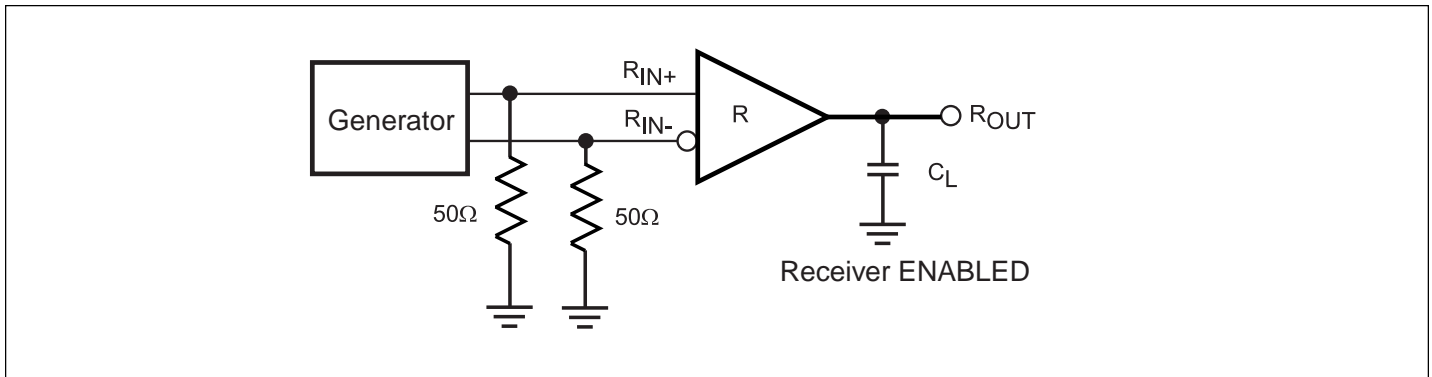


Figure 1. Receiver Propagation Delay and Transition Time Test Circuit

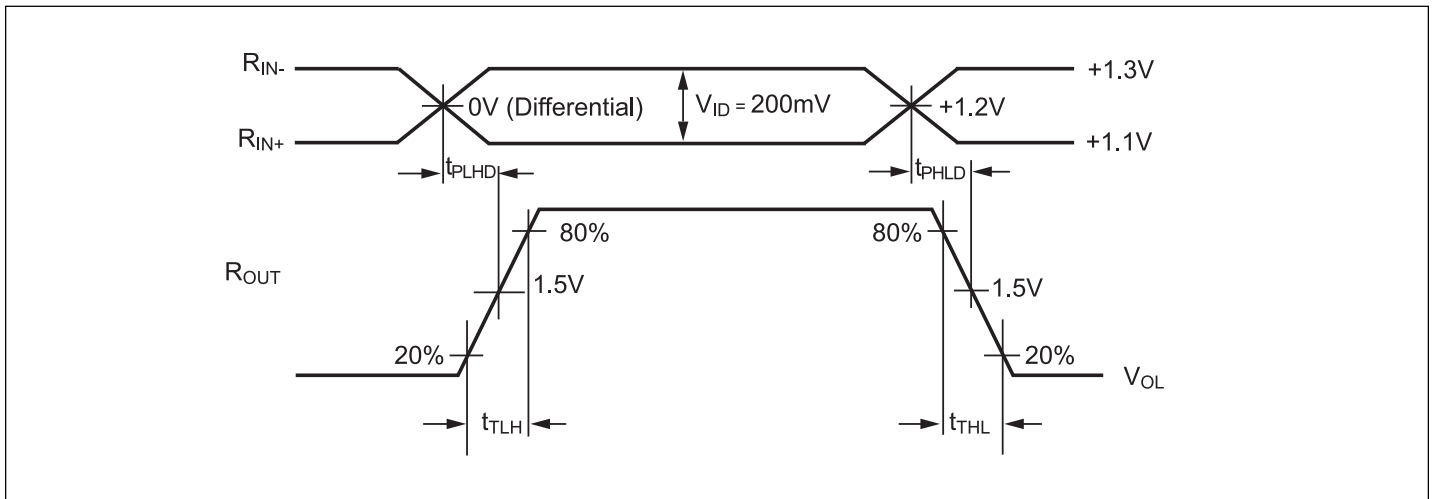


Figure 2. Receiver Propagation Delay and Transition Time Waveforms

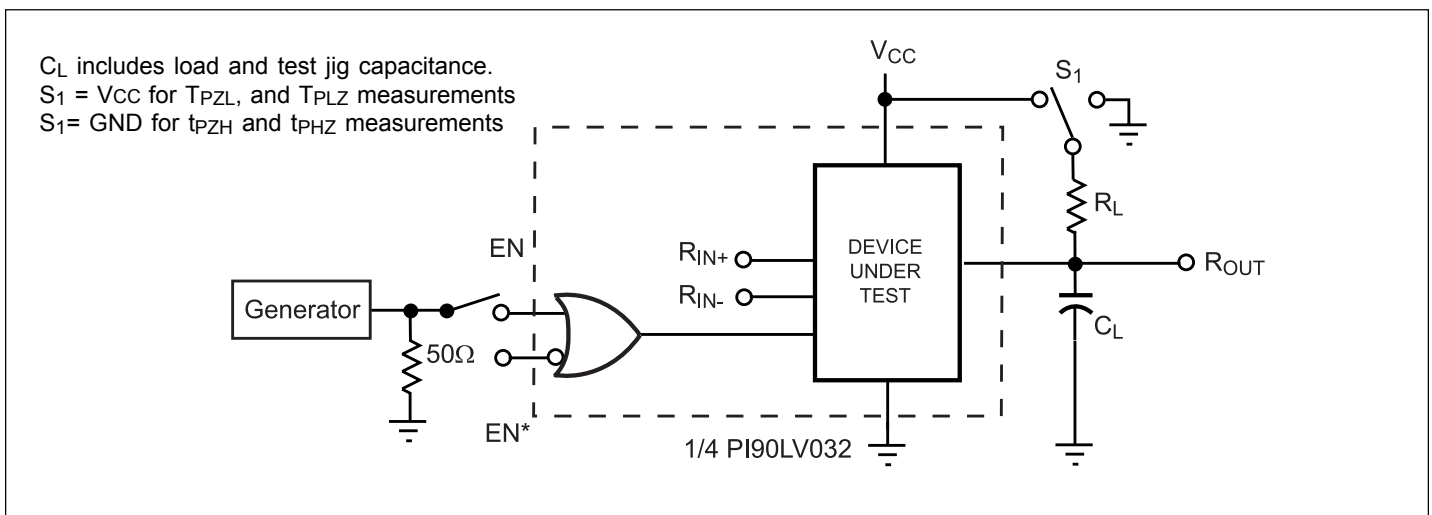


Figure 3. Receiver Three-STATE Delay Test Circuit

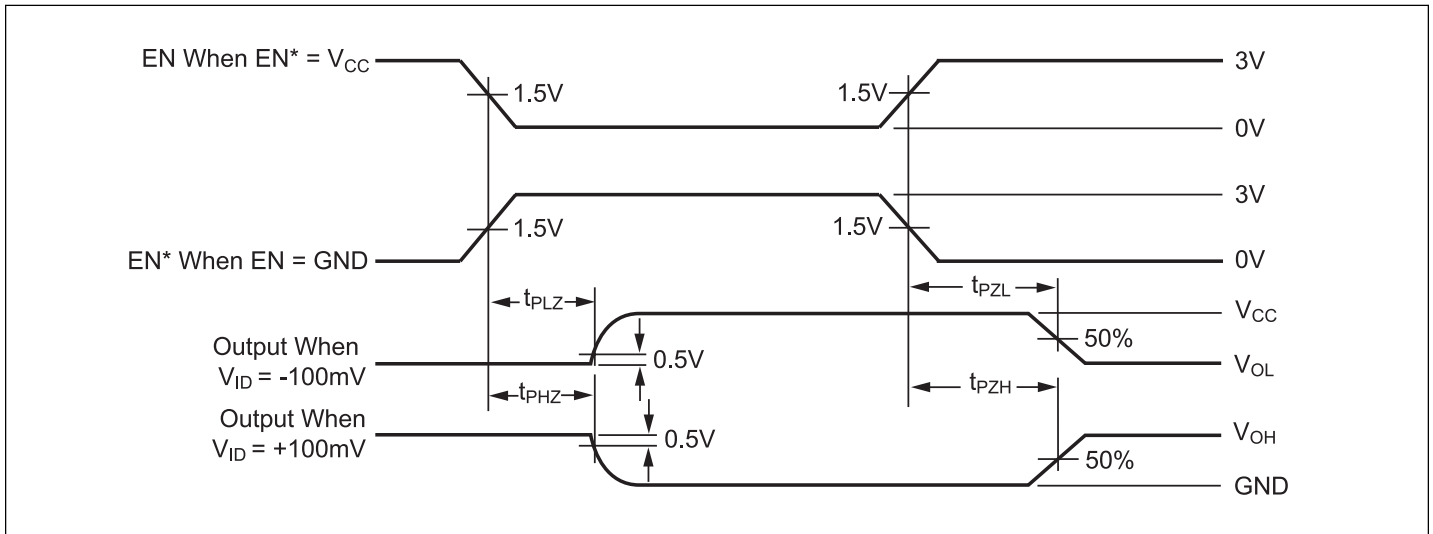


Figure 4. Receiver Three-STATE Delay Waveforms

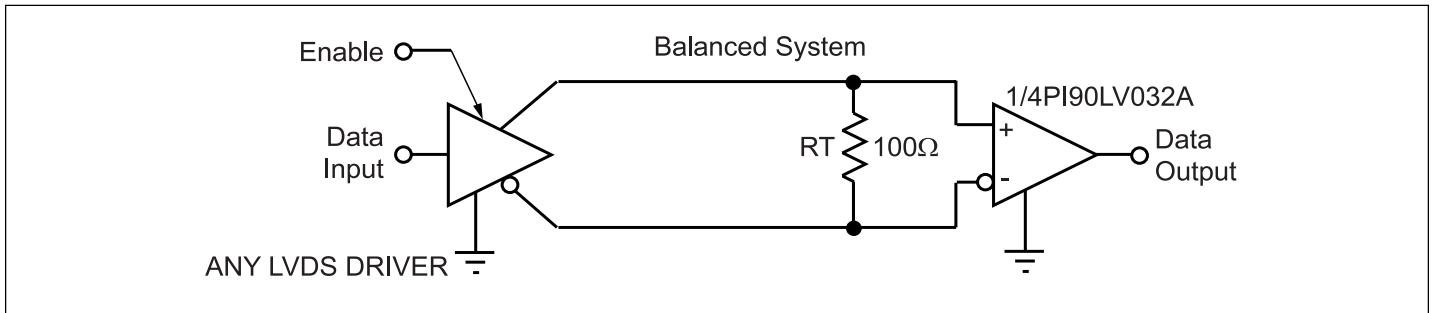
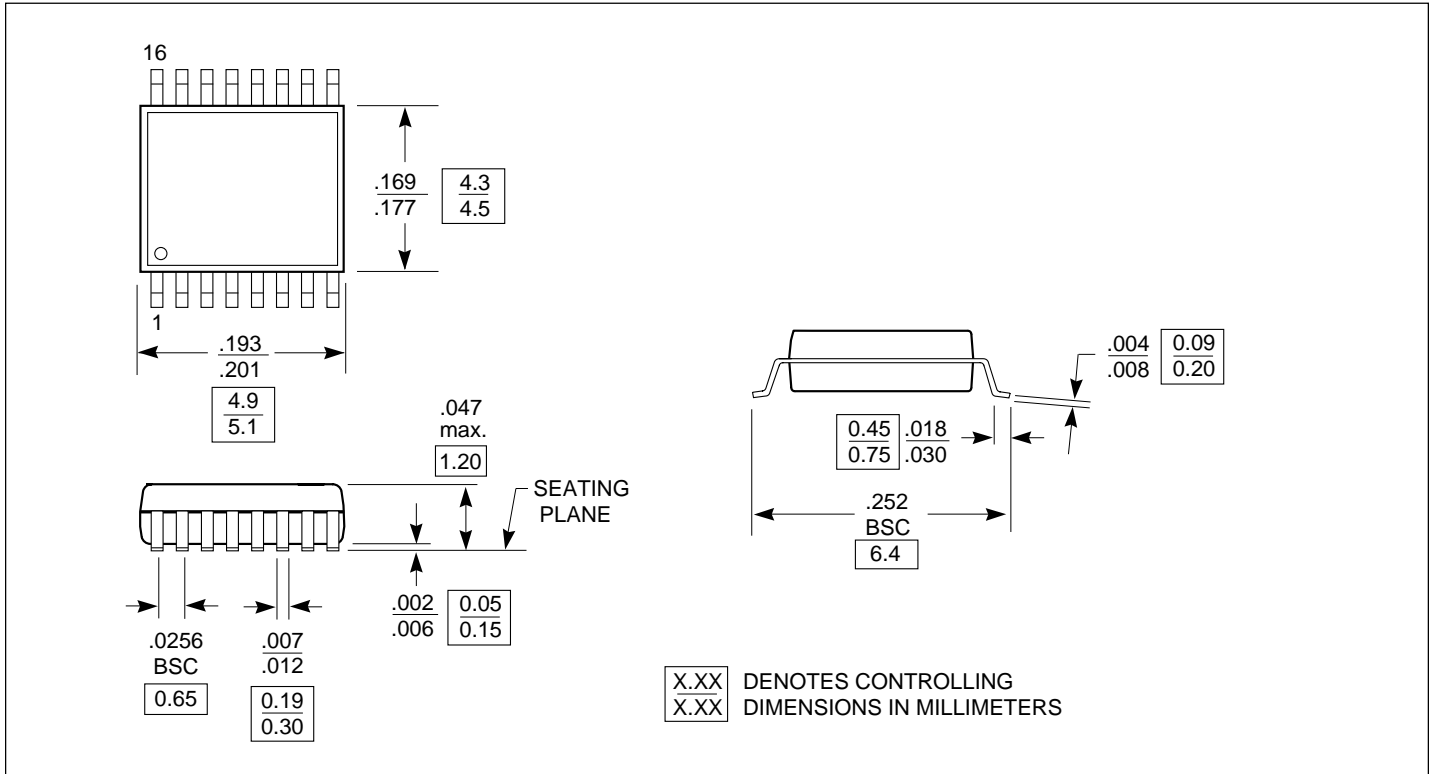


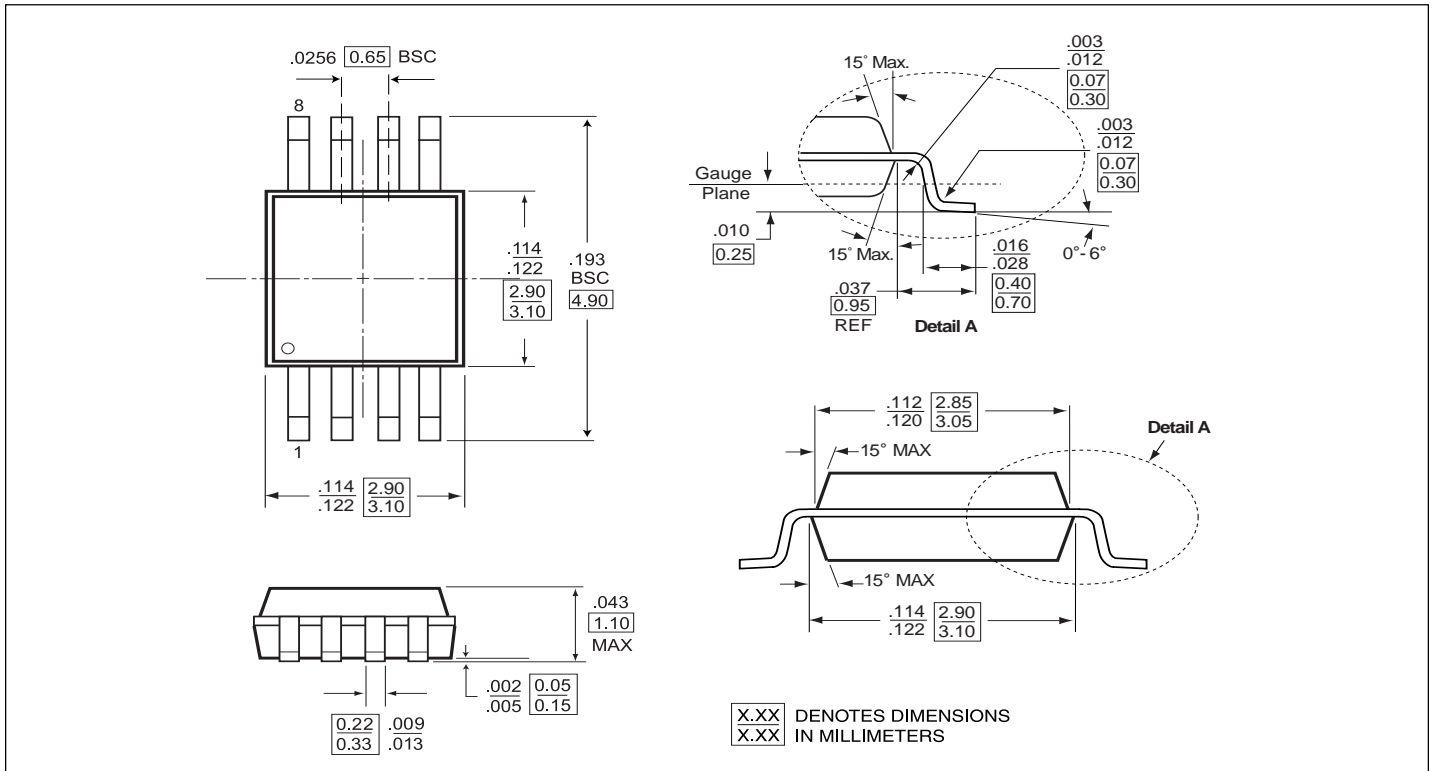
Figure 5. Point-to-Point Application



Packaging Mechanical: 16-Pin TSSOP (4.4mm wide) - L



Packaging Mechanical: 8-Pin Mini Small Outline (MSOP) - U





**Ordering Information**

Ordering Code	Package Code	Package Description
PI90LV032AW	W	16-pin SOIC
PI90LV032AWE	W	Pb-free & Green, 16-pin SOIC
PI90LV032AL	L	16-pin TSSOP
PI90LV032ALE	L	Pb-free & Green, 16-pin TSSOP
PI90LV028AW	W	8-pin SOIC
PI90LV028AWE	W	Pb-free & Green, 8-pin SOIC
PI90LV028AU	U	8-pin MSOP
PI90LV028AUE	U	Pb-free & Green, 8-pin MSOP
PI90LV018AW	W	8-pin SOIC
PI90LV018AWE	W	Pb-free & Green, 8-pin SOIC
PI90LV018AU	U	8-pin MSOP
PI90LV018AUE	U	Pb-free & Green, 8-pin MSOP

**Notes:**

1. Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)