Ordering number : ENA1708

SANYO Semiconductors
DATA SHEET

LV8130V — Bi-CMOS IC For Brushless Motor Drive Direct PWM Drive, Quiet Predriver IC

Overview

The LV8130V is a PWM drive pre-driver IC designed for three-phase brushless motors.
This IC reduces motor driving noise by imparting a slope to the phase switching current by quiet PWM drive, and realizes high efficiency through the use of synchronous rectification.
A motor drive circuit with the desired output capability (voltage, current) can be implemented by adding discrete transistors or other devices to the output. Furthermore, the LB8130V provides a full complement of protection circuits allowing it to easily implement high-reliability drive circuits. This IC is optimal for driving various large-scale motors such as those used in air conditioners and water heaters.

Features

- Three-phase bipolar drive
- Quiet PWM drive (150-degree current carrying + current feedback)
- Synchronous rectification (with enable/disable select pin)
- Speed control signal (supports either by analog voltage or PWM duty pulse input.)
- Built-in forward/reverse switching circuit
- Start/stop switching circuit (stop mode power save function)
- Built-in current limiter circuit (Supports 0.25V (typical) reference voltage sensing based high-precision detection)
- Built-in low-voltage protection circuit (The operating voltage can be set with a zener diode.)
- Built-in automatic recovery type constraint protection circuit (ON:OFF = 1:15), with motor constraint protection detection output (RD pin)
- Selectable Hall signal pulse outputs (1-Hall FG or 3-Hall FG)
- Supports thermistor based thermal protection of the output transistors.

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60910 SY PC 20100413-S00001 No.A1708-1/19

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max	V_{CC} pin	23	V
Output current	I_O max1	Pins UH, VH, WH	50	mA
	I_O max2	Pins UL, VL, WL	50	mA
LVS pin applied voltage	LVS max	LVS pin	23	V
Allowable power dissipation	Pd max1	Independent IC, Tj = 150°C	0.45	W
	Pd max2	Mounted on a circuit board.*	1.05	W
Operating temperature	Topr		-40 to +100	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified circuit board : 114.3mm × 76.1mm × 1.6mm, glass epoxy

Allowable Operating range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1-1	V_{CC}1-1	V_{CC} pin	9 to 21	V
Supply voltage range 1-2	V_{CC}1-2	V_{CC} pin, V_{CC}-VREG short time	4.5 to 5.5	V
Output current	I_O	Pins UL, VL, WL, UH, VH, WH	45	mA
5V constant voltage output current	I_{REG}		-30	mA
HP pin applied voltage	V_{HP}		0 to 5	V
HP pin output current	I_{HP}		0 to 15	mA
RD pin applied voltage	V_{RD}		0 to 5	V
RD pin output current	I_{RD}		0 to 15	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = 12V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current 1	I_{CC}1			4	6	mA
Supply current 2	I_{CC}2	At stop		1	2	mA
5V Constant-voltage Output (VREG pin)						
Output voltage	VREG		4.7	5.0	5.3	V
Line regulation	ΔVREG1	V_{CC} = 8 to 17V		40	100	mV
Load regulation	ΔVREG2	I_O = -5 to -20mA		5	35	mV
Temperature coefficient	ΔVREG3	Design target value*		0		mV/°C
Output block						
Output voltage 1-1	V_{OUT}1-1	Low level, I_O = 10mA		0.3	0.5	V
Output voltage 1-2	V_{OUT}1-2	Low level, I_O = 30mA		0.9	1.3	V
Output voltage 2-1	V_{OUT}2-1	High level, I_O = -10mA		V_{CC}-0.3	V_{CC}-0.5	V
Output voltage 2-2	V_{OUT}2-2	High level, I_O = -30mA		V_{CC}-0.9	V_{CC}-1.3	V
Output leakage current	$I_O$leak				10	μA
CTL Amplifier						
Input offset voltage	V_{IOF} (CTL)		-10		10	mV
Input bias current	IB (CTL)		-1		1	μA
Common-mode input voltage range	VICM		0		VREG-1.7	V
Input open voltage	V_{IO} (CTL)		VREG-0.5		VREG	V
Low level input current	I_{IL} (CTL)	VEI^+ = 0V	-100	-80		μA
High level output voltage	V_{OH} (CTL)	ITOC = -0.2mA	VREG-1.2	VREG-0.8		V
Low level output voltage	V_{OL} (CTL)	ITOC = 0.2mA		0.8	1.05	V
Open-loop gain	G (CTL)	f (CTL) = 1kHz	45	51		dB

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
PWM Oscillator (PWM pin)						
High level output voltage	V_{OH} (PWM)		2.8	3.0	3.2	V
Low level output voltage	V_{OL} (PWM)		1.3	1.5	1.7	V
External capacitor charge current	ICHG	VPWM = 2.1V	-50	-40	-30	μA
Oscillation frequency	f (PWM)	C = 1000pF		25		kHz
Amplitude	V (PWM)		1.3	1.5	1.7	Vp-p
Drive block (TOC pin)						
Input voltage 1	VTOC	Output duty 0%		1.28		V
Gain	GDF			0.14		
Limiter voltage	VL			3.0		V
Hall Amplifier						
Input bias current	IHB (HA)		-2	-0.5		μA
Common-mode input voltage range 1	VICM1	When using Hall elements	0.5		VREG-2.0	V
Common-mode input voltage range 2	VICM2	At one-side input bias (Hall IC application)	0		VREG	V
Hall input sensitivity			80			mVp-p
Hysteresis width	ΔV_{IN} (HA)		15	24	40	mV
Input voltage Low → High	VSLH (HA)		5	12	20	mV
Input voltage High → Low	VSHL (HA)		-20	-12	-5	mV
HP pin						
Output saturation voltage	VHPL	I_O = 10mA		0.2	0.5	V
Output leakage current	IHPleak	V_O = 5V			10	μA
CSD oscillator (CSD pin)						
High level output voltage	V_{OH} (CSD)		2.7	3.0	3.3	V
Low level output voltage	V_{OL} (CSD)		0.7	1.0	1.3	V
External capacitor charge current	ICHG1	VCSD = 2V	-3.0	-2.2	-1.7	μA
External capacitor discharge current	ICHG2	VCSD = 2V	0.11	0.15	0.19	μA
Charge/discharge current ratio	RCSD	Charge current/Discharge current	12	15	18	
RD pin						
Low level output voltage	VRDL	I_O = 10mA		0.2	0.5	V
Output leakage current	IL (RD)	V_O = 5V			10	μA
Current control circuit (RF pin)						
Limiter voltage	VRF	RF-RFGND	0.234	0.26	0.286	V
Low-voltage protection circuit (LVS pin)						
Operation voltage	VSDL		3.5	3.7	3.9	V
Release voltage	VSDH		4.0	4.2	4.4	V
Hysteresis width	ΔVSD		0.35	0.5	0.65	V
PWMIN pin						
Input frequency	f (PI)				50	kHz
High level input voltage range	V_{IH} (PI)		2.0		VREG	V
Low level input voltage range	V_{IL} (PI)		0		1.0	V
Input open voltage	V_{IO} (PI)		VREG-0.5		VREG	V
Hysteresis width	V_{IS} (PI)		0.2	0.3	0.4	V
High level input current	I_{IH} (PI)	VPWMIN = VREG	-10	0	10	μA
Low level input current	I_{IL} (PI)	VPWMIN = 0V	-120	-90		μA
S/S pin						
High level input voltage	V_{IH} (SS)		2.0		VREG	V
Low level input voltage range	V_{IL} (SS)		0		1.0	V
Hysteresis width	V_{IS} (SS)			0.28		V
High level input current	I_{IH} (SS)	VS/S = VREG	-10	0	10	μA
Low level input current	I_{IL} (SS)	VS/S = 0V	-10	-1		μA

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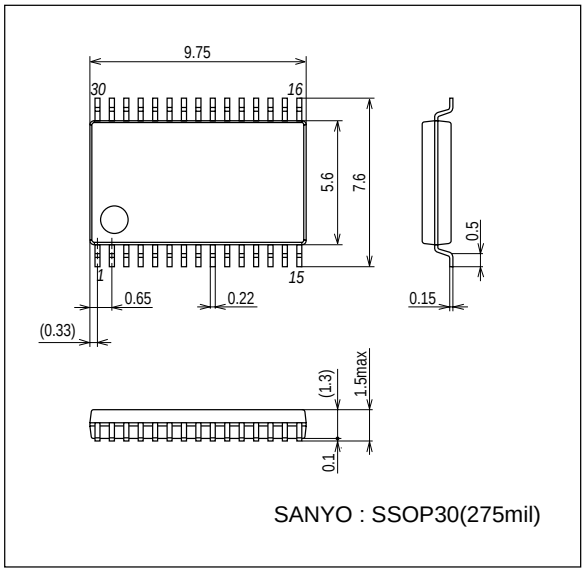
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
F/R pin						
High level input voltage	V_{IH} (FR)		2.0		VREG	V
Low level input voltage	V_{IL} (FR)		0		1.0	V
Input open voltage	V_{IO} (FR)		VREG-0.5		VREG	V
Hysteresis width	V_{IS} (FR)		0.2	0.3	0.4	V
High level input current	I_{IH} (FR)	VF/R = VREG	-10	0	10	μA
Low level input current	I_{IL} (FR)	VF/R = 0V	-120	-90		μA
N1 pin						
High level input voltage	V_{IH} (N1)		3.5		VREG	V
Low level input voltage	V_{IL} (N1)		0		2.0	V
Input open voltage	V_{IO} (N1)		VREG-0.5		VREG	V
High level input current	I_{IH} (N1)	VN1 = VREG		0		μA
Low level input current	I_{IL} (N1)	VN1 = 0V	-120	-50		μA
SR pin						
High level input voltage	V_{IH} (SR)		3.5		VREG	V
Low level input voltage	V_{IL} (SR)		0		2.0	V
Input open voltage	V_{IO} (SR)		VREG-0.5		VREG	V
High level input current	I_{IH} (SR)	VSR = VREG		0		μA
Low level input current	I_{IL} (SR)	VSR = 0V	-120	-50		μA

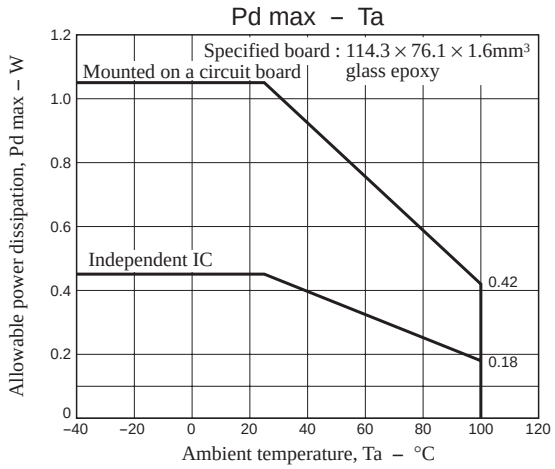
Package Dimensions

unit : mm (typ)

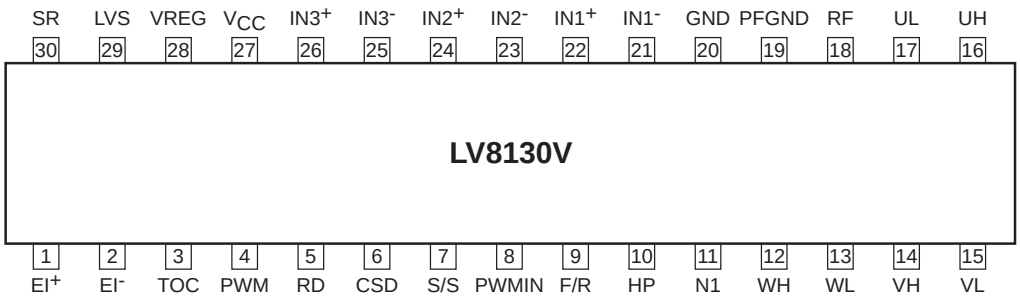
3191B



SANYO : SSOP30(275mil)



Pin Assignment



Three-phase logic truth table (IN = "High" indicates the state where $IN^+ > IN^-$.)

	F/R = ⌈L⌋			F/R = ⌈H⌋			Drive output	
	IN1	IN2	IN3	IN1	IN2	IN3	Upper	Lower
1	H	L	H	L	H	L	VH	UL
2	H	L	L	L	H	H	WH	UL
3	H	H	L	L	L	H	WH	VL
4	L	H	L	H	L	H	UH	VL
5	L	H	H	H	L	L	UH	WL
6	L	L	H	H	H	L	VH	WL

S/S pin

Input state	Mode
High	Stop
Low	Start

PWMIN pin

Input state	Mode
High or Open	Output OFF
Low	Output ON

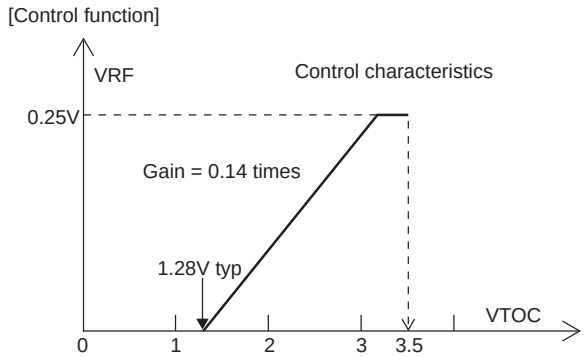
N1 pin

Input state	HP output
High or Open	Synthesis of three Halls
Low	1-Hall

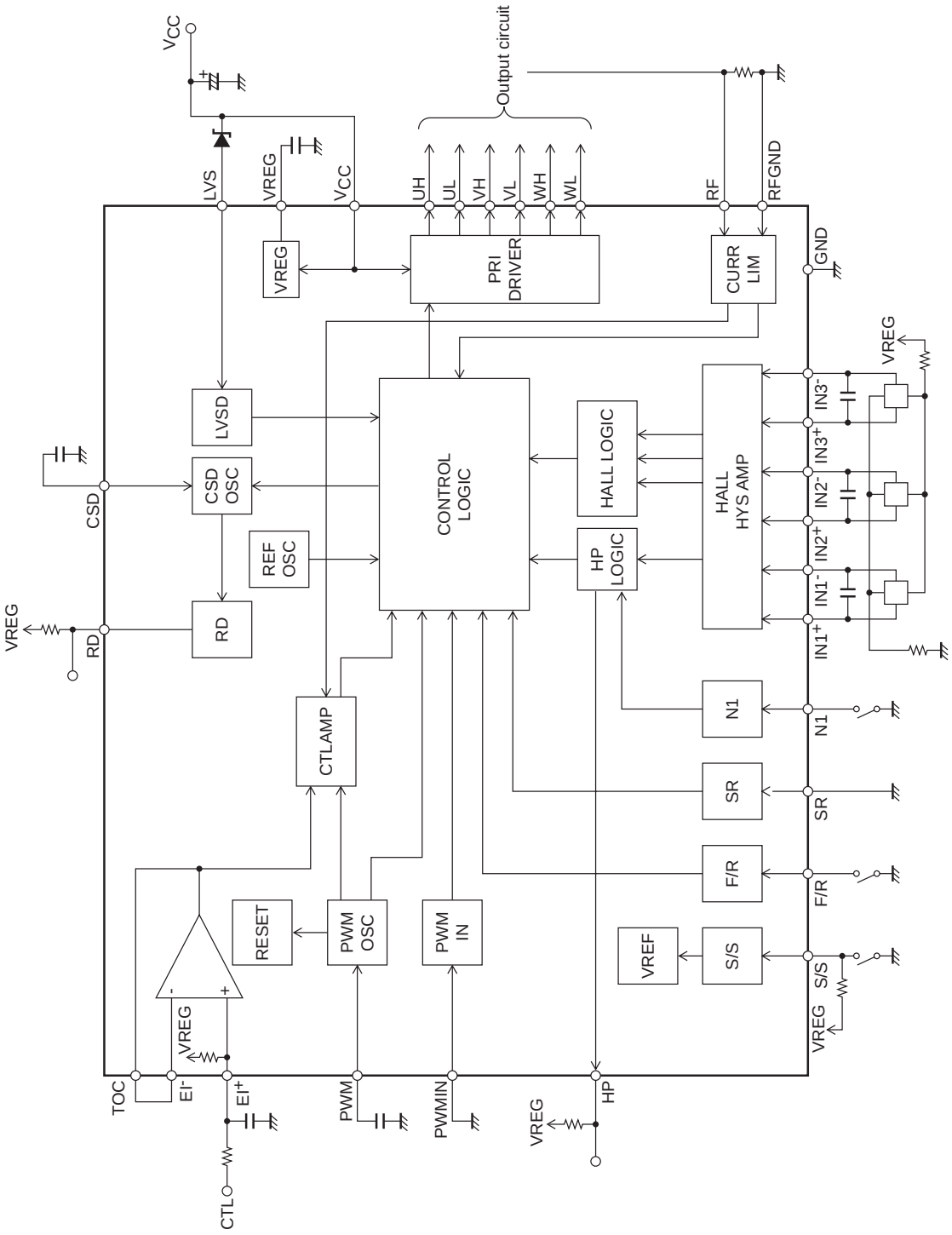
SR pin

Input state	Synchronous rectification
High or Open	ON
Low	OFF

The S/S pin does not have a built-in pull-up resistor, so an external pull-up resistor or equivalent is required to set the IC to the stop state. If the S/S and PWMIN pins are not used, the unused pin input must be set to low-level voltage.
When the PWMIN pin is used for control, apply voltage between 4V and VREG to the EI^+ pin.
The HP output can be selected by the N1 pin setting from the N1 Hall input converted to a pulse output (one-Hall output) or the three-phase output synthesized from the Hall inputs (three-Hall synthesized output).
With or without synchronous rectification when PWM is off can be specified by the SR pin.

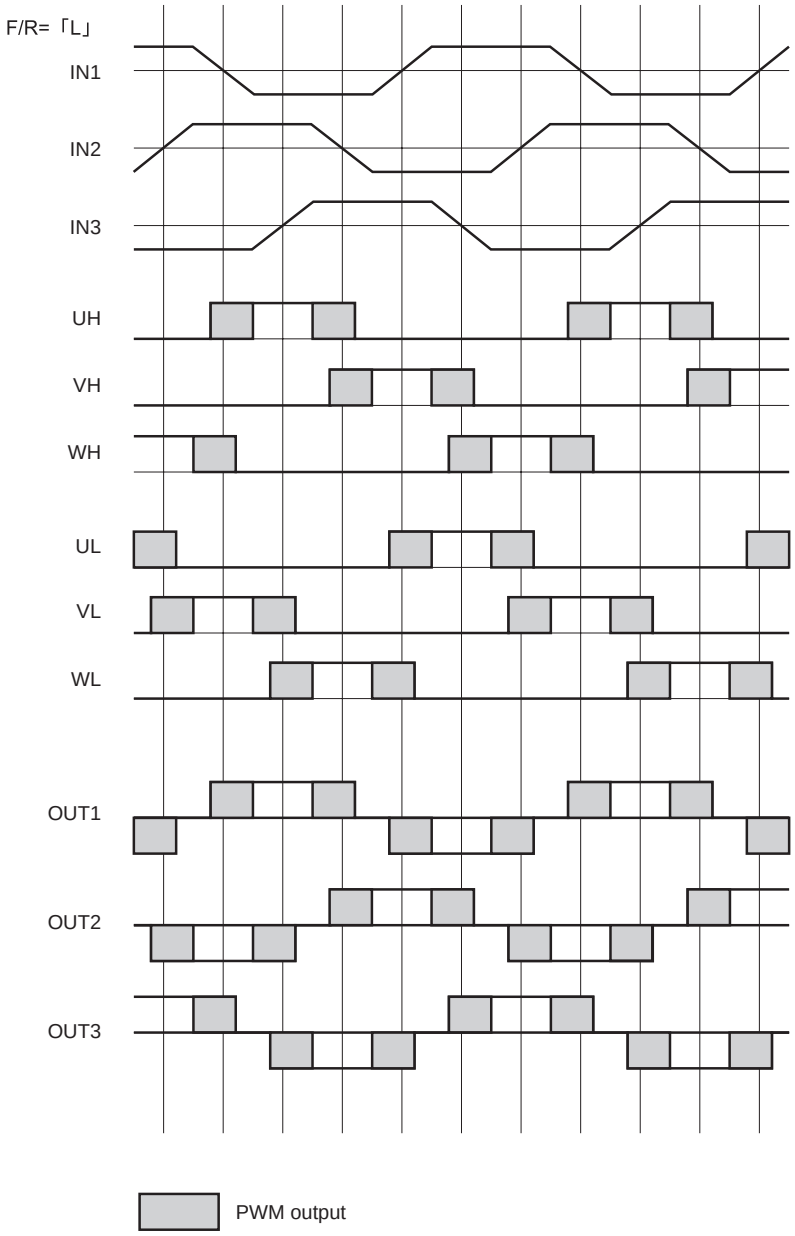


Block Diagram

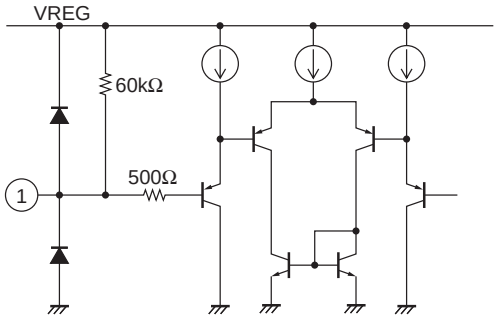
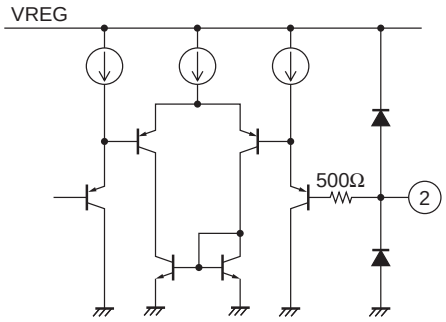
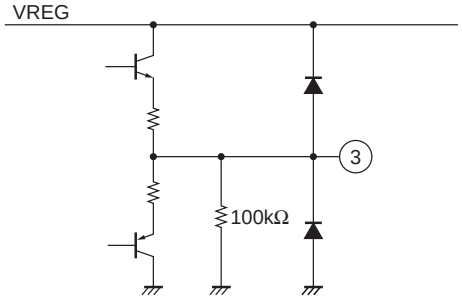
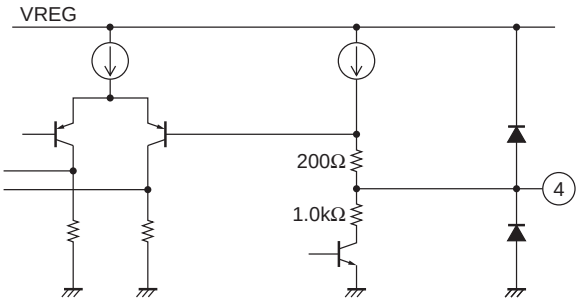
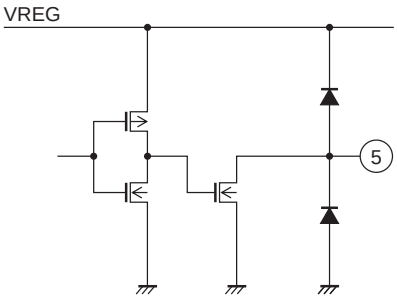


Hall Input/Output Timing Chart

The Hall input order must be set up as follows.
If the F/R pin and the Hall input order differ from the timing chart, the motor is driven by the 120 degrees current-carrying.
The Hall input is performed by the reverse order when the F/R pin is low or high.



Pin Functions

Pin No.	Pin Name	Pin function	Equivalent Circuit
1	EI^+	CTL amplifier input + pin. For control with this pin, the input voltage must be 3.5V or less.	
2	EI^-	CTL amplifier input - pin. Normally connect with the TOC pin.	
3	TOC	CTL amplifier output pin. When the TOC pin voltage rises, the IC changes the output signal PWM duty to increase the torque output.	
4	PWM	Multiplexed function pin: PWM oscillation frequency setting and initial reset pulse generation. Insert a capacitor between this pin and ground.	
5	RD	Motor constraint protection detection output pin. This pin output is on when the motor is turning, and off when the constraint protection circuit operates. This is an open-collector output.	

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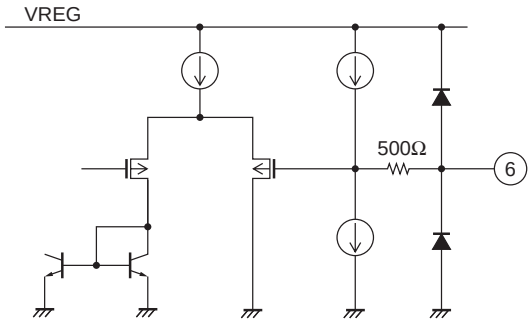
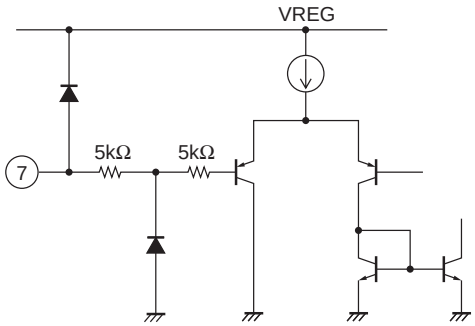
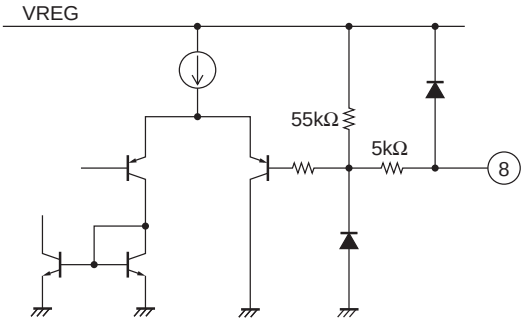
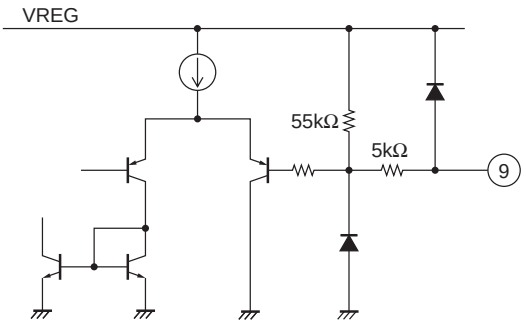
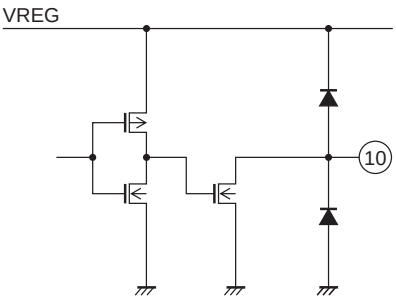
Pin No.	Pin Name	Pin function	Equivalent Circuit
6	CSD	Pin to set the operating time of the motor constraint protection circuit. Insert a capacitor between this pin and ground. This pin must be connected to ground if the constraint protection circuit is not used.	
7	S/S	Start/stop input pin. A low-level input sets the IC to start mode, and a high-level input set it to stop mode.	
8	PWMIN	PWM pulse input pin. A low-level input specifies the output drive state, and a high-level or open input specifies the output off state. When this pin is used for control, the EI^+ pin voltage must be set to between 4V and VREG.	
9	F/R	Forward/reverse input pin.	
10	HP	Hall signal output pin (This is an open-collector output). The IN1 Hall input converted to a pulse output by the N1 pin setting. The HP output can be selected by the N1 pin setting from the IN1 Hall input converted to a pulse output (one-Hall output) or the three-phase output synthesized from the Hall inputs (three-Hall synthesized output).	

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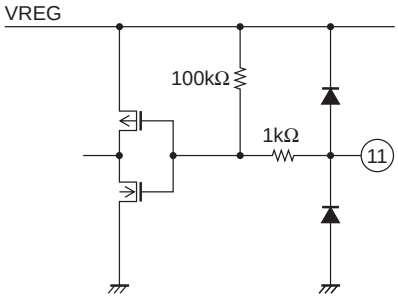
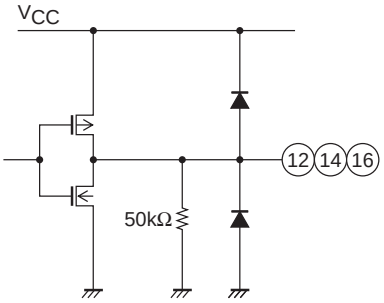
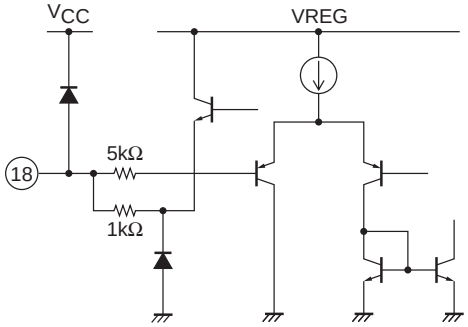
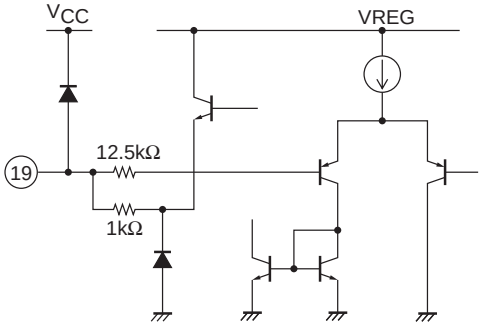
Pin No.	Pin Name	Pin function	Equivalent Circuit
11	N1	Pin to select the Hall signal output type (HP output).	
12 13 14 15 16 17	WH WL VH VL UH UL	Output pins. These are push-pull outputs.	
18	RF	Output current detection pin. Detection is performed by sensing the voltages on both ends of the current detection resistor (Rf) with the RF and RFGND pins. This sets the maximum output current I_{OUT} to be 0.25/Rf.	
19	RF GND	Output current detection reference pin.	
20	GND	Ground.	

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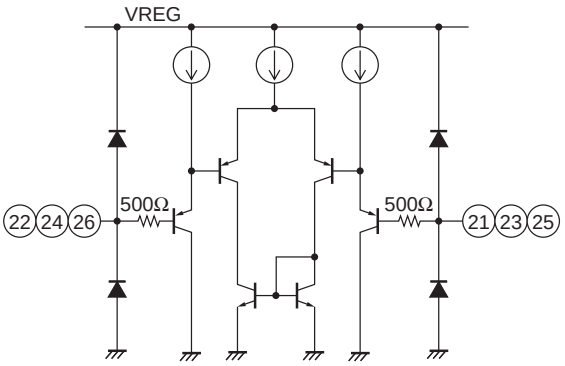
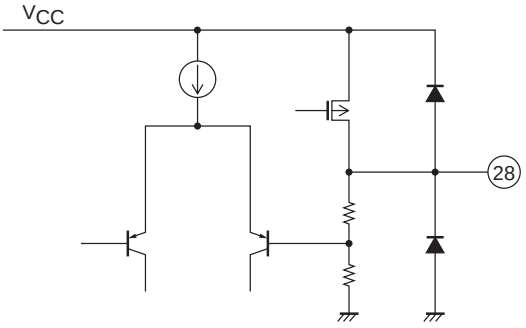
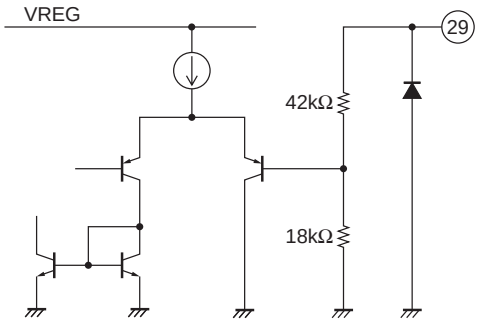
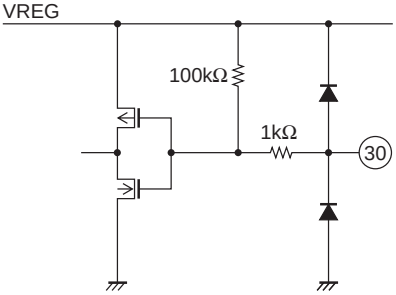
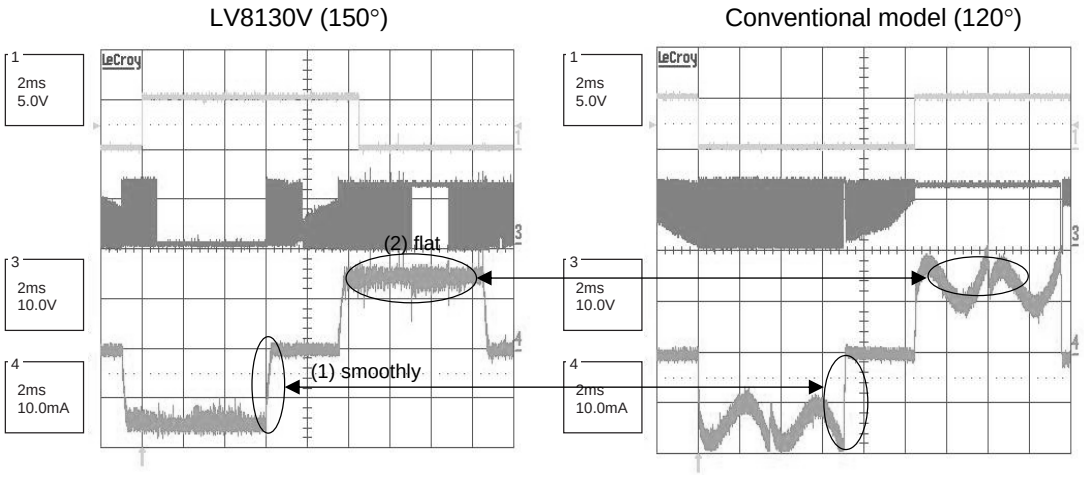
Pin No.	Pin Name	Pin function	Equivalent Circuit
22 21 24 23 26 25	IN^+ IN^- $IN2^+$ $IN2^-$ $IN3^+$ $IN3^-$	Hall signal input pins from each motor phase. The logic high state is the state where $IN^+ > IN^-$. If input is provided from a Hall IC, the common-mode input range can be expanded by biasing either + or -.	
27	V_{CC}	Power supply pin. Insert a capacitor between this pin and ground to prevent the influence of noise, etc.	
28	VREG	5V regulator output pin (control circuit power supply). Insert a capacitor between this pin and ground for stabilization.	
29	LVS	Undervoltage protection voltage detection pin. If a 5V or higher supply voltage is to be detected, set the detection voltage by insetting an appropriate zener diode in series.	
30	SR	Synchronous rectification select pin. A low-level input set up the IC with synchronous rectification disabled, and a high-level input synchronous rectification enabled.	

Description of LV8130V

1. Output Drive Circuit

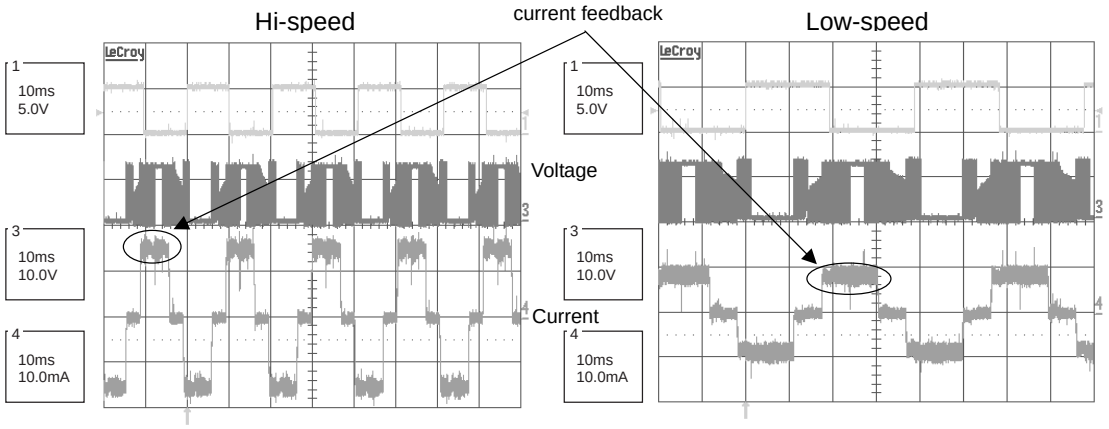
The LV8130V adopts quiet PWM drive to realize low power consumption and low noise.
This drive method is a direct PWM drive to reduce power loss in the output. In addition, the current-carrying angle is 150 degrees to reduce noise, and soft-switching is performed by changing the duty and imparting a slope to the current when switching the phases. Furthermore, when the IC is controlled with the EI^+ pin voltage, current feedback is performed to keep the coil current constant, allowing it to implement a system with reduced noise and vibration.

Waveform Example (1)



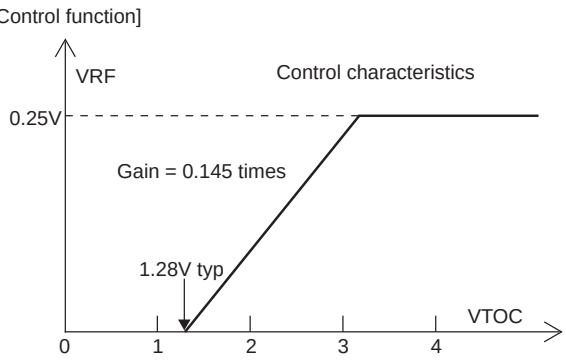
(1) Current slope when switching the phases by quiet PWM drive
(2) Reduction of current fluctuation by current feedback

Waveform Example (2)



The right figure shows the relationship between the control voltage and the RF voltage for current feedback. Current is flowed to the coil until the RF voltage determined by the control voltage is reached, and when the RF voltage reaches the target voltage, the PWM is turned off to maintain a constant current. This relationship shown in the right figure enables adjustment of the coil current by the RF resistor. Labeling the RF resistor as R0 (Ω), the coil current relative to the control voltage is as follows.

$$I_O = (\Delta V_{IN} \times 0.145) / R0$$



2. Control Methods

- Control using the EI^+ pin (TOC pin) ⇒ Current feedback

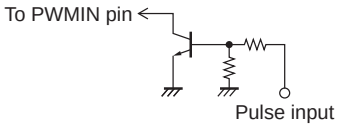
  The output transistor duty is determined according to the result of comparing the TOC pin voltage with the RF voltage. When the RF voltage reaches the target voltage set by the control voltage, the PWM is turned off to maintain a constant current.

  The TOC pin is the CTL amplifier output pin, so the control voltage cannot be input directly to the TOC pin. Normally, the CTL amplifier is used as a full-feedback amplifier (with the EI^- pin connected to the TOC pin), and DC voltage is input to the EI^+ pin (EI^+ pin voltage will become equal to the TOC pin voltage).

  When the EI^+ pin is in open state, the motor will be driven. So connect a pull-down resistor to the EI^+ pin if the motor should not operate when the EI^+ pin is open. When performing control using the TOC pin voltage, leave the PWMIN pin voltage open or connect the pin to ground.

- Pulse control using the PWMIN pin

  The output can be controlled based on the duty of the pulse signal input to the PWMIN pin. However, as there is a delay time as shown in the figure below, the input duty and the output duty do not match.

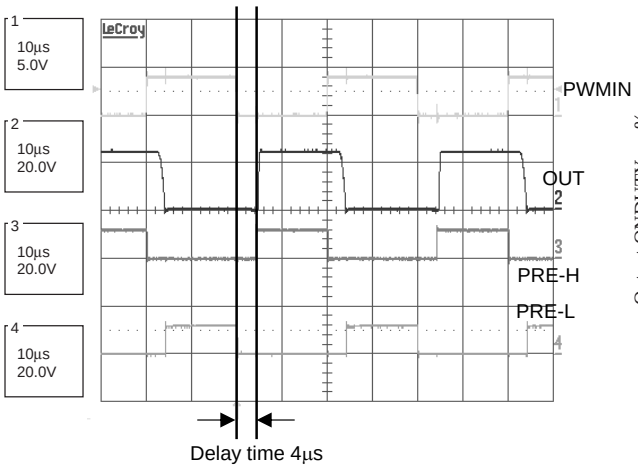
  

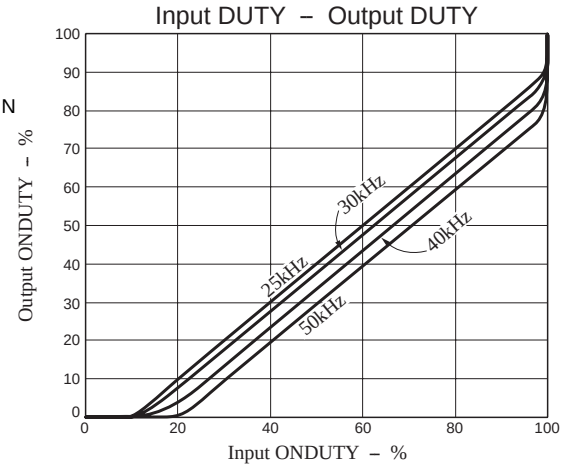
  The output is on when a low-level voltage is input to the PWM pin, and off when a high-level voltage is input to the PWM pin. When the PWMIN pin is open, it goes to high level and the output is off. When inverted logic input is required, this can be supported by adding an external transistor (NPN).

  When controlling motor operation from the PWMIN pin, connect the EI^- pin to ground and the EI^+ pin to the TOC pin.

  Note that the PWM oscillation is also used as the internal circuit clock, connect a capacitor (approx. 1000pF) to the PWM pin, even if the PWMIN pin is used to control the motor.

Waveform Example (3)





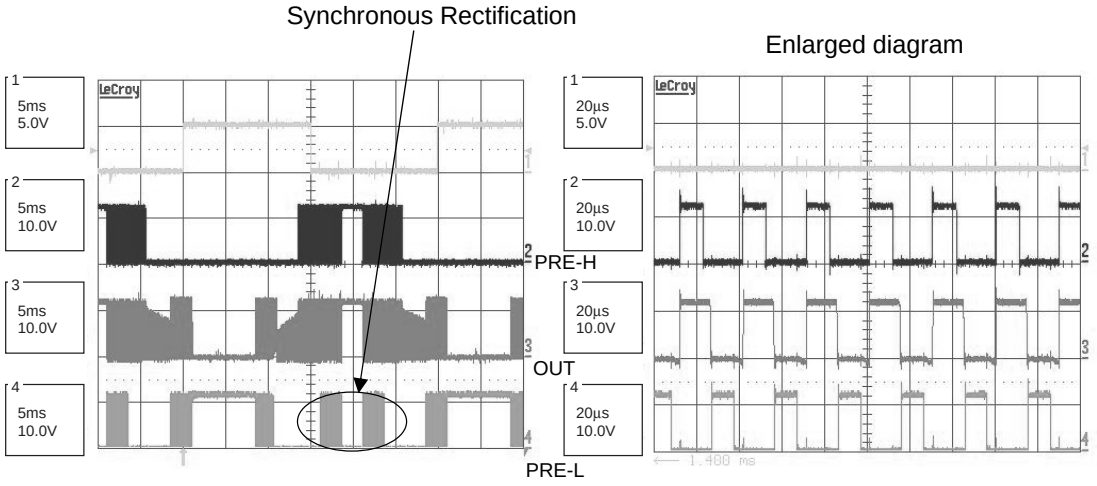
The LV8130 has a delay time of 4µs (between when the PWMIN pin input changes from high (OFF) to low (ON) and when the PRE-H output changes from low (OFF) to high (ON)) in order to realize synchronous rectification.
Therefore, the relationship between the input duty and the output duty is as shown in the right figure.
This input duty - output duty relationship changes according to the input frequency to maintain a constant delay time.

3. Synchronous Rectification

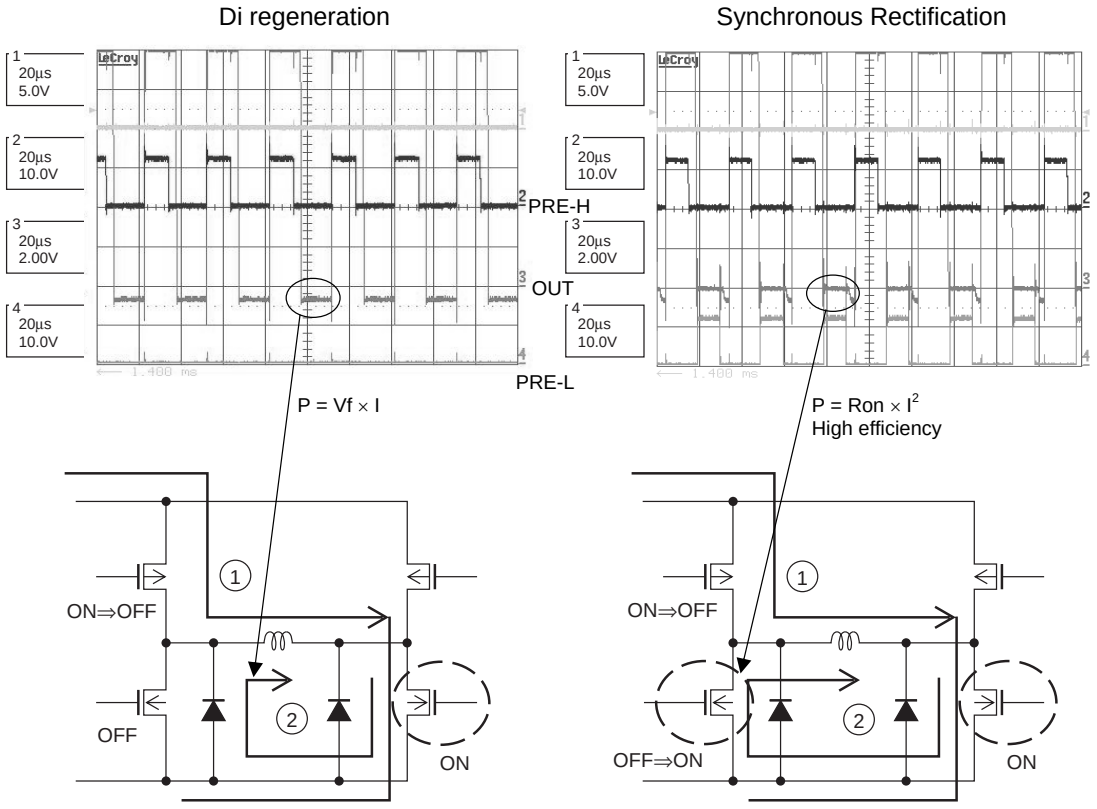
This IC performs synchronous rectification by setting the SR pin to high or open. Synchronous rectification sets the lower output FET to on when PWM is off (high side = OFF). This causes regenerative current to flow to the FET instead of the diode, so the loss during regeneration can be reduced by establishing the relationship Vf > ON resistor × Regenerative current.

The IC pre-output has an output delay time of approx. 4μs between the high side off and the low side on, but a through current flows according to the output stage delay time, so this must be investigated.

Waveform Example (4)



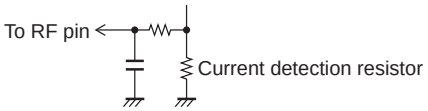
Waveform Example (5)



4. Current Limiter Circuit

The current limiter circuit limits the output current peak value to a level determined by the equation I = V_{RF}/Rf (V_{RF} = 0.26V (typical), Rf: current detection resistor). This circuit suppresses the output current by reducing the output on duty.

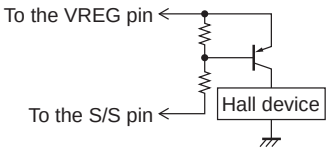
High-precision detection can be implemented by connecting lines from the RF and RFGND pin close to the both ends of the current detection resistor (Rf).



The current limiter circuit has an internal filter circuit that works to prevent incorrect current limiting operation by detecting the reverse recovery current of the output diode due to PWM operation. In normal applications there should be no problems with the internal filter circuit, but if incorrect operation occurs (when the diode reverse recovery current flows for 1μs or more), add an external filter circuit (R, C low-pass filter, etc.).

5. Power Saving Circuit

This IC goes to a low-power mode (power saving state) when set to the stop state. In the power save state, the bias current in most of the circuits is cut. However, the 5V regulator output (VREG) is still provided in the power saving state. If it is also necessary to cut the Hall device bias current, this function can be provided by an application that, for example, connects the Hall devices to 5V through PNP transistors.



6. Notes on the PWM Frequency

The PWM frequency is determined by the capacitor C (F) connected to the PWM pin.

$$fPWM \approx 1/(41000 \times C)$$

If a 1000pF capacitor is used, the circuit will oscillate at approx. 25kHz. If the PWM frequency is too low, switching noise will be audible from the motor, and if it too high, the output power loss will increase. Thus a frequency in the range of 15kHz and 50kHz must be used. The capacitor's ground terminal must be placed as close as possible to the IC's ground pin to minimize the influence of output noise and other noise sources.

7. Hall Input Signal

A pulse input with the amplitude in excess of the hysteresis (80mV maximum) is required for the Hall inputs. Considering the possibility of noise and phase displacement, an even larger amplitude is desirable.

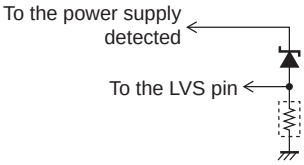
If noise disrupts the output waveform (during phase switching) or the HP output (Hall signal output), this must be prevented by inserting capacitors or other devices across these inputs. The constraint protection circuit uses the Hall inputs to discriminate the motor constraint state. Although the circuit is designed to tolerate a certain amount of noise, care is required when using the constraint protection circuit.

If all three phases of the Hall input signal go to the same input state, the outputs are all set to the off state (the UL, VL, WL, UH, VH and WH outputs all go to the low level).

If the outputs from a Hall IC are used, fixing one side of the inputs (either the + or – side) at a voltage within the common-mode input voltage range allows the other input side to be used as an input over the 0V to V_{CC} range.

8. Undervoltage Protection Circuit

The undervoltage protection circuit turns one side of the outputs (UH, VH, WH) off when the LVS pin voltage falls below the minimum operating voltage. (see the Electrical Characteristics.) To prevent this circuit from repeatedly turning the outputs on and off in the vicinity of the protection operating voltage, this circuit is designed with hysteresis. Thus the output will not recover until the operating voltage rises 0.5V (typical) higher than the operating voltage.



The protection operation voltage detection level is set up for 5V systems. The detected voltage level can be increased by shifting the voltage by inserting a zener diode in series with the LVS pin to shift the detection level.

- Operation voltage ≈ 3.7 + ZD voltage
- Reset voltage ≈ 4.2 + ZD voltage

The LVS pin influx current during detection is approx. 80μA. To increase the diode current to stabilize the zener diode voltage rise, insert a resistor between the LVS pin and ground.

If the LVS pin is left open, it is set to ground level input by the internal pull-down resistor, and the output will be turned off. Therefore, when not using the undervoltage protection circuit, a voltage in excess of the LVS circuit reset voltage (4.4V) or more must be applied to the LVS pin. (The LVS pin can also be shorted with 5VREG pin.) The maximum rating for the voltage applied to the LVS pin is 18V.

9. Constraint Protection Circuit

When the motor is physically constrained (held stopped), the CSD pin external capacitor is charged (to approx. 3.0V) by a constant current of approx. 2.25μA and is then discharged (to approx. 1.0V) by a constant current of approx. 0.15μA. This process is repeated, generating a sawtooth wave. The constraint protection circuit turns motor drive on and off repeatedly based on this sawtooth waveform. (The UH, VH and WH side outputs are turned on and off.) Motor drive is on during the period the CSD pin external capacitor is being charged from approx. 1.0V to approx. 3.0V, and motor drive is off during the period the CSD pin external capacitor is being discharged from approx. 3.0V to approx. 1.0V. The IC and the motor are protected by this repeated drive on/off operation when the motor is physically constrained.

The motor drive on and off times are determined by the value of the connected capacitor C (μF).

TCSD1 (drive on period) ≈ 0.9 × C (seconds)
TCSD2 (drive off period) ≈ 13.7 × C (seconds)

When a 0.47μF capacitor is connected externally to the CSD pin, this iterated operation will have a drive on period of approx. 0.4 seconds and drive off period of approx. 6.4 seconds.

While the motor is turning, the discharge pulse signal (generated once for each Hall input period) that is created by combining the Hall inputs internally in the IC discharges the CSD pin external capacitor. Since the CSD pin voltage does not rise, the constraint protection circuit does not operate.

When the motor is physically constrained, the Hall inputs do not change and the discharge pulses are not generated. As a result, the CSD pin external capacitor is charged by a constraint current of approx. 2.25μA to approx. 3.0V, at which point the constraint protection circuit operates. When the constraint on motor is released, the constraint protection is released.
Connect the CSD pin to ground if the constraint protection function is not used.

10. Forward/Reverse Direction Operation

This IC is designed so that through currents (due to the output transistor off delay time when switching) do not flow in the output when switching directions when the motor is running. However, if the direction is switched when the motor is running, current levels in excess of the current limiter value may flow in the output transistors due to the motor coil resistance and the motor back EMF state when switching. Therefore, designers must consider selecting external transistors that are not destroyed by those current levels or switching directions only after the speed has fallen below a certain speed.

11. Handling Different Power Supply Types

When this IC is operated from an externally supplied 5V power supply (4.5V to 5.5V), short the V_{CC} pin to the VREG pin and connect them to the external power supply.
When this IC is operated from an externally supplied 12V power supply (8V to 17V), connect the V_{CC} pin to the power supply. (The VREG pin will generate a 5V level to function as the control circuit power supply.)

12. Power Supply Stabilization

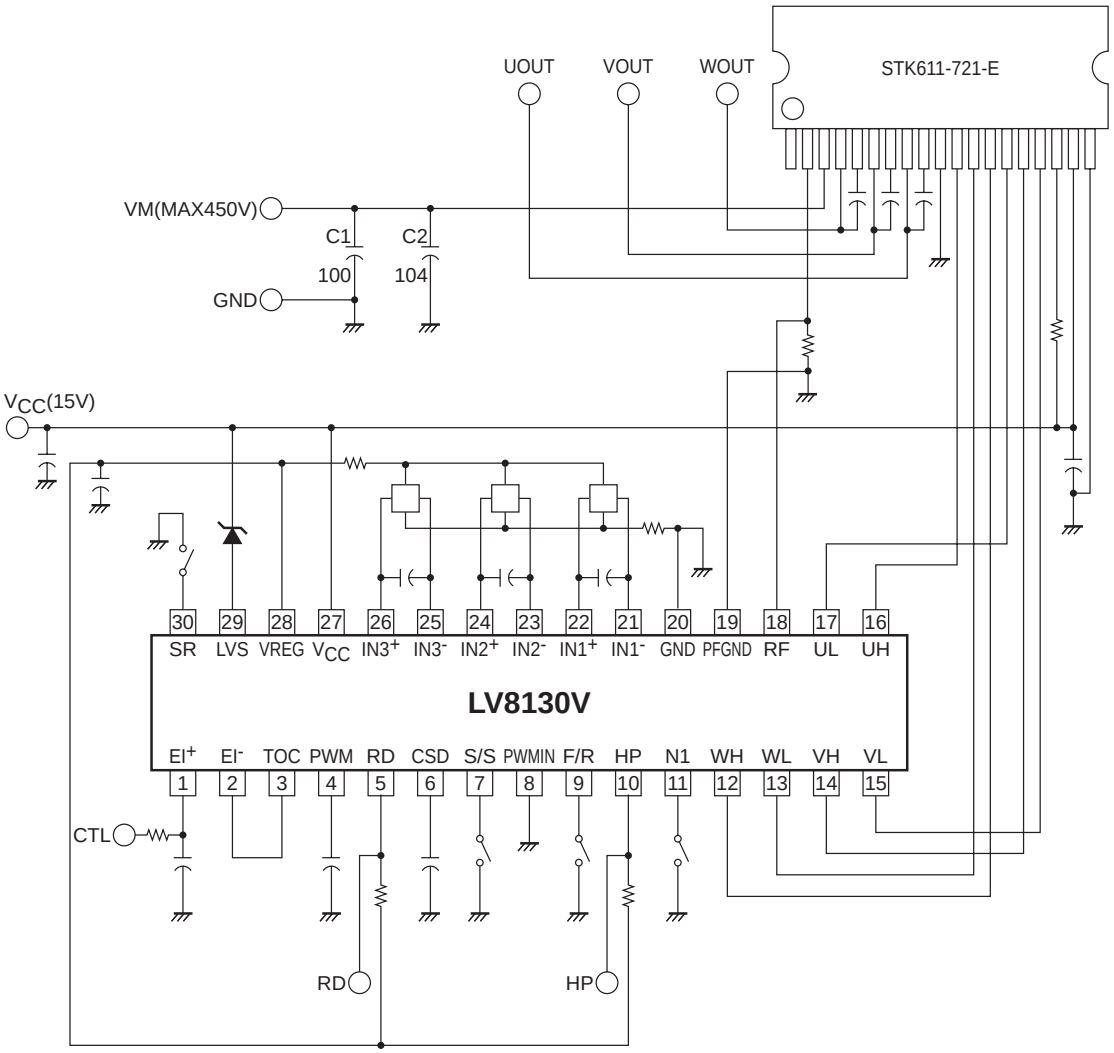
Since this IC uses a switching drive technique, the power supply line level can be disturbed easily. Therefore, capacitors with adequate capacitance to stabilize the power supply line must be inserted between V_{CC} pin and ground. If diodes are inserted in the power supply line to prevent IC destruction if the power supply is connected with reverse polarity, the power supply lines are even more easily disrupted. And even larger capacitor are required.
If the power supply is turned on and off by a switch, and if there is a significant distance between the switch and the stabilization capacitor, the supply voltage can be disrupted significantly by the line inductance and surge current into the capacitor. As a result, the withstand voltage of the device may be exceeded. In application such as this, the surge current must be suppressed and the voltage rise prevented by not using ceramic capacitors with a low series impedance, and by using electrolytic capacitors instead.

13. VREG Stabilization

To stabilize the VREG voltage, which is the control circuit power supply, a 0.1μF or larger capacitor must be inserted between the VREG pin and ground. The ground side of this capacitor must be connected to the IC ground pin with a line that is as short as possible.

Application Circuits Example

Example 1
High voltage application
Using a fan motor HIC (STK611 series)
CTL voltage control



Example 2
MOSFET drive (Pch + Nch)
PWM duty control