



# CY7B131 CY7B141

## 1Kx8 Dual-Port Static RAM

### Features

- 0.8-micron BiCMOS for high performance
- Automatic power-down
- TTL compatible
- Capable of withstanding greater than 2001V electrostatic discharge
- Fully asynchronous operation
- Master CY7B131 easily expands data bus width to 16 or more bits using slave CY7B141
- BUSY output flag on CY7B131; BUSY input on CY7B141
- INT flag for port-to-port communication

### Functional Description

The CY7B131 and CY7B141 are high-speed BiCMOS 1K by 8 dual-port static RAMs. Two ports are provided to permit independent access to any location in memory. The CY7B131

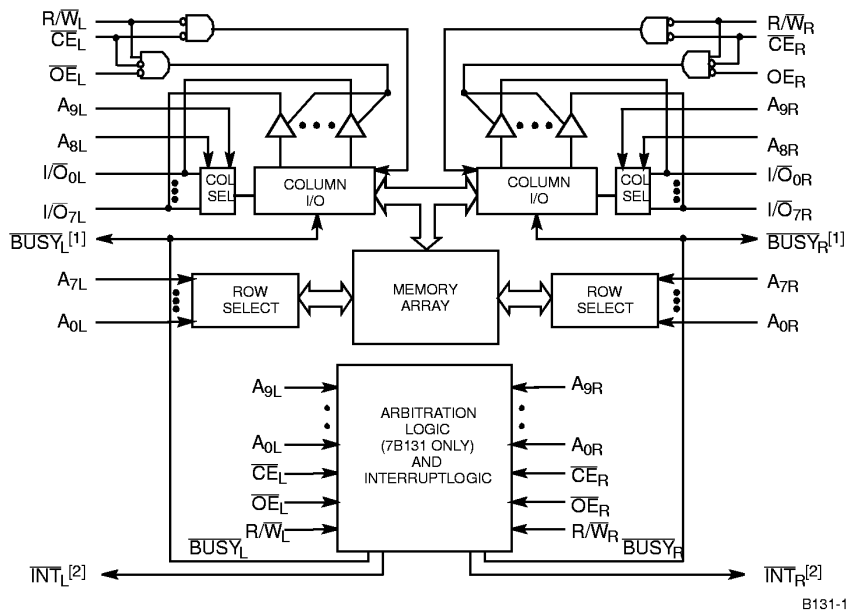
can be utilized as either a standalone 8-bit dual-port static RAM or as a MASTER dual-port RAM in conjunction with the CY7B141 SLAVE dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ( $\overline{CE}$ ), write enable (R/W), and output enable ( $\overline{OE}$ ). BUSY flags are provided on each port. In addition, an interrupt flag ( $\overline{INT}$ ) is provided on each port. BUSY signals that the port is trying to access the same location currently being accessed by the other port. The INT is an interrupt flag indicating that data has been placed in a unique location (3FF for the right port and 3FE for the left port).

An automatic power-down feature is controlled independently on each port by the chip enable ( $\overline{CE}$ ) pins.

The CY7B131/CY7B141 are available in 52-lead PLCC.

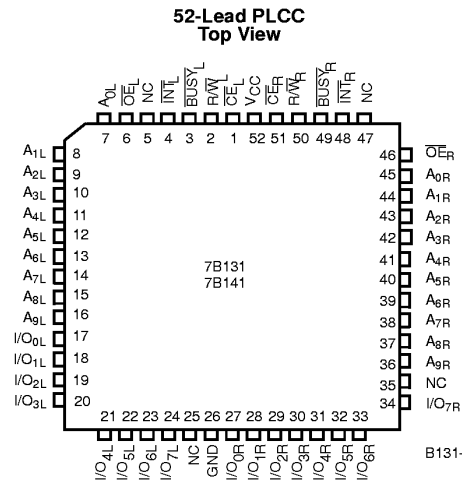
### Logic Block Diagram



#### Notes:

1. CY7B131 (Master): BUSY is an open drain output and requires a pull-up resistor. CY7B141 (Slave): BUSY is an input.
2. Open drain outputs; pull-up resistor required.

## Pin Configuration



## Selection Guide

		<b>7B131-15</b> <b>7B141-15</b>	<b>7B131-20</b> <b>7B141-20</b>
Maximum Access Time (ns)		15	20
Maximum Operating Current (mA)	Com'I/Ind	260	240/300
Maximum Standby Current (mA)	Com'I/Ind	110	100/105

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to ±150°C

Ambient Temperature with Power Applied ..... -55°C to ±125°C

Supply Voltage to Ground Potential (Pin 52 to Pin 26) ..... -0.5V to ±7.0V

DC Voltage Applied to Outputs in High Z State ..... -0.5V to ±7.0V

DC Input Voltage ..... -3.5V to ±7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001 V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

**Electrical Characteristics** Over the Operating Range<sup>[3]</sup>

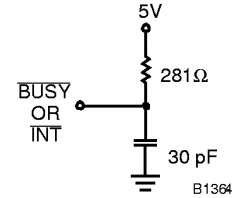
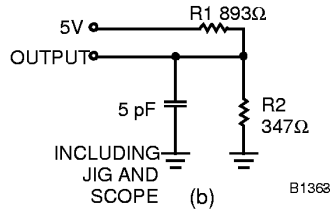
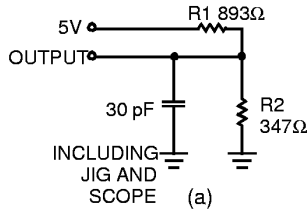
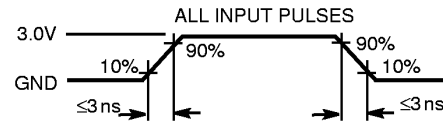
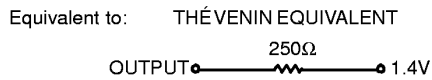
Parameter	Description	Test Conditions	7B131-15 7B141-15		7B131-20 7B141-20		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 4.0 mA		0.4		0.4	V
		I <sub>OL</sub> = 16.0 mA <sup>[4]</sup>		0.5		0.5	
V <sub>IH</sub>	Input HIGH Voltage		2.2		2.2		V
V <sub>IL</sub>	Input LOW Voltage			0.8		0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10	+10	-10	+10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-10	+10	-10	+10	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	CE = V <sub>IL</sub> , Outputs Open, f = f <sub>MAX</sub> <sup>[5]</sup>	Com'l	260	240		mA
			Ind		300		
I <sub>SB1</sub>	Standby Current Both Ports, TTL Inputs	CE <sub>L</sub> and CE <sub>R</sub> ≥ V <sub>IH</sub> , f = f <sub>MAX</sub> <sup>[5]</sup>	Com'l	110	100		mA
			Ind		105		
I <sub>SB2</sub>	Standby Current One Port, TTL Inputs	CE <sub>L</sub> or CE <sub>R</sub> ≥ V <sub>IH</sub> , Active Port Outputs Open, f = f <sub>MAX</sub> <sup>[5]</sup>	Com'l	165	155		mA
			Ind		180		
I <sub>SB3</sub>	Standby Current Both Ports, CMOS Inputs	Both Ports CE <sub>L</sub> and CE <sub>R</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0	Com'l	15	15		mA
			Ind		30		
I <sub>SB4</sub>	Standby Current One Port, CMOS Inputs	One Port CE <sub>L</sub> or CE <sub>R</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, Active Port Outputs Open, f = f <sub>MAX</sub> <sup>[5]</sup>	Com'l	160	150		mA
			Ind		170		

**Capacitance**<sup>[6]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

**Notes:**

- See the last page of this specification for Group A subgroup testing information.
- BUSY and INT pins only.
- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency of read cycle of 1/t<sub>rc</sub> and using AC Test Waveforms input levels of GND to 3V.
- Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms]**

**BUSY Output Load  
(CY7B136 ONLY)**

**Switching Characteristics Over the Operating Range<sup>[3, 7]</sup>**

Parameter	Description	7B131-15 7B141-15		7B131-20 7B141-20		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
$t_{RC}$	Read Cycle Time	15		20		ns
$t_{AA}$	Address to Data Valid <sup>[8]</sup>		15		20	ns
$t_{OHA}$	Data Hold from Address Change	3		3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid <sup>[8]</sup>		15		20	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid <sup>[8]</sup>		10		13	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[9]</sup>	3		3		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[9, 10]</sup>		10		13	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[9]</sup>	3		3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[9, 10]</sup>		10		13	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		15		20	ns

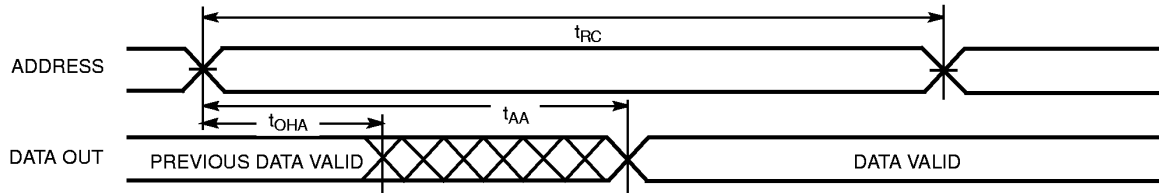
**Notes:**

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- AC test conditions use  $V_{OH} = 1.6V$  and  $V_{OL} = 1.4V$ .
- At any given temperature and voltage condition for any given device,  $t_{HZCE}$  is less than  $t_{LZCE}$  and  $t_{HZOE}$  is less than  $t_{LZOE}$ .
- $t_{LZCE}$ ,  $t_{LZWE}$ ,  $t_{HZOE}$ ,  $t_{LZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are tested with  $C_L = 5pF$  as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.

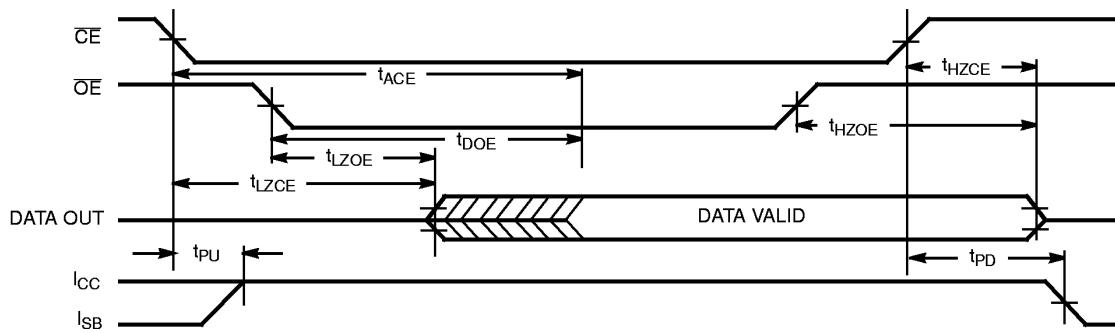


**Switching Characteristics** Over the Operating Range<sup>3, 7</sup> (Continued)

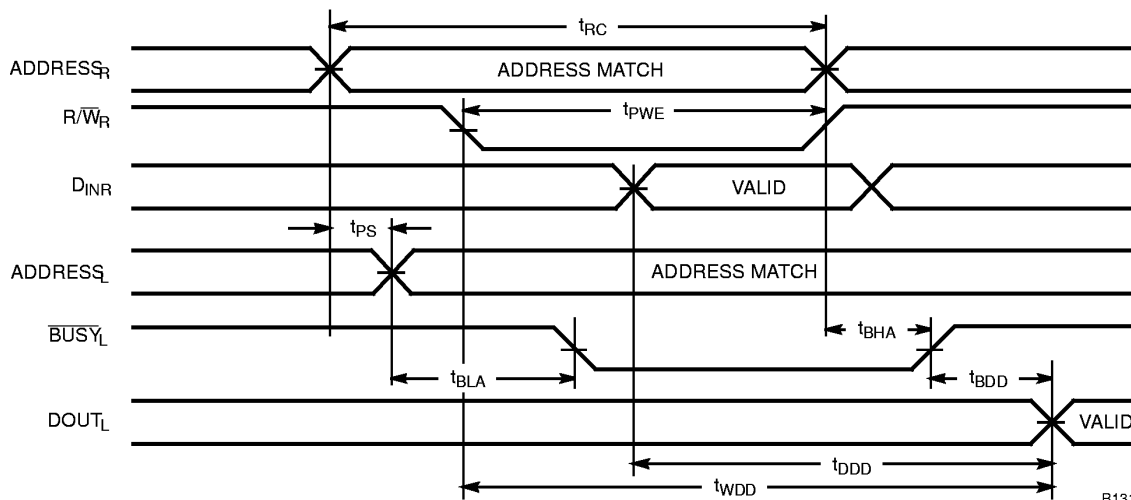
Parameter	Description	7B131-15 7B141-15		7B131-20 7B141-20		Unit
		Min.	Max.	Min.	Max.	
<b>WRITE CYCLE<sup>[11]</sup></b>						
t <sub>WC</sub>	Write Cycle Time	15		20		ns
t <sub>SCE</sub>	CE LOW to Write End	12		15		ns
t <sub>AW</sub>	Address Set-Up to Write End	12		15		ns
t <sub>HA</sub>	Address Hold from Write End	2		2		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	R/W Pulse Width	12		15		ns
t <sub>SD</sub>	Data Set-Up to Write End	10		13		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	R/W LOW to High Z		10		13	ns
t <sub>LZWE</sub>	R/W HIGH to Low Z	3		3		ns
<b>BUSY/INTERRUPT TIMING</b>						
t <sub>BLA</sub>	BUSY LOW from Address Match		15		20	ns
t <sub>BHA</sub>	BUSY HIGH from Address Mismatch <sup>[12]</sup>		15		20	ns
t <sub>BLC</sub>	BUSY LOW from $\overline{CE}$ LOW		15		20	ns
t <sub>BHC</sub>	BUSY HIGH from $\overline{CE}$ HIGH <sup>[12]</sup>		15		20	ns
t <sub>PS</sub>	Port Set Up for Priority	5		5		ns
t <sub>WB</sub> <sup>[13]</sup>	R/W LOW after BUSY LOW	0		0		ns
t <sub>WH</sub>	R/W HIGH after BUSY HIGH	13		20		ns
t <sub>BDD</sub>	BUSY HIGH to Valid Data		15		20	ns
t <sub>DDD</sub>	Write Data Valid to Read Data Valid <sup>[14]</sup>		25		30	ns
t <sub>WDD</sub>	Write Pulse to Data Delay <sup>[14]</sup>		30		40	ns
<b>INTERRUPT TIMING</b>						
t <sub>WINS</sub>	R/W to INTERRUPT Set Time		15		20	ns
t <sub>EINS</sub>	CE to INTERRUPT Set Time		15		20	ns
t <sub>INS</sub>	Address to INTERRUPT Set Time		15		20	ns
t <sub>OINR</sub>	OE to INTERRUPT Reset Time <sup>[12]</sup>		15		20	ns
t <sub>EINR</sub>	CE to INTERRUPT Reset Time <sup>[12]</sup>		15		20	ns
t <sub>INR</sub>	Address to INTERRUPT Reset Time <sup>[12]</sup>		15		20	ns
<b>Notes:</b>						
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and R/W LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.						
12. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.						
13. CY7B141 only.						
14. For information on port-to-port delay through RAM cells, from writing port to reading port, refer to the Read Timing with Port-to-Port Delay timing diagram.						

**Switching Waveforms**
**Read Cycle No. 1 (Either Port—Address Access)<sup>[15, 16]</sup>**


B131- 5

**Read Cycle No. 2 (Either Port— $\overline{CE}/\overline{OE}$ )<sup>[15, 17]</sup>**


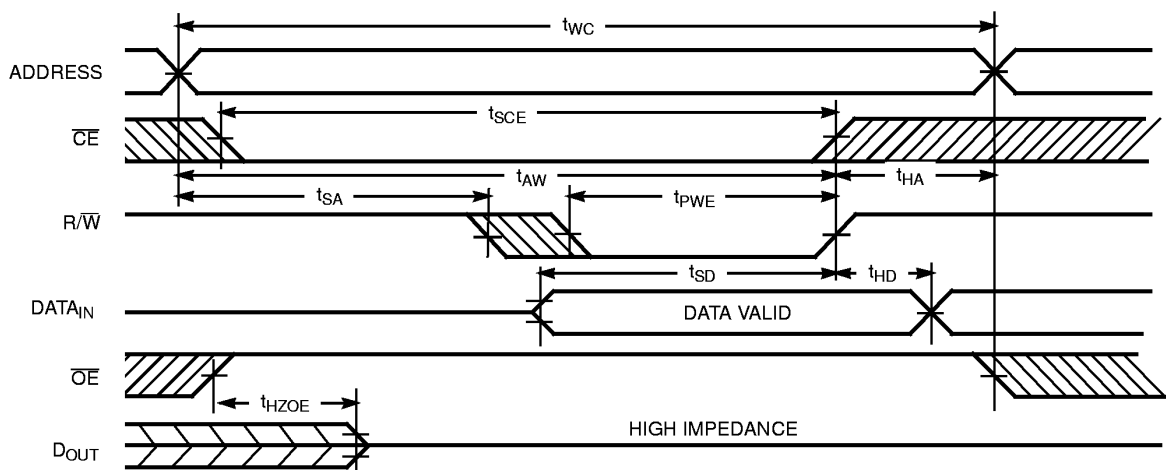
B131- 6

**Read Cycle No. 3 (Read with  $\overline{BUSY}$  Master: CY7B131)**


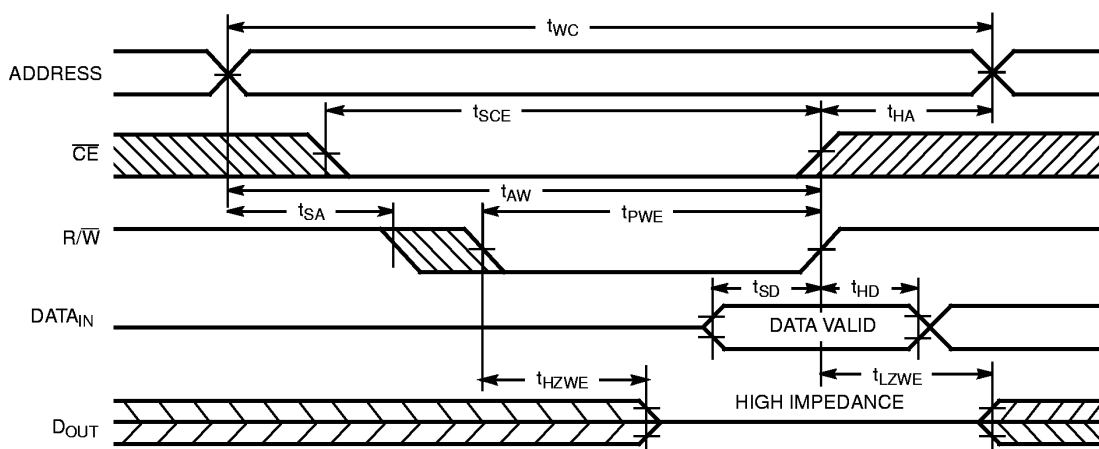
B131- 7

**Notes:**

15. R/ $\overline{W}$  is HIGH for read cycle.
16. Device is continuously selected,  $\overline{CE} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .
17. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms (Continued)**
**Write Cycle No. 1 (OE Three-States Data I/Os — Either Port)<sup>[11, 18]</sup>**


B131- 8

**Write Cycle No. 2 (R/E Three-States Data I/Os — Either Port)<sup>[11, 19]</sup>**


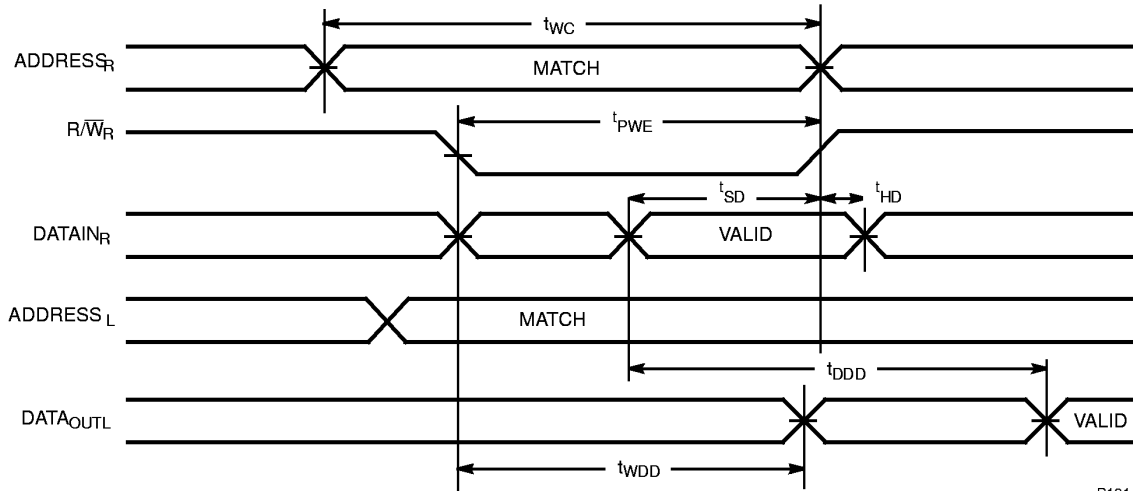
B131- 9

**Notes:**

18. If  $\overline{OE}$  is LOW during a R/W controlled write cycle, the write pulse width must be the larger of  $t_{PWE}$  or  $t_{HZWE} + t_{SD}$  to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required  $t_{SD}$ .
19. If the  $\overline{CE}$  LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in a high-impedance state.

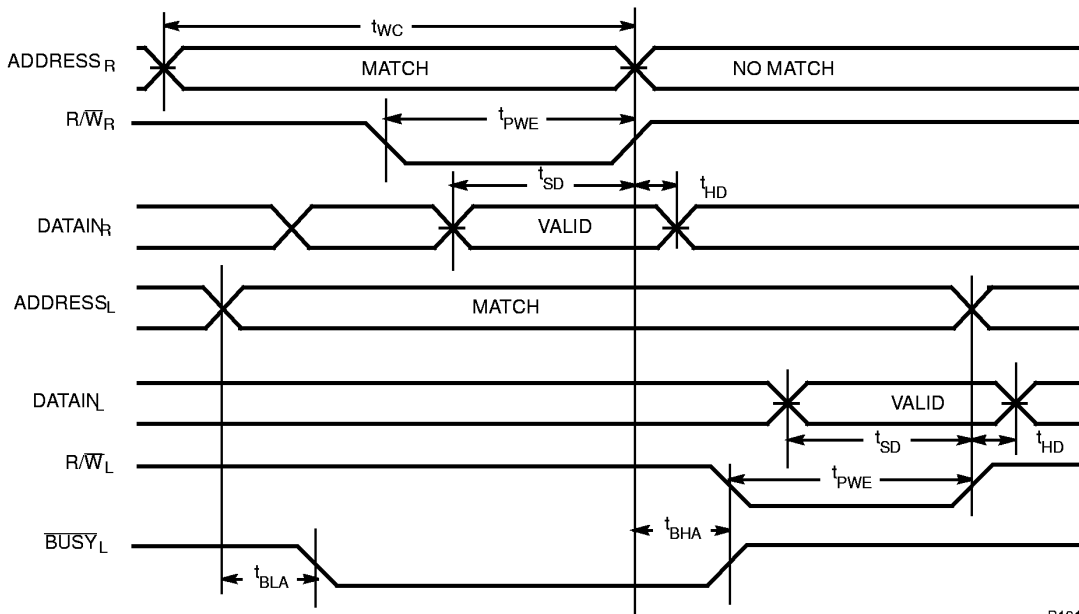
**Switching Waveforms (Continued)**

**Read Timing with Port-to-Port Delay ( $\overline{CE}_L = \overline{CE}_R = \text{LOW}$ ,  $\text{BUSY} = \text{HIGH}$  for the Writing Port)**



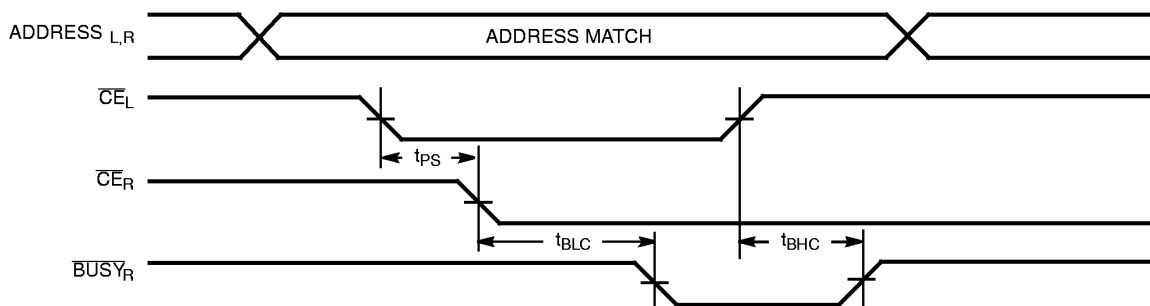
B131-10

**Write Timing with Port-to-Port Delay ( $\overline{CE}_L = \overline{CE}_R = \text{LOW}$ )**

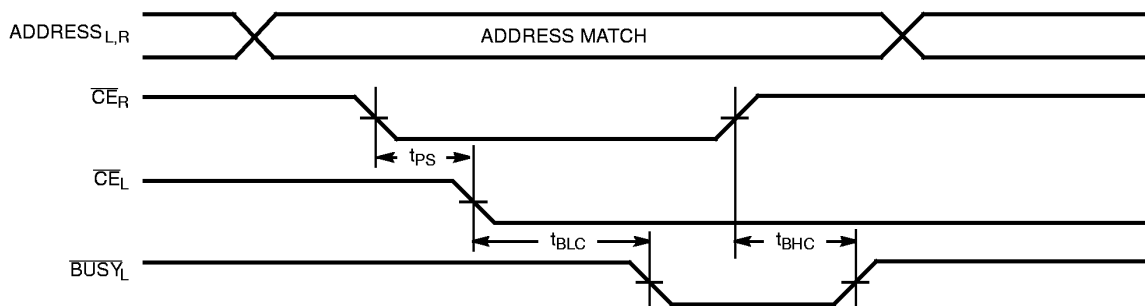


B131-11



**Switching Waveforms (Continued)**
**Busy Timing Diagram No. 1 ( $\overline{CE}$  Arbitration)**
 $\overline{CE}_L$  Valid First:


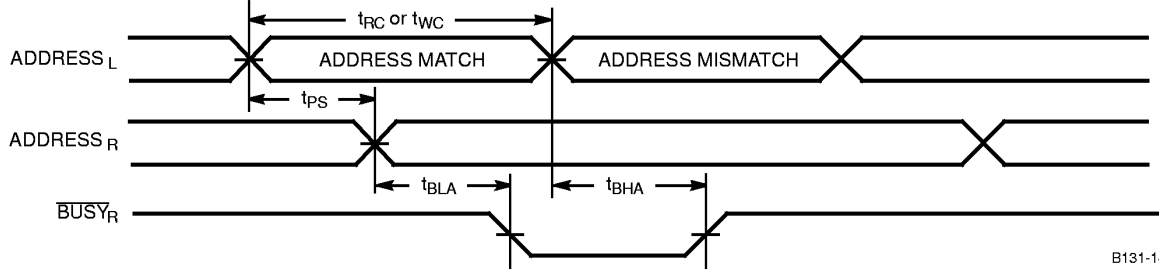
B131-12

 $\overline{CE}_R$  Valid First:


B131-13

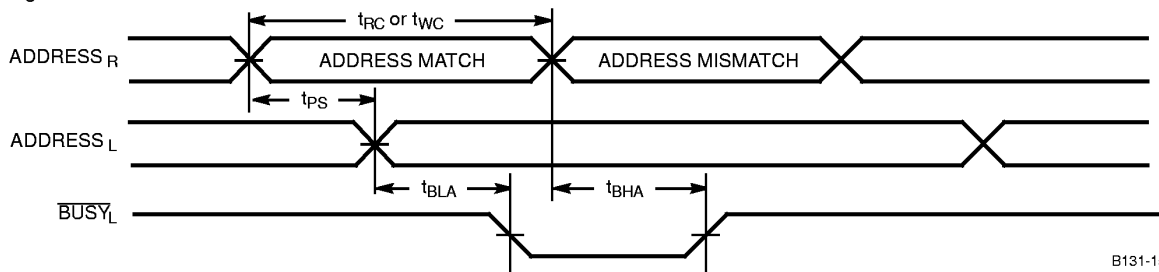
**Busy Timing Diagram No. 2 (Address Arbitration)**

Left Address Valid First:

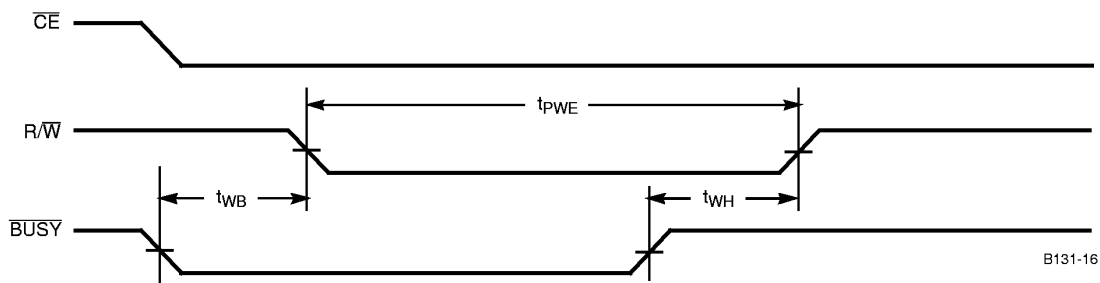
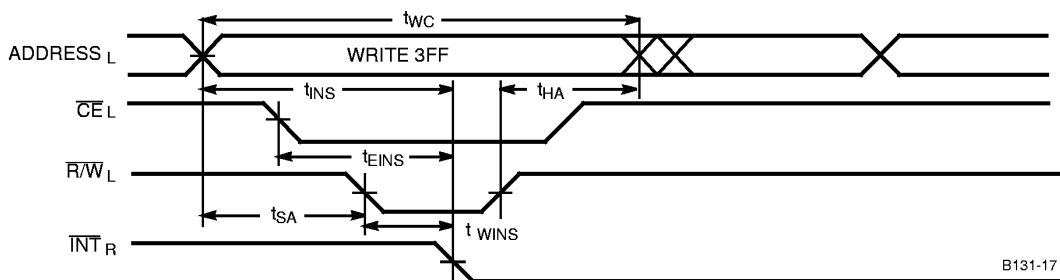
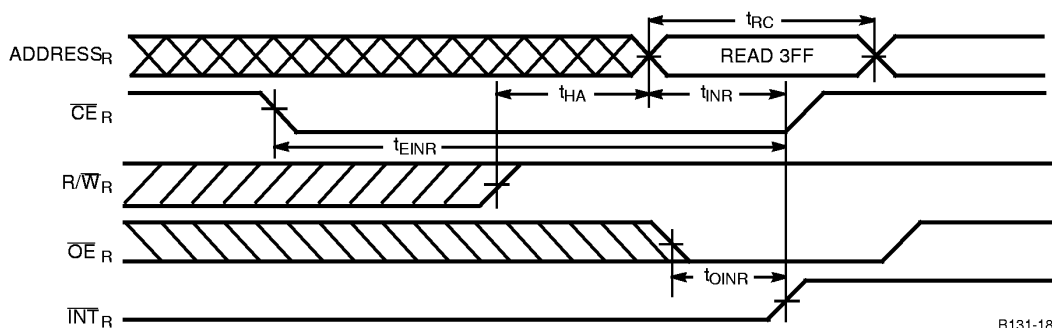
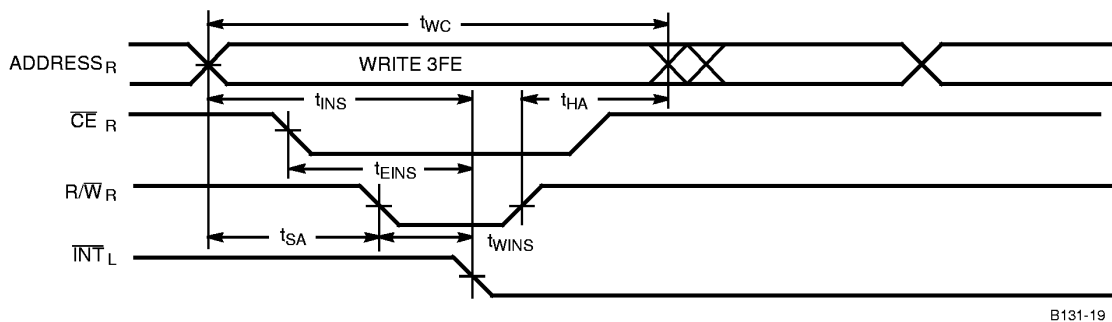


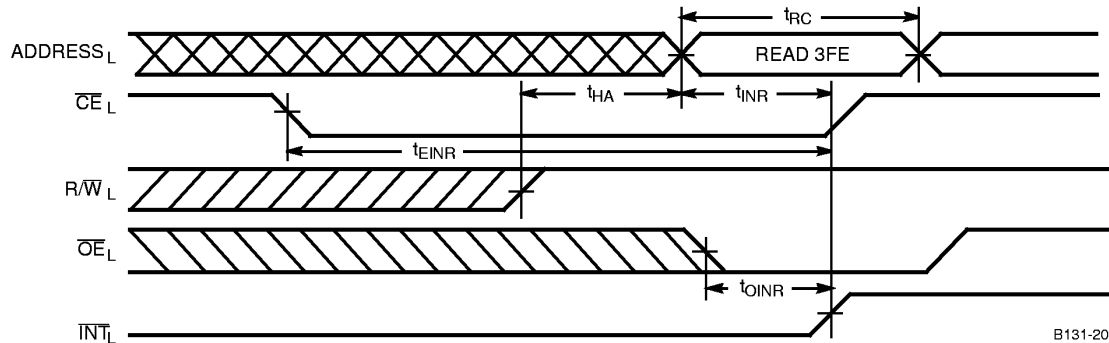
B131-14

Right Address Valid First:



B131-15

**Switching Waveforms (Continued)**
**Busy Timing Diagram No.3 (Write with  $\overline{\text{BUSY}}$ , Slave: CY7B141)**

**Intercept Timing Diagrams**
**Left Side Sets  $\overline{\text{INT}}_R$** 

**Right Side Clears  $\overline{\text{INT}}_R$** 

**Right Side Sets  $\overline{\text{INT}}_R$** 


**Intercept Timing Diagrams (Continued)**
**Left Side Sets  $\overline{INT}_R$** 

**Architecture**

The CY7B131 (master) and CY7B141 (slave) are 1024-byte deep dual-port RAMs, with two independent sets of address signals, common I/O data signals, and control signals. By convention, the two ports are called the left port and the right port. The subscript R or L on the signal name identifies the port.

The upper two memory locations (3FF, 3FE) are special locations and may be used as "mailboxes" for passing messages between the ports. Location 3FF is the mailbox for the right port and location 3FE is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner of the mailbox. When the owner reads the mailbox, the interrupt is reset.

The address and control signals provide independent, asynchronous, random access to any location in the memory. It is possible that both ports may attempt to access the same memory location at the same time. If this contention occurs, a circuit in the master called an arbiter decides which port temporarily "owns" the memory location. The losing port receives a BUSY signal, which notifies it that the memory location is owned by the other port and that the operation it attempted to perform may not be successful.

The two BUSY signals are outputs from the master and inputs to the slave.

**Contention, Arbitration and Resolution—  
The Significance of BUSY**

When contention occurs, the arbiter decides which port wins (owns) the memory location and which port loses. The decision is on a "first-come-first-served" basis. In order for contention to occur, both ports must address the same memory location and have their respective chip enables active. If one port precedes the other by an amount of time greater than or equal to  $t_{PS}$  (port set-up for priority; equal to five nanoseconds) it is guaranteed to win the arbitration. If contention occurs within the  $t_{PS}$  interval, it is not possible to predict which port will win, but one will win and the other will lose.

There are two ports and each may be either reading or writing, and each may win or lose, so there are eight combinations. They are listed in Table 1 and identified as cases one through

eight. In cases one and two, both ports are reading, the losing port receives a BUSY, the read is allowed to occur, and the data read by both ports is valid. In case three, the left port wins and reads valid data, and the write attempted by the right port is inhibited. In cases four and five, when the winning port is writing, the write is completed, but the data read by the losing port may be invalid. Case six is similar to case three; the right port successfully reads and the write attempt by the left port is inhibited. In cases seven and eight the winning port successfully writes and the attempted write by the losing port is inhibited.

In cases four and five, where the losing port is reading, if the port signals are asynchronous to each other, the data read may be the old data, the new data, or some random combination of the two sets of data. In cases seven and eight the losing port is prevented from writing. The commonality between these four cases is that the losing port receives a busy signal, which tells it that either (1) the operation it attempted was not successful, or (2) that the data it read may not be valid. In either situation, the operation should be repeated after the busy signal becomes inactive.

**Flow-Through Operation**

The CY7B131/141 have a flow-through architecture that facilitates repeating (actually extending) an operation when a BUSY is received by a losing port. The BUSY signal should be interpreted as a NOT READY. If a BUSY to a port is active, the port should wait for BUSY to go inactive, and then extend the operation it was performing for another cycle. The timing diagram titled, "Read Timing with Port-to-Port Delay" illustrates the case where the right port is writing to an address and the left port reads the same address. The data that the right port has just written flows through to the left, and is valid either  $t_{WDD}$  after the falling edge of the write strobe of the left port, or  $t_{DDD}$  after the data being written becomes stable.

The timing diagram titled, "Write Timing with Port-to-Port Delay" illustrates the case where the right port is writing to an address and the left port wants to write to the same address. If the left port extends its write strobe for a minimum time of  $t_{PWE}$  after the BUSY signal to it goes inactive, its write will be successful; it writes over the data just written by the right port.

### Data Bus Width Expansion Using Slaves

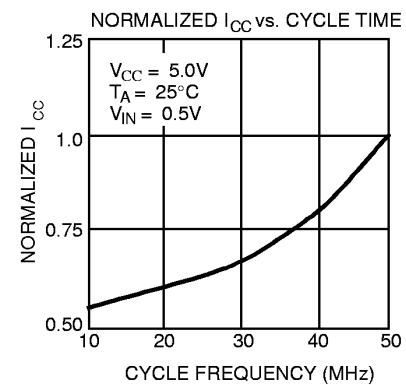
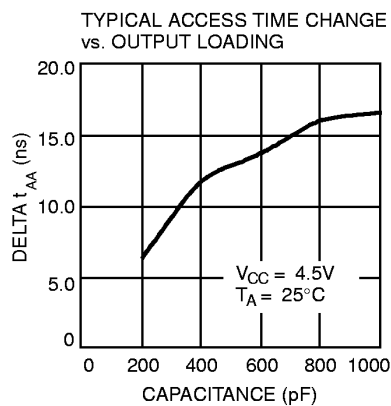
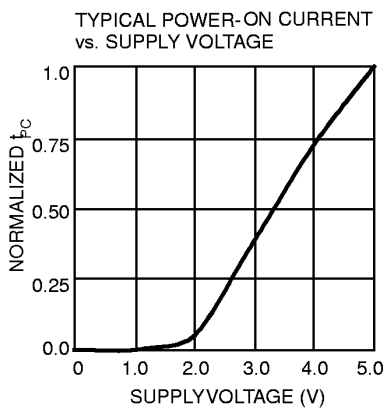
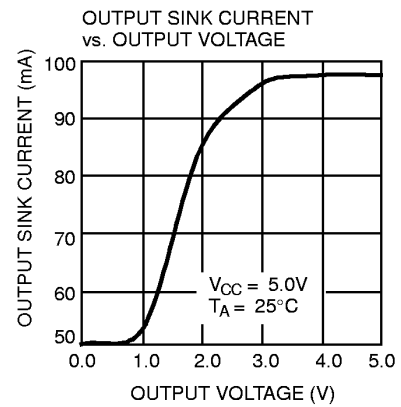
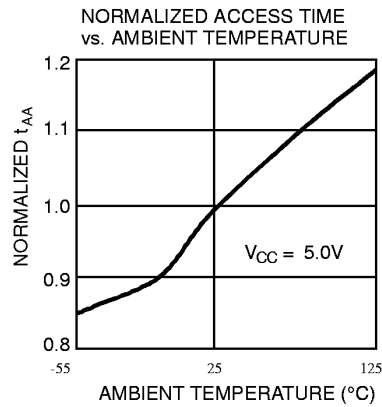
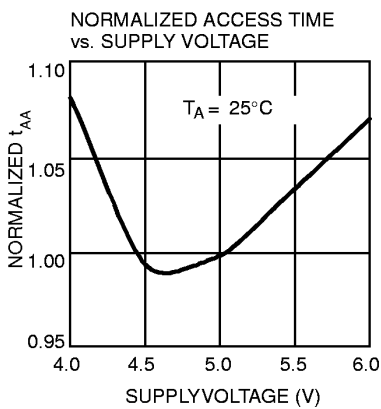
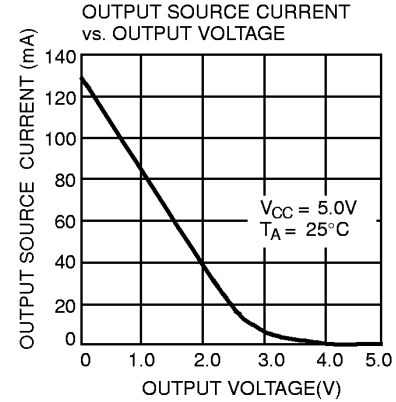
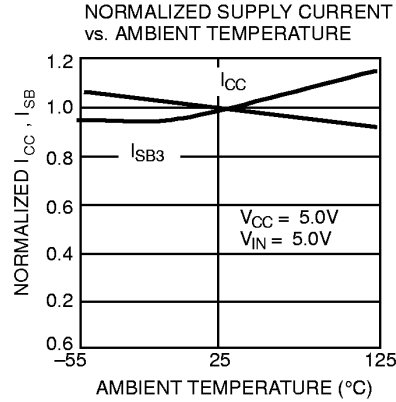
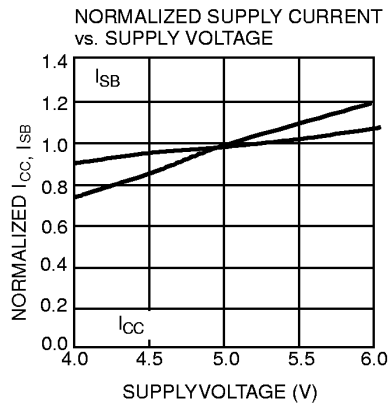
One master and as many slaves as necessary may be connected in parallel to expand the data bus width in byte increments.

Two masters must not be connected in parallel because, if the time interval between which they address the same location is less than  $t_{PS}$ , both could end up waiting for the other to release the BUSY to it.

Therefore, only one master must arbitrate, and it can drive as many slaves as required. The write strobe to the slaves must be delayed an amount of time equal to at least  $t_{BLA}$ . This insures that the slave is not inadvertently written to before the outcome of the arbitration is determined.

Table 1. Operation.

Case	Operation Port		Winning Port	Result
	L	R		
1	R	R	L	Both Read
2	R	R	R	Both Read
3	R	W	L	L Reads OK, R Write Inhibited
4	R	W	R	R Writes OK L Data May Be Invalid
5	W	R	L	L writes OK R Data May Be Invalid
6	W	R	R	R Reads OK L Write Inhibited
7	W	W	L	L Writes OK R Write Inhibited
8	W	W	R	R Writes OK L Write Inhibited

**Typical DC and AC Characteristics**




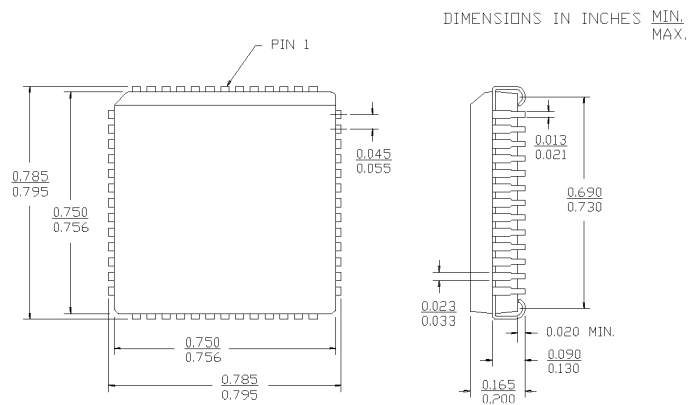
**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B131-15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
20	CY7B131-20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B131-20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

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**Package Diagram**

**52-Lead Plastic Leaded Chip Carrier J69**



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