CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7B138
CY7B139

4K x 8/9 Dual-Port Static RAM with Sem, Int, Busy

Features

- 0.8-micron BiCMOS for high performance
- High-speed access
  - —15 ns (com'l)
  - —25 ns (mil)
- Automatic power-down
- Fully asynchronous operation
- Master /Slave select pin allows bus width expansion to 16/18 bits or more
- Busy arbitration scheme provided
- Semaphores included to permit software handshaking between ports
- $\overline{INT}$ flag for port-to-port communication
- Available in 68-pin LCC/PLCC/PGA
- TTL compatible

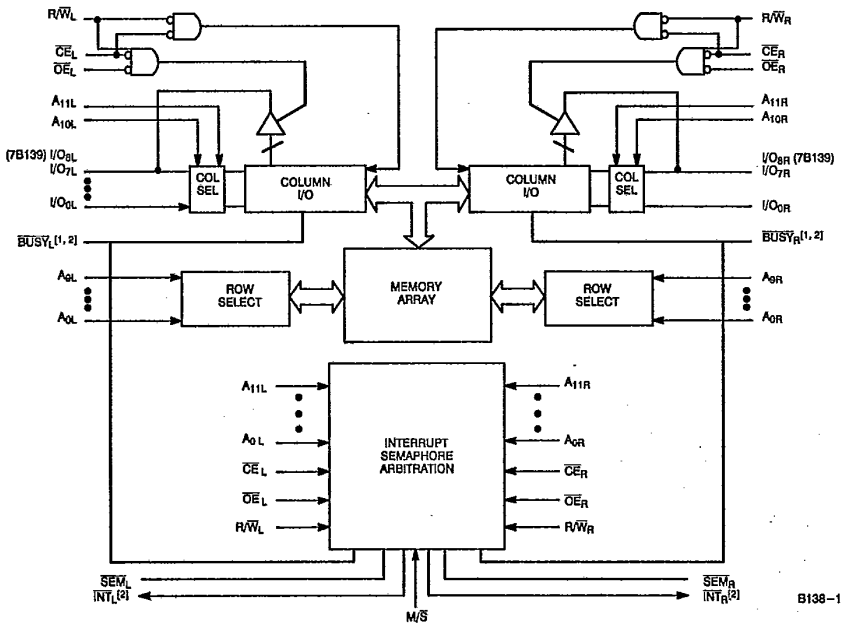
Functional Description

The CY7B138 and CY7B139 are high-speed BiCMOS 4K x 8 and 4K x 9 dual-port static RAMs. Various arbitration schemes are included on the CY7B138/9 to handle situations when multiple processors access the same piece of data. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. The CY7B138/9 can be utilized as a standalone 64-Kbit dual-port static RAM or multiple devices can be combined in order to function as a 16/18-bit or wider master/slave dual-port static RAM. An $M/\overline{S}$ pin is provided for implementing 16/18-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable ($R/\overline{W}$), and output enable ($\overline{OE}$). Two flags are provided on each port ($\overline{BUSY}$ and $\overline{INT}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of mail box or message center. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin.

The CY7B138 and CY7B139 are available in 68-pin LCCs, PLCCs, and PGAs.

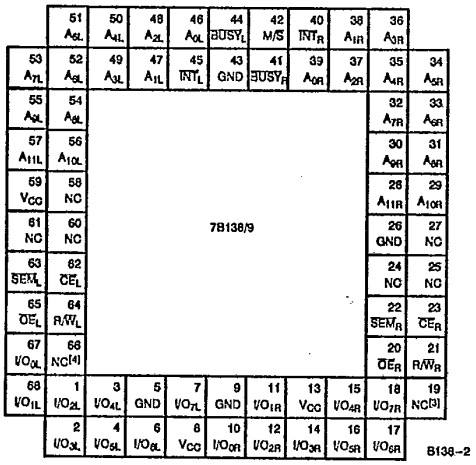
Logic Block Diagram



Notes:
1. $\overline{BUSY}$ is an output in master mode and an input in slave mode.
2. Master: push-pull output and requires no pull-up resistor.

Pin Configurations

68-Pin PGA
Top View



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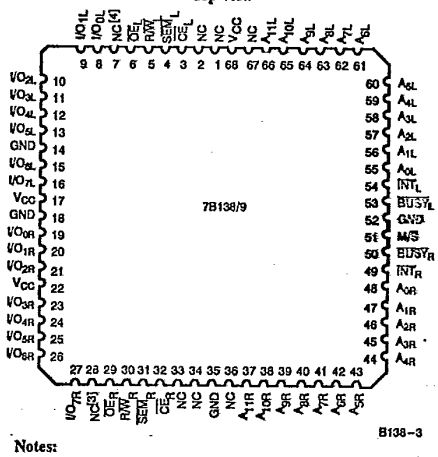
68-Pin LCC/PLCC
Top View



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Notes:
3. I/O_{8R} on the CY7B139.
4. I/O_{8L} on the CY7B139.

Pin Definitions

Left Port	Right Port	Description
$I/O_{0L-7L(8L)}$	$I/O_{0R-7R(8R)}$	Data Bus Input/Output
A_{0L-11L}	A_{0R-11R}	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag. $\overline{INT}_L$ is set when right port writes location FFE and is cleared when left port reads location FFE. $\overline{INT}_R$ is set when left port writes location FFF and is cleared when right port reads location FFF.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

Selection Guide

		7B138–15 7B139–15	7B138–25 7B139–25	7B138–35 7B139–35
Maximum Access Time (ns)		15	25	35
Maximum Operating Current (mA)	Commercial	260	220	210
	Military		280	250
Maximum Standby Current for I_{SB1}(mA)	Commercial	90	75	70
	Military		80	75

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to + 150°C

Ambient Temperature with Power Applied ..... – 55°C to + 125°C

Supply Voltage to Ground Potential ..... – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to + 7.0V

DC Input Voltage[5] ..... – 3.5V to + 7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Industrial	–40°C to + 85°C	5V ± 10%
Military[6]	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[7]

Parameter	Description	Test Conditions		7B138–15 7B139–15 Min.	7B138–15 7B139–15 Max.	7B138–25 7B139–25 Min.	7B138–25 7B139–25 Max.	7B138–35 7B139–35 Min.	7B138–35 7B139–35 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2..4		2..4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–10	+10	–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	Output Disabled, GND ≤ V_O ≤ V_{CC}		–10	+10	–10	+10	–10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, Outputs Disabled	Com'l		260		220		210	mA
			Mil/Ind				280		250	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		90		75		70	mA
			Mil/Ind				80		75	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[8]	Com'l		160		140		130	mA
			Mil/Ind				180		160	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0[8]	Com'l		15		15		15	mA
			Mil/Ind				30		30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[8]	Com'l		140		120		110	mA
			Mil/Ind				150		130	

Capacitance[9]

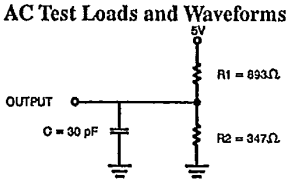
Parameters	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		15	pF

Notes:

5. Pulse width < 20 ns.
6. T_A is the "instant on" case temperature.
7. See the last page of this specification for Group A subgroup testing information.
8. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.
9. Tested initially and after any design or process changes that may affect these parameters.

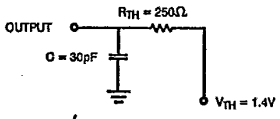
AC Test Loads and Waveforms

T-46-23-12



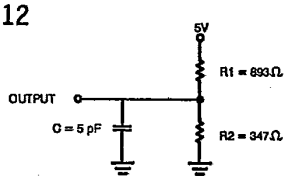
(a) Normal Load (Load 1)

B138–4



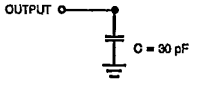
(b) Thevenin Equivalent (Load 1)

B138–5



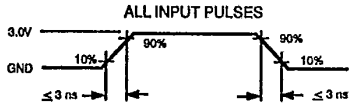
(c) Three-State Delay (Load 3)

B138–6



Load (Load 2)

B138–7



B138–8

Switching Characteristics Over the Operating Range[10,11]

Parameters	Description	7B138–15 7B139–15 Min.	Max.	7B138–25 7B139–25 Min.	Max.	7B138–35 7B139–35 Min.	Max.	Units
READ CYCLE								
t_{RC}	Read Cycle Time	15		25		35		ns
t_{AA}	Address to Data Valid[12]		15		25		35	ns
t_{OHA}	Output Hold From Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[12]		15		25		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[12]		10		15		20	ns
t_{LZOE}[13]	$\overline{OE}$ Low to Low Z	3		3		3		ns
t_{HZOE}[13]	$\overline{OE}$ HIGH to High Z		10		15		20	ns
t_{LZCE}[13]	$\overline{CE}$ LOW to Low Z	3		3		3		ns
t_{HZCE}[13]	$\overline{CE}$ HIGH to High Z		10		15		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		25		35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	15		25		35		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		20		30		ns
t_{AW}	Address Set-Up to Write End	12		20		30		ns
t_{HA}	Address Hold From Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	Write Pulse Width	12		20		25		ns
t_{SD}	Data Set-Up to Write End	10		15		15		ns
t_{HD}	Data Hold From Write End	0		0		0		ns
t_{HZWE}[13]	R/$\overline{W}$ LOW to High Z		10		15		20	ns
t_{LZWE}[13]	R/$\overline{W}$ HIGH to Low Z	3		3		3		ns
t_{WDD}[14]	Write Pulse to Data Delay		30		50		60	ns
t_{DDD}[14]	Write Data Valid to Read Data Valid		25		30		35	ns

Switching Characteristics Over the Operating Range[10, 11] (continued)

Parameters	Description	7B138–15 7B139–15		7B138–25 7B139–25		7B138–35 7B139–35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING[15]								
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20		20	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		15		20		20	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20		20	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		15		20		20	ns
t_{PS}	Port Set-Up for Priority		5		5		5	ns
t_{WB}	$\overline{WE}$ LOW after $\overline{BUSY}$ LOW		0		0		0	ns
t_{WH}	$\overline{WE}$ HIGH after $\overline{BUSY}$ HIGH		13		20		30	ns
t_{BDD}	$\overline{BUSY}$ HIGH to Data Valid		15		25		35	ns
INTERRUPT TIMING[15]								
t_{INS}	$\overline{INT}$ Set Time		15		25		25	ns
t_{INR}	$\overline{INT}$ Reset Time		15		25		25	ns
SEMAPHORE TIMING								
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		15		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		ns

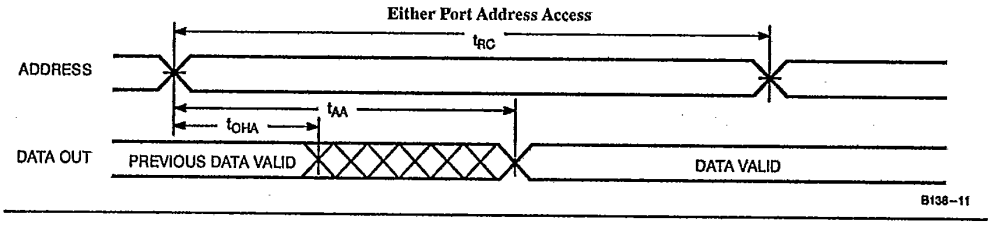
Notes:

10. See the last page of this specification for Group A subgroup testing information.
11. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
12. AC test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
13. Test conditions used are Load 3.
14. For information on part-to-part delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.
15. Test conditions used are Load 2.

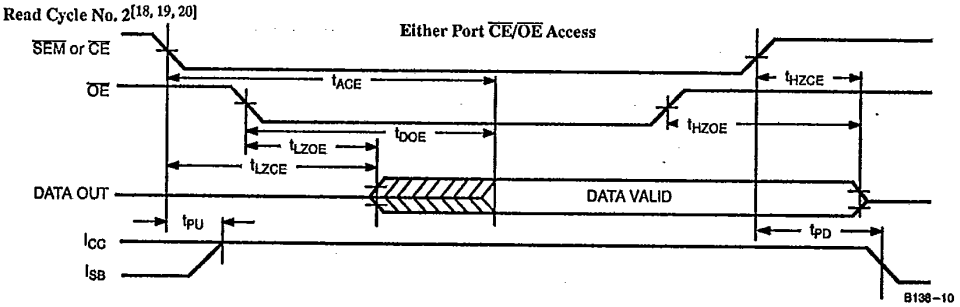
Switching Waveforms

T-46-23-12

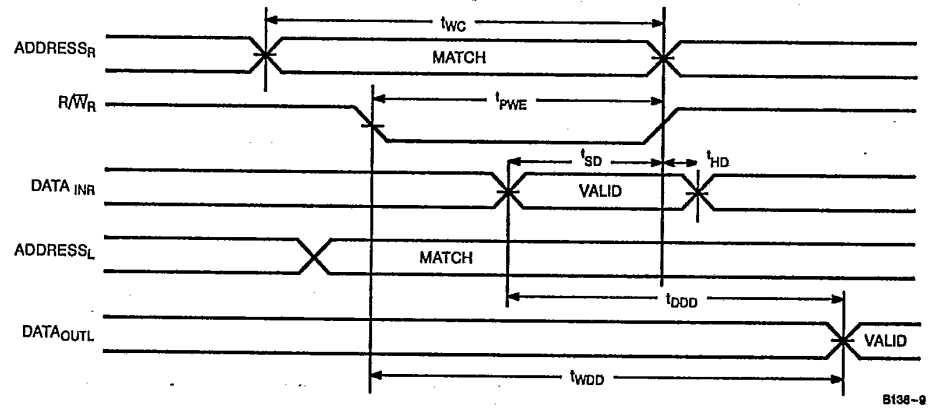
Read Cycle No. 1[20, 21]



Read Cycle No. 2[18, 19, 20]



Read Timing with Port-to-Port Delay (M/S = L)[16, 17]



Notes:
16. $\overline{BUSY}$ = HIGH for the writing port.
17. $\overline{CE}_L = \overline{CE}_R$ = LOW.
18. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
19. $\overline{CE}_L$ = L, $\overline{SEM}$ = H when accessing RAM. $\overline{CE}$ = H, $\overline{SEM}$ = L when accessing semaphores.
20. R/$\overline{W}$ is HIGH for read cycle.
21. Device is continuously selected $\overline{CE}$ = LOW and $\overline{OE}$ = LOW. This waveform cannot be used for semaphore reads.

Switching Waveforms (continued)

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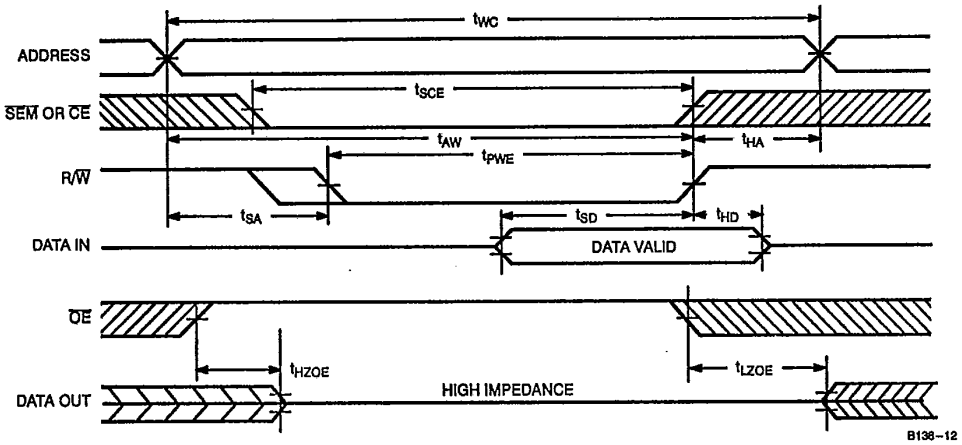
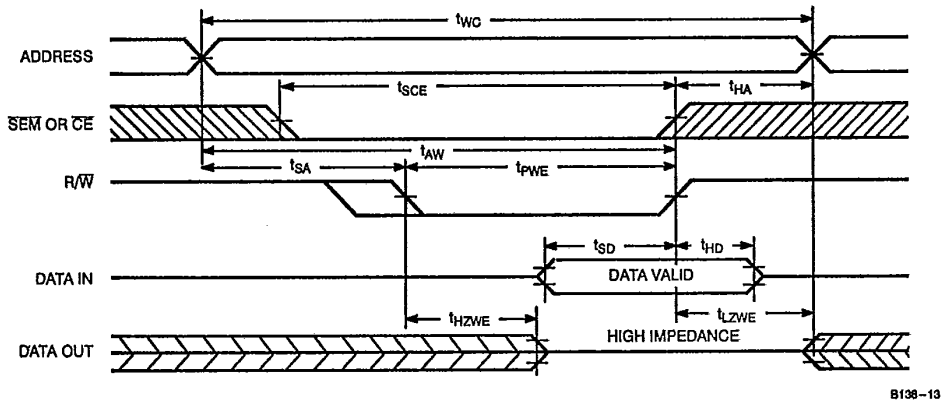
Write Cycle No. 1: $\overline{OE}$ Three-States Data I/Os (Either Port)[22, 23, 24]



Write Cycle No. 2: R/$\overline{W}$ Three-States Data I/Os (Either Port)[22, 24, 25]

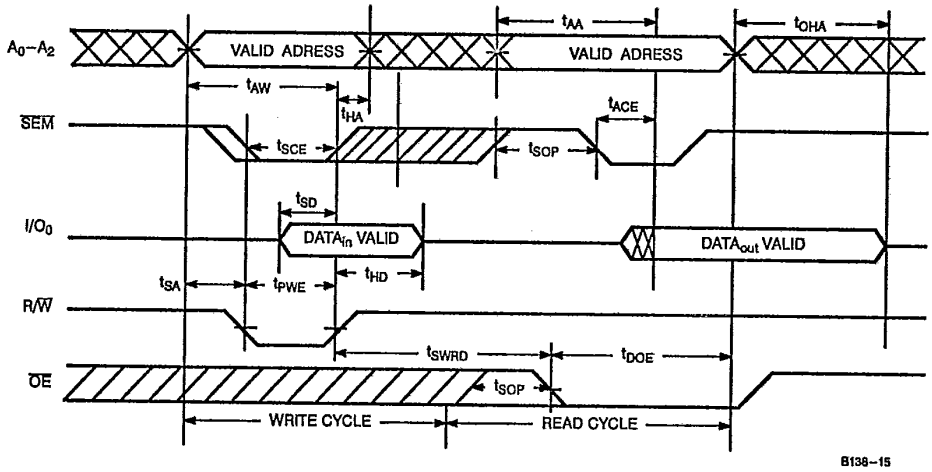


Notes:

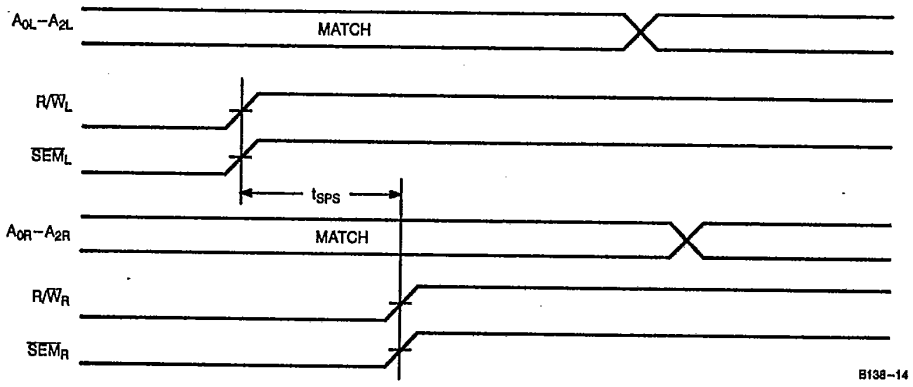
22. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
23. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
24. R/$\overline{W}$ must be HIGH during all address transitions.
25. Data I/O pins enter high impedance when $\overline{OE}$ is held LOW during write.

Switching Waveforms (continued)

Semaphore Read After Write Timing, Either Side[29]



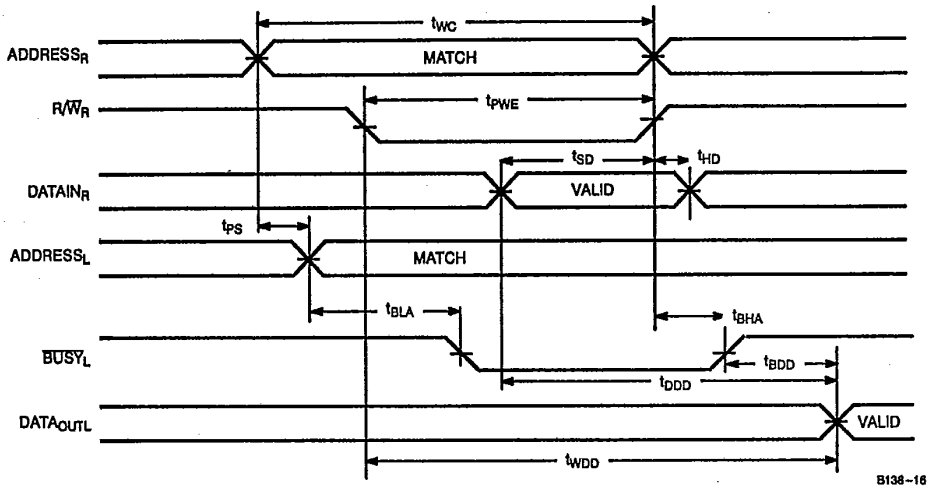
Timing Diagram of Semaphore Contention[26, 27, 28]



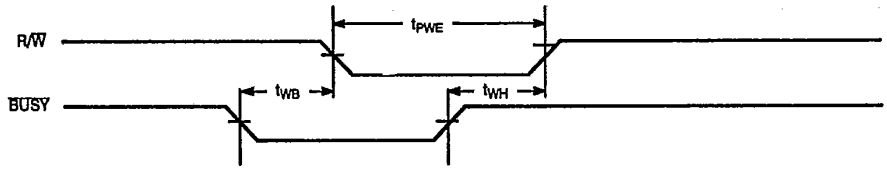
Notes:
26. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH
27. Semaphores are reset (available to both ports) at cycle start.
28. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.
29. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).

Switching Waveforms (continued) T-46-23-12

Timing Diagram of Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[17]



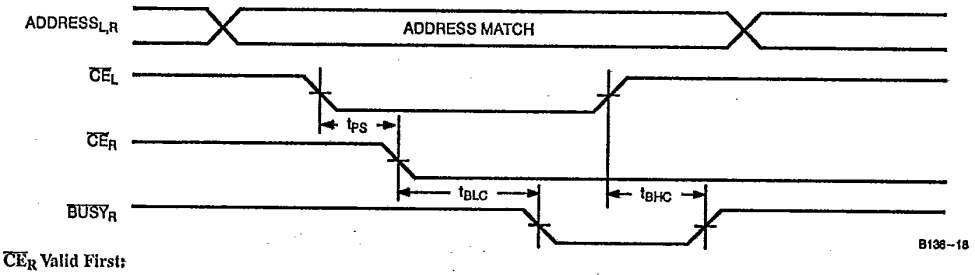
Write Timing with Busy Input (M/$\overline{S}$=LOW)



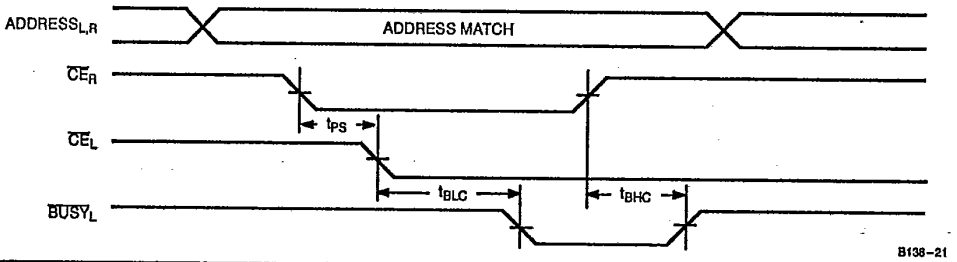
Switching Waveforms (continued)

Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[30]

$\overline{CE}_L$ Valid First:

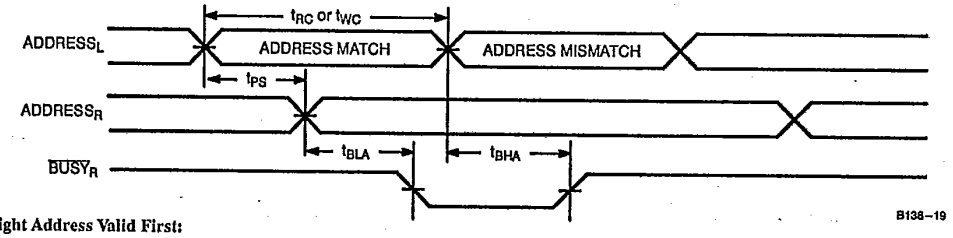


$\overline{CE}_R$ Valid First:

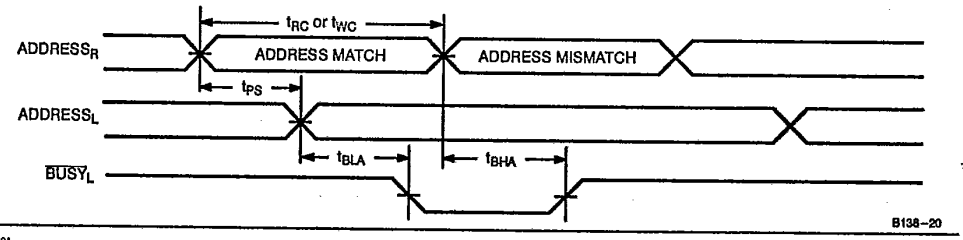


Busy Timing Diagram No. 2 (Address Arbitration)[30]

Left Address Valid First:



Right Address Valid First:



Note:
30. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted.

Switching Waveforms (continued)

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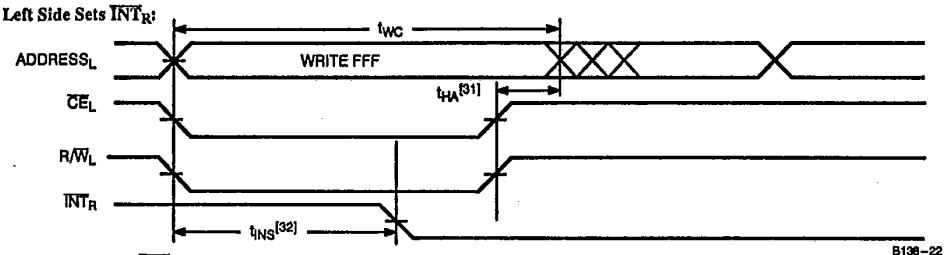
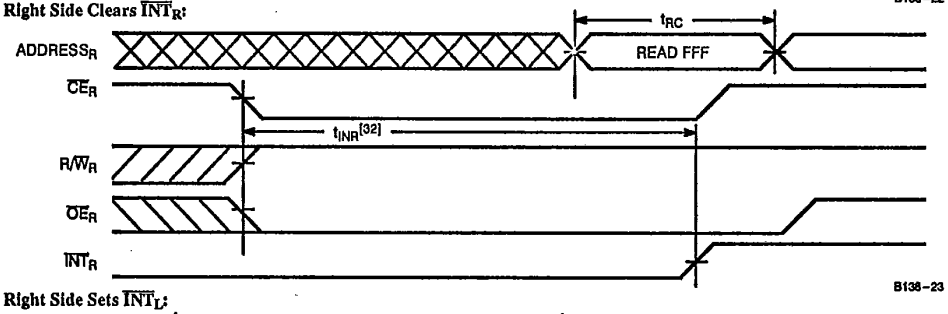
Interrupt Timing Diagrams

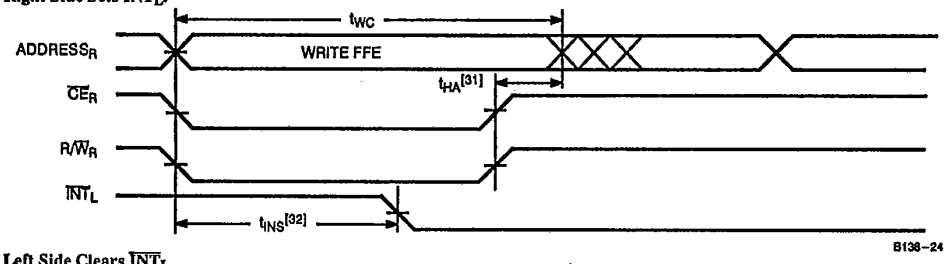
Left Side Sets $\overline{INT}_R$:



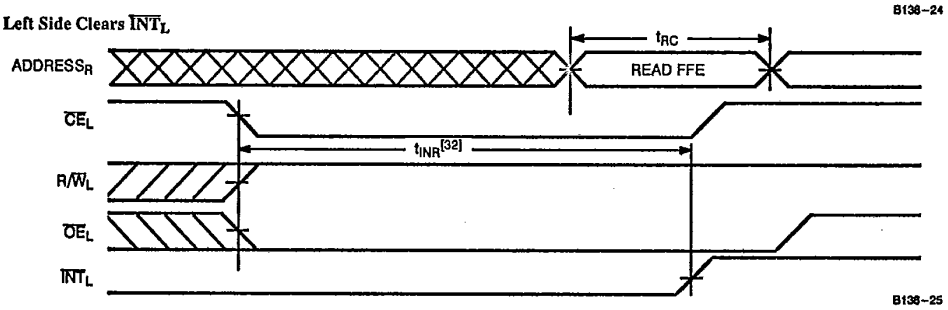
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$



Notes:

31. t_{HA} depends on which enable pin ($\overline{CE}_L$ or R/$\overline{W}_L$) is deasserted first.
32. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or R/$\overline{W}_L$) is asserted last.

Architecture

The CY7B138/9 consists of an array of 4K words of 8/9 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. Two interrupt ($\overline{INT}$) pins can be utilized for port-to-port communication. Two semaphore ($\overline{SEM}$) control pins are used for allocating shared resources. With the M/$\overline{S}$ pin, the CY7B138/9 can function as a master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). The CY7B138/9 has an automatic power-down feature controlled by $\overline{CE}$. Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. A write operation is controlled by either the $\overline{OE}$ pin (see Write Cycle No. 1 waveform) or the R/$\overline{W}$ pin (see Write Cycle No. 2 waveform). Data can be written to the device t_{HZOE} after the $\overline{OE}$ is deasserted or t_{HZWE} after the falling edge of R/$\overline{W}$. Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output. Data will be valid on the port wishing to read the location t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ is asserted. If the user of the CY7B138/9 wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin.

Interrupts

The interrupt flag ($\overline{INT}$) permits communications between ports. When the left port writes to location FFF, the right port's interrupt flag ($\overline{INT_R}$) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag ($\overline{INT_L}$) is accomplished when the right port writes to location FFE. This flag is cleared when the left port reads location FFE. The message at FFF or FFE is user-defined. See *Table 2* for input requirements for $\overline{INT}$. $\overline{INT_R}$ and $\overline{INT_L}$ are push-pull outputs and do not require pull-up resistors to operate. $\overline{BUSY_L}$ and $\overline{BUSY_R}$ in master mode are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7B138/9 provides on-chip arbitration to alleviate simultaneous memory location access (contention). If both ports' $\overline{CE}$s are asserted or an address match occurs within t_{PS} of each other the Busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. $\overline{BUSY}$ will be asserted t_{BLA} after an address match or t_{BLC} after $\overline{CE}$ is taken LOW.

Master/Slave

A M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. This will allow the device to interface to a master device with no external components. Writing of slave devices must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation. When presented as a HIGH input, the M/$\overline{S}$ pin allows the device to be used as a master and therefore the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7B138/9 provides eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control over the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the a semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches ($\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW). A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a zero is written to the left port of an unused semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Table 1. Non-Contending Read/Write

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O_{0-7}	Operation
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read Data in Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H	⌐	X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L$=$\overline{BUSY}_R$=HIGH)

	Left Port					Right Port				
Function	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0-11}	$\overline{INT}$	R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	A_{0-11}	$\overline{INT}$
Set Left $\overline{INT}$	X	X	X	X	L	L	L	X	FFE	X
Reset Left $\overline{INT}$	X	L	L	FFE	H	X	X	X	X	X
Set Right $\overline{INT}$	L	L	X	FFF	X	X	X	X	X	L
Reset Right $\overline{INT}$	X	X	X	X	X	X	L	L	FFF	H

Table 3. Semaphore Operation Example

Function	I/O 0 Left	I/O 0 Right	Status
No action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7B138–15GC	G68	Commercial
	CY7B138–15JC	J81	
	CY7B138–15LC	L81	
25	CY7B138–25GC	G68	Commercial
	CY7B138–25JC	J81	
	CY7B138–25LC	L81	
	CY7B138–25JI	J81	Industrial
	CY7B138–25GMB	G68	Military
	CY7B138–25LMB	L81	
35	CY7B138–35GC	G68	Commercial
	CY7B138–35JC	J81	
	CY7B138–35LC	L81	
	CY7B138–35JI	J81	Industrial
	CY7B138–35GMB	G68	Military
	CY7B138–35LMB	L81	

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7B139–15GC	G68	Commercial
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	CY7B139–15LC	L81	
25	CY7B139–25GC	G68	Commercial
	CY7B139–25JC	J81	
	CY7B139–25LC	L81	
	CY7B139–25JI	J81	Industrial
	CY7B139–25GMB	G68	Military
	CY7B139–25LMB	L81	
35	CY7B139–35GC	G68	Commercial
	CY7B139–35JC	J81	
	CY7B139–35LC	L81	
	CY7B139–35JI	J81	Industrial
	CY7B139–35GMB	G68	Military
	CY7B139–35LMB	L81	

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MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11
t_{DDD}	7, 8, 9, 10, 11
t_{WDD}	7, 8, 9, 10, 11

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