PRELIMINARY

CY7B9331

HOTLink™ OLC Receiver

Features

- **Fibre Channel compliant**
- **IBM ESCON™ compliant**
- **OLC Compatible system interface**
- **8B/10B-coded or 10-bit unencoded**
- **160- to 330-Mbps data rate**
- **No external PLL components**
- **Dual ECL 100K serial inputs**
- **Low power: 650 mW**
- **Compatible with fiberoptic modules, coaxial cable, and twisted pair media**
- **Built-In Self-Test**
- **28-pin SOIC/PLCC**

Functional Description

The CY7B9331 HOTLink OLC Receiver is a point-to-point communications building block that receives data over high-speed serial links (fiber, coax, and twisted pair) at 160 to 330 Mbits/second. The HOTLink OLC Receiver system interface has been tailored to match OLC (Optical Link Card) timing and functionality.

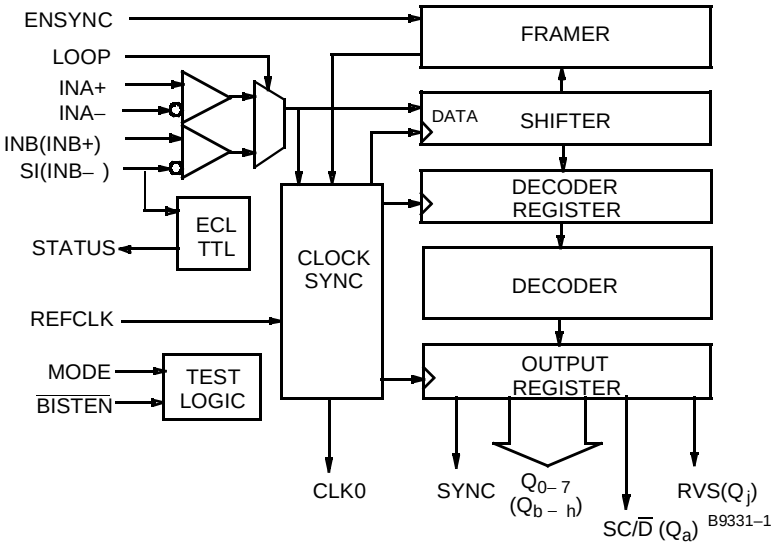
The HOTLink receiver accepts the serial bit stream at its differential line receiver inputs and, using a completely integrated PLL clock synchronizer, recovers the timing information necessary for data reconstruction.

The bit stream is deserialized, decoded, and checked for transmission errors. The recovered byte is presented in parallel to the receiving host along with a byte rate clock.

The 8B/10B encoder/decoder can be disabled in systems that already encode or scramble the transmitted data. A Built-In Self-Test pattern generator and checker allows testing of the transmitter, receiver, and the connecting link as a part of a system diagnostic check.

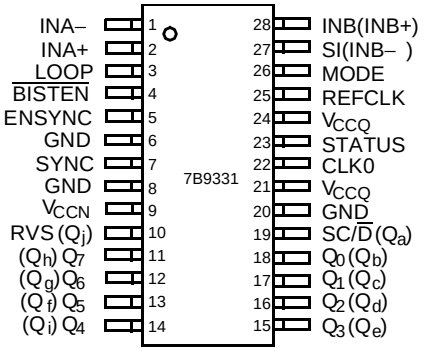
The CY7B9331 HOTLink Receiver is a companion part to the CY7B923 HOTLink Transmitter. The HOTLink chip set provides a complete physical interface solution. For further information on HOTLink Transceiver and Receiver functions see the CY7B923/933 datasheet.

Receiver Logic Block Diagram

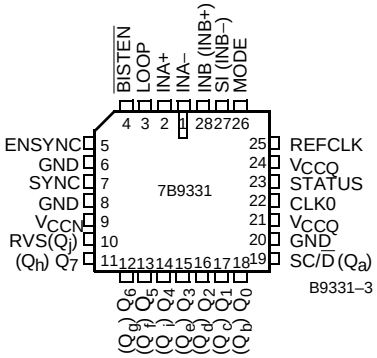


Pin Configurations

SOIC
Top View



PLCC
Top View



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CY7B9331 HOTLink Receiver Pin Description

Name	I/O	Description
Q_{0-7} (Q_{b-h})	TTL Out	Q_{0-7} Parallel Data Output. Q_{0-7} contain the most recently received data. These outputs change synchronously with Clk0. When MODE is HIGH, $Q_{0, 1, ...7}$ become $Q_{b, c,...h}$ respectively.
SC/$\overline{D}$ (Q_a)	TTL Out	Special Character/Data Select. SC/$\overline{D}$ indicates the context of received data. HIGH indicates a Control (Special Character) code, LOW indicates a Data character. When MODE is HIGH, SC/$\overline{D}$ acts as Q_a output.
RVS (Q_j)	TTL Out	Received Violation Symbol. A HIGH on RVS indicates that a code rule violation has been detected in the received data stream. A LOW shows that no error has been detected. In BIST mode, a LOW on RVS indicates correct operation of the transmitter, receiver, and link on a byte-by-byte basis. When MODE is HIGH, RVS acts as Q_j output.
SYNC	TTL Out	In Encoded mode, SYNC asserted HIGH indicates that new data has been received and is ready to be delivered. SYNC asserted LOW shows that the received data is the Null character (normally inserted by the transmitter as a pad between data inputs). In Bypass mode, SYNC stays LOW except to indicate a K28.5 character when the framer is enabled (ENSYNC HIGH). In BIST mode, SYNC will remain HIGH for all but the last byte of a test loop and will pulse LOW one byte time per BIST loop.
CLK0	TTL Out	Recovered Byte Clock. This byte rate clock output is phase and frequency aligned to the incoming serial data stream. SYNC, Q_{0-7}, SC/$\overline{D}$, and RVS all switch synchronously with the rising edge of this output.
LOOP	ECL in	Serial Data Input Select. This ECL 100K (+5V referenced) input selects INB or INA as the active data input. If LOOP is HIGH, INB is connected to the shifter and signals connected to INB will be decoded. If LOOP is LOW INA is selected.
INA±	Diff In	Serial Data Input A. The differential signal at the receiver end of the communication link may be connected to the differential input pairs INA± or INB±. Either the INA pair or the INB pair can be used as the main data input and the other can be used as a loopback channel or as an alternative data input selected by the state of LOOP.
INB (INB+)	ECL in (Diff In)	Serial Data Input B. This pin is either a single-ended ECL data receiver (INB) or half of the INB of the differential pair. If STATUS is wired to V_{CC}, then INB± can be used as differential line receiver interchangeably with INA±. If STATUS is normally connected and loaded, INB becomes a single-ended ECL 100K (+5V referenced) serial data input. INB is used as the test clock while in Test mode.
SI (INB–)	ECL in (Diff In)	Status Input. This pin is either a single-ended ECL status monitor input (SI) or half of the INB of the differential pair. If STATUS is wired to V_{CC}, then INB± can be used as differential line receiver interchangeably with INA±. If STATUS is normally connected and loaded, SI becomes a single-ended ECL 100K (+5V referenced) status monitor input.
STATUS	TTL Out	Status Out. Status is the inverted TTL-translated output of SI. It is typically used to translate the Carrier Detect output from a fiberoptic receiver. When this pin is normally connected and loaded (without any external pull-up resistor), STATUS will assume the negative logical level of SI and INB will become a single-ended ECL serial data input. If the status monitor translation is not desired, then STATUS may be wired to V_{CC} and the INB± pair may be used as a differential serial data input.
ENSYNC	TTL In	Reframe Enable. ENSYNC controls the Framer logic in the receiver. When ENSYNC is held HIGH, each SYNC (K28.5) symbol detected in the shifter will frame the data that follows. When ENSYNC is held LOW, the reframing logic is disabled. The incoming data stream is then continuously deserialized and decoded using byte boundaries set by the internal byte counter. Bit errors in the data stream will not cause alias SYNC characters to reframe the data erroneously.
REFCLK	TTL In	Reference Clock. REFCLK is the clock frequency reference for the clock/data synchronizing PLL. REFCLK sets the approximate center frequency for the internal PLL to track the incoming bit stream. REFCLK must be connected to a crystal-controlled time base that runs within the frequency limits of the Tx/Rx pair, and the frequency must be the same as the transmitter CKW frequency (within CKW±0.1%).
MODE	3-Level In	Decoder Mode Select. The level on the MODE pin determines the decoding method to be used. When wired to GND (Encoded Mode), MODE selects 8B/10B decoding. When wired to V_{CC} (Bypass MODE), registered shifter contents bypass the decoder and are sent to Q_{a-j} directly. When left floating (internal resistors hold the MODE pin at $V_{CC}/2$) the internal bit clock generator is disabled and INB becomes the bit rate test clock to be used for factory test. In typical applications, MODE is wired to V_{CC} or GND.

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CY7B9331 HOTLink Receiver Pin Description (continued)

Name	I/O	Description
$\overline{\text{BISTEN}}$	TTL In	Built-In Self-Test Enable. When $\overline{\text{BISTEN}}$ is LOW the receiver awaits a D0.0 (sent once per BIST loop) character and begins a continuous test sequence that tests the functionality of the transmitter, the receiver, and the link connecting them. In BIST mode the status of the test can be monitored with Sync and RVS outputs. In normal use $\overline{\text{BISTEN}}$ is held HIGH or wired to V_{CC}.
V_{CCN}		Power for output drivers.
V_{CCQ}		Power for internal circuitry.
GND		Ground

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

Output Current into TTL Outputs (LOW) ..... 30 mA

Output Current into ECL outputs (HIGH) ..... –50 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
Receiver TTL-Compatible Pins: Q_{0-7}, SC/$\overline{D}$, RVS, Sync, Clk0, REFCLK, EnSync, $\overline{\text{BISTEN}}$, Status					
V_{OHT}	Output HIGH Voltage	I_{OH} = – 2 mA	2.4		V
V_{OLT}	Output LOW Voltage	I_{OL} = 4 mA		0.45	V
I_{OST}	Output Short Circuit Current	V_{OUT} =0V[1]	–15	–90	mA
V_{IHT}	Input HIGH Voltage		2.0	V_{CC}	V
V_{ILT}	Input LOW Voltage		–0.5	0.8	V
I_{IHT}	Input HIGH Current	V_{IN} = V_{CC}	–10	+10	µA
I_{ILT}	Input LOW Current	V_{IN} = 0.0V		–500	µA
Receiver ECL-Compatible Input Pins: Loop, SI, INB					
V_{IHE}	Input HIGH Voltage		V_{CC}–1.165	V_{CC}	V
V_{ILE}	Input LOW Voltage		2.0	V_{CC}–1.475	V
I_{IHE}[2]	Input HIGH Current	V_{IN} = V_{IHE} Max.		+500	µA
I_{ILE}[2]	Input LOW Current	V_{IN} = V_{ILL} Min.	+0.5		µA
Differential Line Receiver Input Pins: INA+, INA–, INB+, INB–					
V_{DIFF}	Input Differential Voltage |(IN+) – (IN–)|		50	1200	mV
V_{IHH}	Highest Input HIGH Voltage			V_{CC}	V
V_{ILL}	Lowest Input LOW Voltage		2.0		V
I_{IHH}	Input HIGH Current	V_{IN} = V_{IHH} Max.		750	µA
I_{ILL}[3]	Input LOW Current	V_{IN} = V_{ILL} Min.	–200		µA

Notes:
1. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle.
2. Applies to Loop only.
3. Input currents are always positive at all voltages above V_{CC}/2.

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Electrical Characteristics (continued)

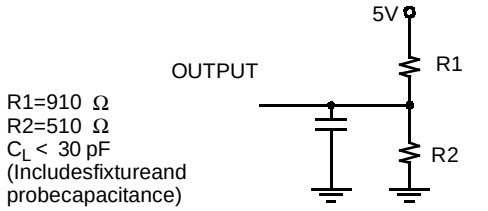
Parameter	Description	Test Conditions	Min.	Max.	Unit
Miscellaneous			**Typ.**	**Max.**	
I_{CCR}[4]	Receiver Power Supply Current	Freq. = Max	130	150	mA

Capacitance[5]

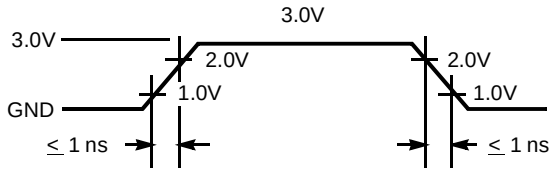
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f_0 = 1 MHz, V_{CC} = 5.0V	10	pF

Notes:
4. Maximum I_{CCR} is measured with V_{CC}=Max., RF=LOW, and outputs unloaded. Typical I_{CCR} is measured with V_{CC}=5.0V, T_A=25°C, RF=LOW, $\overline{BISTEN}$=LOW, and outputs unloaded.
5. Tested initially and after any design or process changes that may affect these parameters.

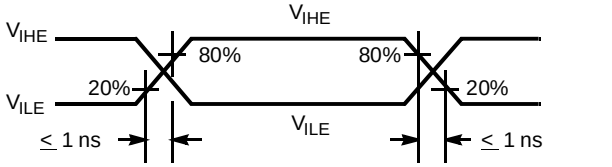
AC Test Loads and Waveforms



(a) TTL AC Test Load[6]



(c) TTL Input Test Waveform B9331–4



(d) ECL Input Test Waveform B9331–5

Receiver Switching Characteristics Over the Operating Range

Parameter	Description	7B9331		Unit
		Min.	Max.	
t_{CKR}	Read Clock Period (No Serial Data Input), REFCLK as Reference[7]	–1	+1	%
t_B	Bit Time[8]	3.03	6.25	ns
t_{CPRH}	Read Clock Pulse HIGH	$5t_B$–3		ns
t_{CPRL}	Read Clock Pulse LOW	$5t_B$–3		ns
t_A	Data Access Time[9, 10]	$2t_B$–3	$2t_B$+4	ns
t_{ROH}	Data Hold Time[9,10]	$2t_B$–3		ns
t_{CKX}	REFCLK Clock Period Referenced to CKW of Transmitter (CY7B923)[11]	–0.1	+0.1	%
t_{CPXH}	REFCLK Clock Pulse HIGH	6.5		ns
t_{CPXL}	REFCLK Clock Pulse LOW	6.5		ns
t_{DS}	Propagation Delay SI to Status (note ECL and TTL thresholds)[12]		20	ns

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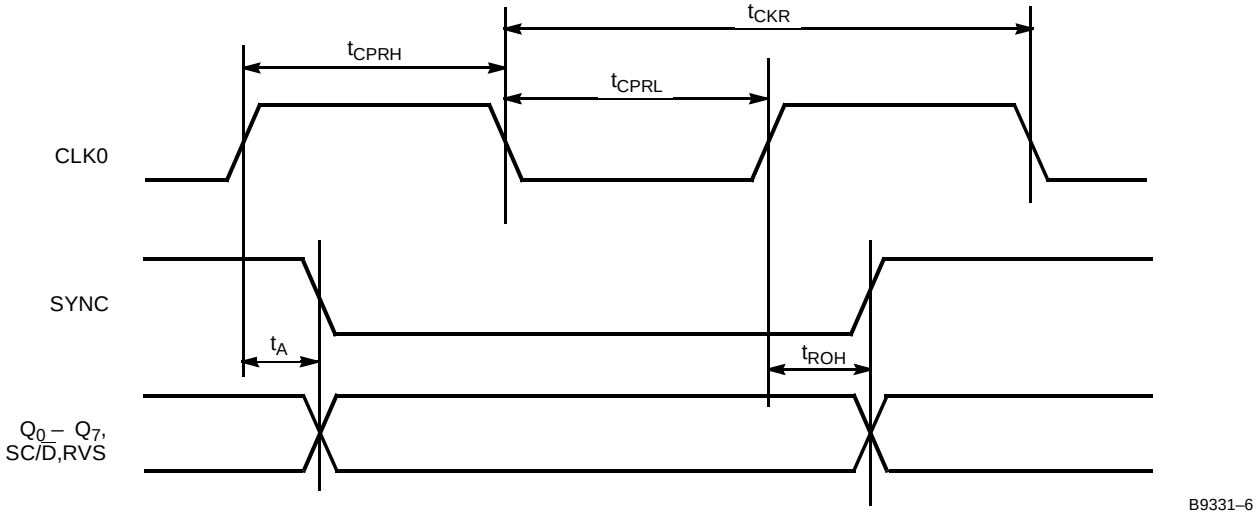
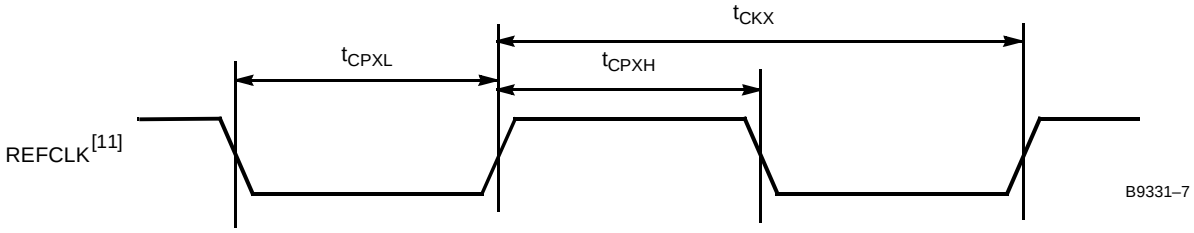
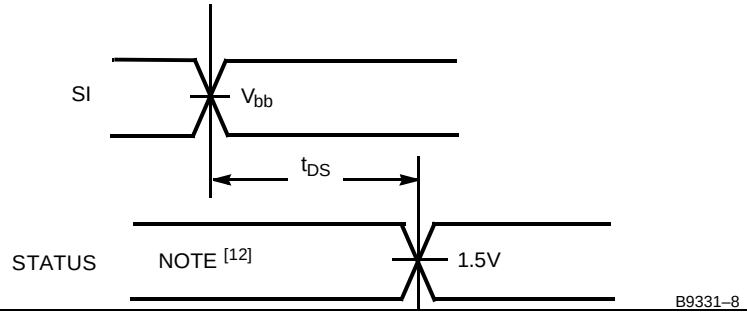
Switching Waveforms for the CY7B9331 HOTLink Receiver







Notes:

6. Tested initially and after any design or process changes that may affect these parameters, but not 100% tested.
7. The period of t_{CKR} will match the period of the transmitter (CY7B923) CKW when the receiver is receiving serial data. When data is interrupted, Clk0 may drift to one of the range limits above.
8. Receiver t_B is calculated as $t_{Clk0}/10$ if no data is being received, or $t_{CKW}/10$ if data is being received.
9. Data includes Q_{0-7}, SC/D, RVS, and Sync.
10. t_A and t_{ROH} specifications are only valid if all outputs (Clk0, Sync, Q_{0-7}, SC/$\overline{D}$, and RVS) are loaded with similar DC and AC loads.
11. REFCLK has no phase or frequency relationship with Clk0 and only acts as a centering reference to reduce clock synchronization time. REFCLK must be within 0.1% of the transmitter CKW frequency, necessitating a ±500-PPM crystal.
12. The ECL switching threshold is the midpoint between the ECL— V_{OH}, and V_{OL} specification (approximately V_{CC} — 1.35V). The TTL switching threshold is 1.5V.

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Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY7B9331–JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
CY7B9331–SC	S21	28-Lead (300-Mil) SOIC	

Document #: 38-00359

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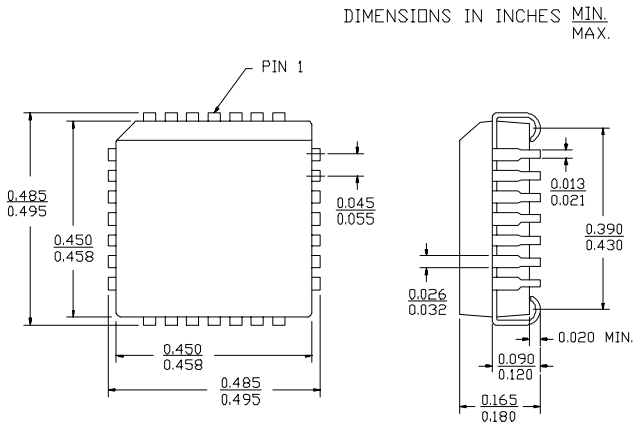
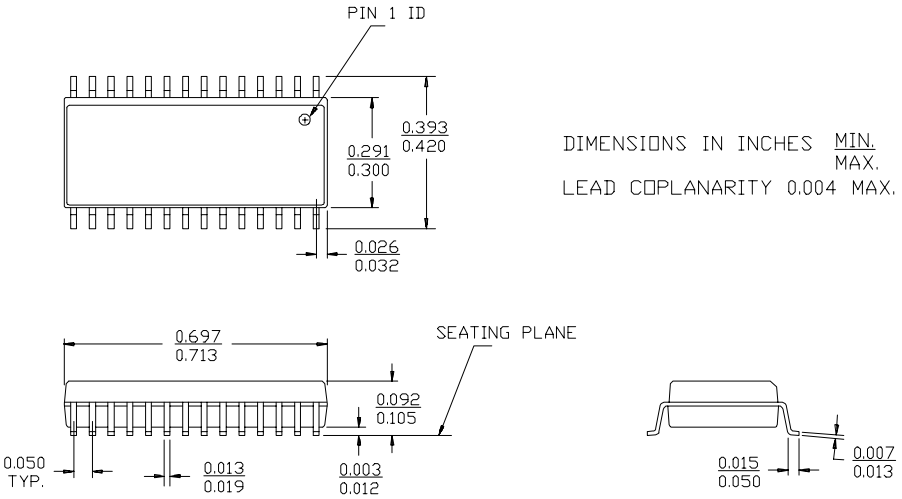
Package Diagrams

28-Lead Plastic Leaded Chip Carrier J64



28–Lead (300-Mil) Molded SOIC S21



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