RoboClock®, CY7B995

2.5/3.3V 200-MHz High-Speed Multi-Phase PLL Clock Buffer

Features

- 2.5V or 3.3V operation
- Split output bank power supplies
- Output frequency range: 6 MHz to 200 MHz
- 45 ps typical cycle-cycle jitter
- ± 2% max output duty cycle
- Selectable output drive strength
- Selectable positive or negative edge synchronization
- Eight LVTTL outputs driving 50 Ω terminated lines
- LVCMOS/LVTTL over-voltage tolerant reference input
- Selectable phase-locked loop (PLL) frequency range and lock indicator
- Phase adjustments in 625/1250 ps steps up to ± 7.5 ns
- (1-6, 8, 10, 12) x multiply and (1/2,1/4)x divide ratios
- Spread-Spectrum compatible
- Power down mode
- Selectable reference divider
- Industrial temperature range: –40°C to +85°C
- 44-pin TQFP package

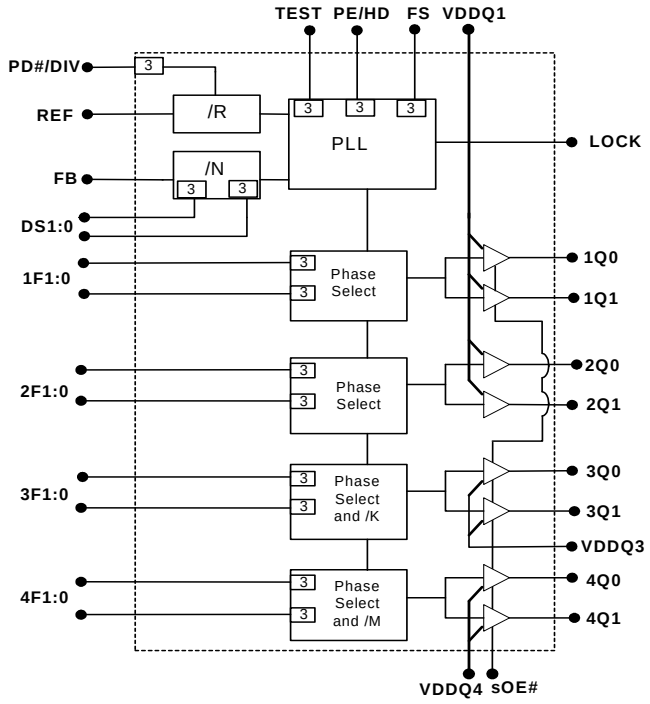
Description

The CY7B995 RoboClock® is a low voltage, low power, eight-output, 200 MHz clock driver. It features output phase programmability which is necessary to optimize the timing of high performance computer and communication systems.

The user can program both the frequency and the phase of the output banks through nF[0:1] and DS[0:1] pins. The adjustable phase feature allows the user to skew the outputs to lead or lag the reference clock. Any one of the outputs can be connected to feedback to achieve different reference frequency multiplication, and divide ratios and zero input-output delay.

The device also features split output bank power supplies, which enable the user to run two banks (1Qn and 2Qn) at a power supply level, different from that of the other two banks (3Qn and 4Qn). The three-level PE/HD pin also controls the synchronization of the output signals to either the rising, or the falling edge of the reference clock and selects the drive strength of the output buffers. The high drive option (PE/HD = MID) increases the output current from ± 12 mA to ± 24 mA.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - 44 Pin TQFP Package Top view

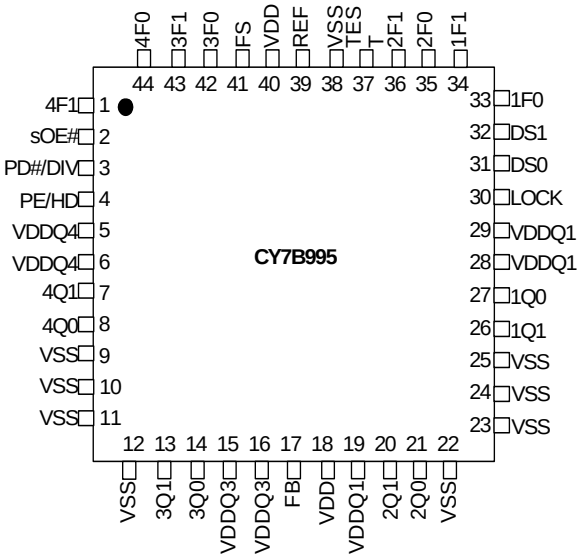


Table 1. Pin Definitions - 44 Pin TQFP Package

Pin	Name	IO[1]	Type	Description
39	REF	I	LVTTL/LVCMOS	**Reference Clock Input.**
17	FB	I	LVTTL	**Feedback Input.**
37	TEST	I	3-Level	**When MID or HIGH, disables PLL**[3]. REF goes to all outputs. Set LOW for normal operation.
2	sOE#	I, PD	LVTTL	**Synchronous Output Enable**. When HIGH, it stops clock outputs (except 2Q0 and 2Q1) in a LOW state (for PE/HD = H or M) – 2Q0, and 2Q1 may be used as the feedback signal to maintain phase lock. When TEST is held at MID level and sOE# is HIGH, the nF[1:0] pins act as output disable controls for individual banks when nF[1:0] = LL. Set sOE# LOW for normal operation.
4	PE/HD	I, PU	3-Level	**Selects Positive or Negative Edge Control, and High or Low output Drive Strength**. When LOW/HIGH, the outputs are synchronized with the negative/positive edge of the reference clock respectively. When at MID level, the output drive strength is increased and the outputs synchronize with the positive edge of the reference clock. See Table 10 on page 5.
34, 33, 36, 35, 43, 42, 1, 44	nF[1:0]	I	3-Level	**Selects Frequency and Phase of the Outputs**. See Table 4, Table 5, Table 6, Table 8, and Table 9 on page 4.
41	FS	I	3-Level	**Selects VCO Operating Frequency Range**. See Table 7 on page 4.
26,27,20,21, 13,14,7,8	nQ[1:0]	O	LVTTL	**Four banks of two outputs**. See Table 6 on page 4 for frequency settings.
32, 31	DS[1:0]	I	3-Level	**Selects Feedback Divider**. See Table 3 on page 4.
3	PD#/DIV	I, PU	3-Level	**Power down and Reference Divider Control**. When LOW, shuts off entire chip. When at MID level, enables the reference divider. See Table 2 for settings.
30	LOCK	O	LVTTL	**PLL Lock Indication Signal**. HIGH indicates lock, LOW indicates the PLL is not locked, and outputs may not be synchronized to the input.
5,6	$V_{DD}Q4$[2]	PWR	Power	**Power supply for Bank 4 Output Buffers**. See Table 11 on page 5 for supply level constraints.
15,16	$V_{DD}Q3$ [2]	PWR	Power	**Power supply for Bank 3 Output Buffers**. See Table 11 on page 5 for supply level constraints.
19,28,29	$V_{DD}Q1$[2]	PWR	Power	**Power supply for Bank 1 and Bank 2 Output Buffers**. See Table 11 on page 5 for supply level constraints.
18,40	V_{DD}[2]	PWR	Power	**Power supply for the Internal Circuitry**. See Table 11 on page 5 for supply level constraints.
9-12, 22-25, 38	V_{SS}	PWR	Power	**Ground**

Device Configuration

The outputs of the CY7B995 can be configured to run at frequencies ranging from 6 MHz to 200 MHz. The feedback input divider is controlled by the 3-level DS[0:1] pins as indicated in Table 3 on page 4, and the reference input divider is controlled by the 3-level PD#/DIV pin as indicated in Table 2.

Table 2. Reference Divider Settings

PD#/DIV	R–Reference Divider
H	1
M	2
L[4]	N/A

Notes
1. PD indicates an internal pull down and 'PU' indicates an internal pull up.
2. A bypass capacitor (0.1µF) must be placed as close as possible to each positive power pin (< 0.2"). If these bypass capacitors are not close to the pins, their high frequency filtering characteristic is cancelled by the lead inductance of the traces.
3. When TEST = MID and sOE# = HIGH, PLL remains active with nF[1:0] = LL functioning as an output disable control for individual output banks. Skew selections remain in effect unless nF[1:0] = LL.
4. When PD#/DIV = LOW, the device enters power down mode.

Table 3. Feedback Divider Settings

DS[1:0]	N-Feedback Input Divider	Permitted Output Divider Connected to FB
LL	2	1 or 2
LM	3	1
LH	4	1,2 or 4
ML	5	1 or 2
MM	1	1,2 or 4
MH	6	1 or 2
HL	8	1 or 2
HM	10	1
HH	12	1

In addition to the reference and feedback dividers, the CY7B995 includes output dividers on Bank3 and Bank4, which are controlled by 3F[1:0] and 4F[1:0] as indicated in Table 4 and Table 5, respectively.

Table 4. Output Divider Settings – Bank 3

3F[1:0]	K - Bank3 Output Divider
LL	2
HH	4
Other[5]	1

Table 5. Output Divider Settings – Bank 4

4F[1:0]	M- Bank4 Output Divider
LL	2
Other[5]	1

The divider settings and the FB input to any output connection needed to produce various output frequencies are summarized in Table 6.

Table 6. Output Frequency Settings.

Configuration	Output Frequency		
FB Input Connected to	1Q[0:1] and 2Q[0:1][6]	3Q[0:1]	4Q[0:1]
1Qn or 2Qn	(N / R) x F_{REF}	(N / R) x (1 / K) x F_{REF}	(N / R) x (1 / M) x F_{REF}
3Qn	(N / R) x K x F_{REF}	(N / R) x F_{REF}	(N / R) x (K / M) x F_{REF}
4Qn	(N / R) x M x F_{REF}	(N / R) x (M / K) x F_{REF}	(N / R) x F_{REF}

The 3-level FS control pin setting determines the nominal operating frequency range of the divide-by-one outputs of the device. The CY7B995 PLL operating frequency range that corresponds to each FS level is given in Table 7.

Table 7. Frequency Range Select

FS	PLL Frequency Range
L	24 to 50 MHz
M	48 to 100 MHz
H	96 to 200 MHz

Selectable output skew is in discrete increments of time units (t_U).The value of t_U is determined by the FS setting and the maximum nominal frequency. The equation used to determine the t_U value is: $t_U = 1 / (f_{NOM} \times MF)$

where MF is a multiplication factor which is determined by the FS setting as indicated in Table 8.

Table 8. MF Calculation

FS	MF	f_{NOM} at which t_U is 1.0 ns (MHz)
L	32	31.25
M	16	62.5
H	8	125

Table 9. Output Skew Settings

nF[1:0]	Skew (1Q[0:1],2Q[0:1])	Skew (3Q[0:1])	Skew (4Q[0:1])
LL[7]	$-4t_U$	Divide By 2	Divide By 2
LM	$-3t_U$	$-6t_U$	$-6t_U$
LH	$-2t_U$	$-4t_U$	$-4t_U$
ML	$-1t_U$	$-2t_U$	$-2t_U$
MM	Zero Skew	Zero Skew	Zero Skew
MH	$+1t_U$	$+2t_U$	$+2t_U$
HL	$+2t_U$	$+4t_U$	$+4t_U$
HM	$+3t_U$	$+6t_U$	$+6t_U$
HH	$+4t_U$	Divide By 4	Inverted[8]

Notes
5. These states are used to program the phase of the respective banks. See Table 8 and Table 9.
6. These outputs are undivided copies of the VCO clock. The formulas in this column can be used to calculate the VCO operating frequency (FNOM) at a given reference frequency (FREF), and divider and feedback configuration. The user must select a configuration and a reference frequency that generates a VCO frequency, and is within the range specified by FS pin. See Table 7.

In addition to determining whether the outputs synchronize to the rising or the falling edge of the reference signal, the 3-level PE/HD pin controls the output buffer drive strength as indicated in Table 10 on page 5. Refer to the AC Timing Definitions section for a description of input-to-output and output-to-output phase relationships.

Table 10. PE/HD Settings

PE/HD	Synchronization	Output Drive Strength[9]
L	Negative	Low Drive
M	Positive	High Drive
H	Positive	Low Drive

The CY7B995 features split power supply buses for Banks 1 and 2, Bank 3 and Bank 4, which enables the user to obtain both 3.3V and 2.5V output signals from one device. The core power supply (V_{DD}) must be set at a level that is equal to or higher than any of the output power supplies.

Table 11. Power Supply Constraints

V_{DD}	$V_{DD}Q1$[10]	$V_{DD}Q3$[10]	$V_{DD}Q4$[10]
3.3V	3.3V or 2.5V	3.3V or 2.5V	3.3V or 2.5V
2.5V	2.5V	2.5V	2.5V

Governing Agencies

The following agencies provide specifications that apply to the CY7B995. The agency name and relevant specification is listed below.

Table 12. Governing Agencies and Specifications

Agency Name	Specification
JEDEC	JESD 51 (Theta JA)
	JESD 65 (Skew, Jitter)
IEEE	1596.3 (Jiter Specs)
UL-194_V0	94 (Moisture Grading)
MIL	883E Method 1012.1 (Therma Theta JC)

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Operating Voltage	Functional @ 2.5V ± 5%	2.25	2.75	V
V_{DD}	Operating Voltage	Functional @ 3.3V ± 10%	2.97	3.63	V
$V_{IN(MIN)}$	Input Voltage	Relative to V_{SS}	V_{SS} – 0.3	–	V
$V_{IN(MAX)}$	Input Voltage	Relative to V_{DD}	–	V_{DD} + 0.3	V
$V_{REF(MAX)}$	Reference Input Voltage	V_{DD} = 3.3V		5.5	V
$V_{REF(MAX)}$	Reference Input Voltage	V_{DD} = 2.5V		4.6	V
T_S	Temperature, Storage	Non Functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Functional	–40	+85	°C
T_J	Temperature, Junction	Functional	–	155	°C
$Ø_{JC}$	Dissipation, Junction to Case	Mil-Spec 883E Method 1012.1	–	42	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	74	°C/W
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
UL-94	Flammability Rating	@1/8 in.	V–0		
MSL	Moisture Sensitivity Level		1		
F_{IT}	Failure in Time	Manufacturing Testing	10		ppm

Notes
7. LL disables outputs if TEST = MID and sOE# = HIGH.
8. When 4Q[0:1] are set to run inverted (HH mode), sOE# disables these outputs HIGH when PE/HD = HIGH or MID, sOE# disables them LOW when PE/HD = LOW.
9. Please refer to “DC Parameters” section for I_{OH}/I_{OL} specifications.
10. $V_{DD}Q1/3/4$ must not be set at a level higher than that of V_{DD}. They can be set at different levels from each other, e.g., V_{DD} = 3.3V, $V_{DD}Q1$ = 3.3V, $V_{DD}Q3$ = 2.5V and $V_{DD}Q4$ = 2.5V.

DC Specifications at 2.5V

Parameter	Description	Condition		Min	Max	Unit
V_{DD}	2.5 Operating Voltage	2.5V ± 5%		2.375	2.625	V
V_{IL}	Input LOW Voltage	REF, FB, and sOE# Inputs		–	0.7	V
V_{IH}	Input HIGH Voltage			1.7	–	V
V_{IHH}[11]	Input HIGH Voltage	3-Level Inputs, (TEST, FS, nF[1:0], DS[1:0], PD#/DIV, PE/HD). (These pins are normally wired to V_{DD}, GND, or unconnected)		V_{DD} – –0.4	–	V
V_{IMM}[11]	Input MID Voltage			$V_{DD}/2$ – 0.2	$V_{DD}/2$ + 0.2	V
V_{ILL}[11]	Input LOW Voltage			–	0.4	V
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}/G_{ND}, V_{DD}$ = Max; (REF and FB Inputs)		–5	5	µA
I_3	3-Level Input DC Current	HIGH, $V_{IN} = V_{DD}$	3-Level Inputs (TEST, FS, nF[1:0], DS[1:0], PD#/DIV, PE/HD)	–	200	µA
		MID, $V_{IN} = V_{DD}/2$		–50	50	µA
		LOW, $V_{IN} = V_{SS}$		–200	–	µA
I_{PU}	Input Pull-Up Current	$V_{IN} = V_{SS}$, V_{DD} = Max		–25	–	µA
I_{PD}	Input Pull-Down Current	$V_{IN} = V_{DD}$, V_{DD} = Max, (sOE#)		–	100	µA
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA (PE/HD = L/H), (nQ[0:1])		–	0.4	V
		I_{OL} = 20 mA (PE/HD = MID),(nQ[0:1])		–	0.4	V
		I_{OL} = 2 mA (LOCK)			0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = –12 mA (PE/HD = L/H),(nQ[0:1])		2.0	–	V
		I_{OH} = –20 mA (PE/HD = MID),(nQ[0:1])		2.0	–	V
		I_{OH} = –2 mA (LOCK)		2.0		V
I_{DDQ}	Quiescent Supply Current	V_{DD} = Max, TEST = MID, REF = LOW, sOE# = LOW, Outputs Not Loaded		–	2	mA
I_{DDPD}	Power down Current	PD#/DIV, sOE# = LOW Test,nF[1:0],DS[1:0] = HIGH; V_{DD} = Max		10(typ.)	25	µA
I_{DD}	Dynamic Supply Current	At 100 MHz		150		mA
C_{IN}	Input Pin Capacitance			4		pF

DC Specifications at 3.3V

Parameter	Description	Condition		Min	Max	Unit
V_{DD}	3.3 Operating Voltage	3.3V ± 10%		2.97	3.63	V
V_{IL}	Input LOW Voltage	REF, FB and sOE# Inputs		–	0.8	V
V_{IH}	Input HIGH Voltage			2.0	–	V
V_{IHH}[11]	Input HIGH Voltage	3-Level Inputs (TEST, FS, nF[1:0], DS[1:0],PD#/DIV, PE/HD); (These pins are normally wired to VDD,GND or unconected		V_{DD}– –0.6	–	V
V_{IMM}[11]	Input MID Voltage			$V_{DD}/2$ – 0.3	$V_{DD}/2$+ 0.3	V
V_{ILL}[11]	Input LOW Voltage			–	0.6	V
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}/G_{ND}, V_{DD}$ = Max (REF and FB inputs)		–5	5	µA
I_3	3-Level Input DC Current	HIGH, $V_{IN} = V_{DD}$	3-Level Inputs, (TEST, FS, nF[1:0], DS[1:0], PD#/DIV, PE/HD)	–	200	µA
		MID, $V_{IN} = V_{DD}/2$		–50	50	µA
		LOW, $V_{IN} = V_{SS}$		–200	–	µA
I_{PU}	Input Pull Up Current	$V_{IN} = V_{SS}$, V_{DD} = Max		–25	–	µA
I_{PD}	Input Pull Down Current	$V_{IN} = V_{DD}$, V_{DD} = Max, (sOE#)		–	100	µA
V_{OL}	Output LOW Voltage	I_{OL} = 12 mA (PE/HD = L/H), (nQ[0:1])		–	0.4	V
		I_{OL} = 24 mA (PE/HD = MID),(nQ[0:1])		–	0.4	V
		I_{OL} = 2 mA (LOCK)			0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = –12 mA (PE/HD = L/H),(nQ[0:1])		2.4	–	V
		I_{OH} = –24 mA (PE/HD = MID),(nQ[0:1])		2.4	–	V
		I_{OH} = –2 mA (LOCK)		2.4		V
I_{DDQ}	Quiescent Supply Current	VDD = Max, TEST = MID, REF = LOW, sOE# = LOW, Outputs Not Loaded		–	2	mA
I_{DDPD}	Power Down Current	PD#/DIV, sOE# = LOW, Test,nF[1:0],DS[1:0] = HIGH, V_{DD} = Max		10(typ.)	25	µA
I_{DD}	Dynamic Supply Current	At 100 MHz		230		mA
C_{IN}	Input Pin Capacitance			4		pF

AC Input Specifications

Parameter	Description	Condition	Min	Max	Unit
T_R,T_F	Input Rise/Fall Time	0.8V – 2.0V	–	10	ns/V
T_{PWC}	Input Clock Pulse	HIGH or LOW	2	–	ns
T_{DCIN}	Input Duty Cycle		10	90	%
F_{REF}	Reference Input Frequency[12]	FS = LOW	2	50	MHz
		FS = MID	4	100	
		FS = HIGH	8	200	

Switching Characteristics

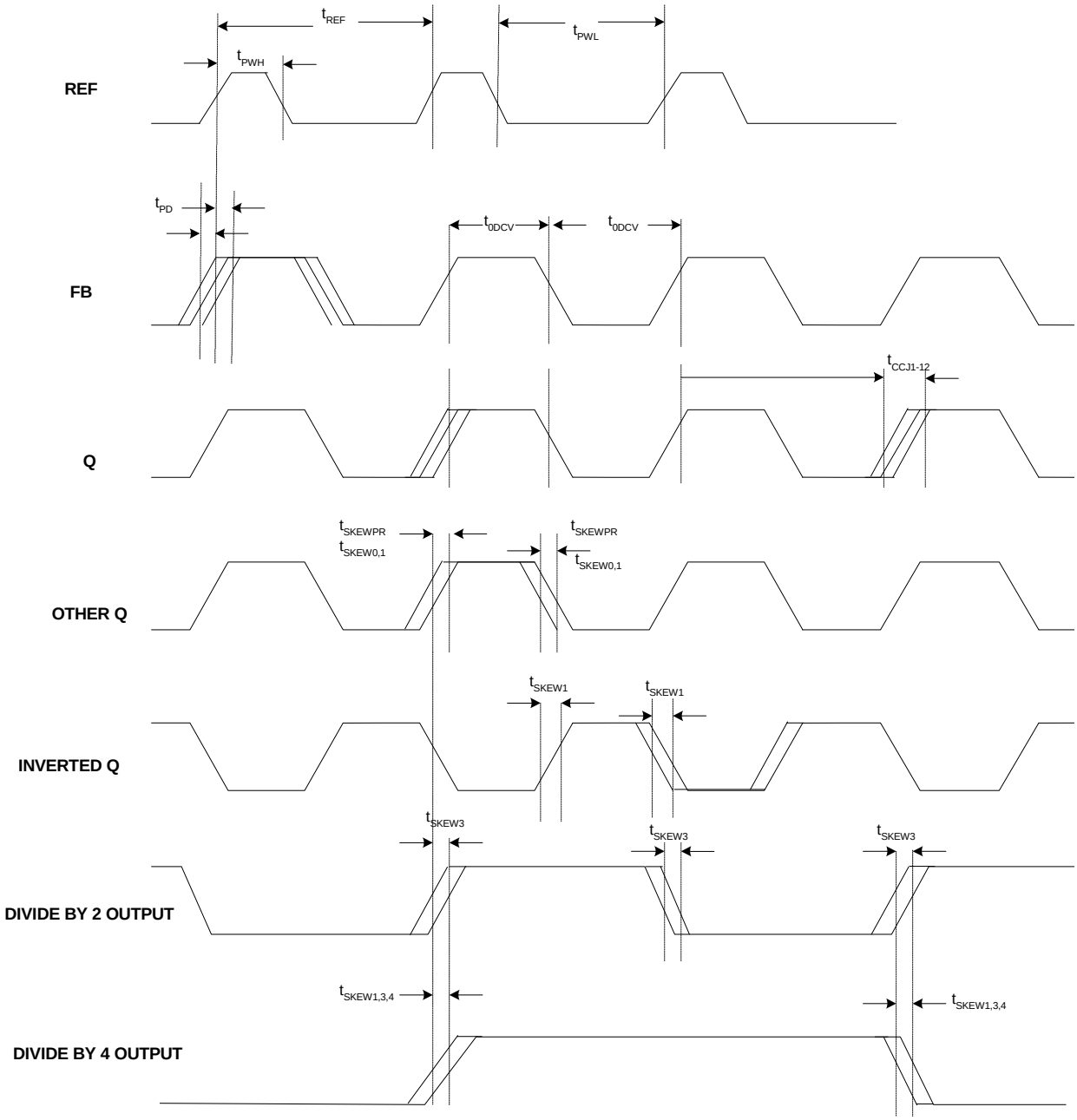
Parameter	Description	Condition	Min	Type	Max	Unit
F_{OR}	Output frequency range		6	–	200	MHz
VCO_{LR}	VCO Lock Range		200	–	400	MHz
VCO_{LBW}	VCO Loop Bandwidth		0.25	–	3.5	MHz
t_{SKEWPR}	Matched-Pair Skew[13]	Skew between the earliest and the latest output transitions within the same bank.	–	–	100	ps
t_{SKEW0}	Output-Output Skew[13]	Skew between the earliest and the latest output transitions among all outputs at $0t_U$.	–	–	200	ps
t_{SKEW1}		Skew between the earliest and the latest output transitions among all outputs for which the same phase delay has been selected.	–	–	200	ps
t_{SKEW2}		Skew between the nominal output rising edge to the inverted output falling edge.	–	–	500	ps
t_{SKEW3}		Skew between non-inverted outputs running at different frequencies.	–	–	500	ps
t_{SKEW4}	Output-Output Skew[13]	Skew between nominal to inverted outputs running at different frequencies.	–	–	500	ps
t_{SKEW5}		Skew between nominal outputs at different power supply levels.	–	–	650	ps
t_{PART}	Part-Part Skew	Skew between the outputs of any two devices under identical settings and conditions (V_{DDQ}, V_{DD}, temp, air flow, frequency, etc.).	–	–	750	ps
t_{PD0}	Ref to FB Propagation Delay[14]		–250	–	+250	ps
t_{ODCV}	Output Duty Cycle	Fout < 100 MHz, Measured at $V_{DD}/2$.	48	–	52	%
		Fout > 100 MHz, Measured at $V_{DD}/2$.	45	–	55	
t_{PWH}	Output High Time Deviation from 50%	Measured at 2.0V for V_{DD} = 3.3V and at 1.7V for V_{DD} = 2.5V.	–	–	1.5	ns
t_{PWL}	Output Low Time Deviation from 50%	Measured at 0.8V for V_{DD} = 3.3V and at 0.7V for V_{DD} = 2.5V.	–	–	2.0	ns
t_R/t_F	Output Rise/Fall Time	Measured at 0.8V–2.0V for V_{DD} = 3.3V and 0.7V–1.7V for V_{DD} = 2.5V.	0.15	–	1.5	ns
t_{LOCK}	PLL Lock Time[15,16]		–	–	0.5	ms
t_{CCJ}	Cycle-Cycle Jitter	Divide by one output frequency, FS = L, FB = divide by any.	–	45	100	ps
		Divide by one output frequency, FS = M/H, FB = divide by any.	–	55	150	ps

Notes

11. These Inputs are normally wired to VDD, GND or unconnected. Internal termination resistors bias unconnected inputs to $V_{DD}/2$.
12. IF PD#/DIV is in HIGH level (R-reference divider = 1). Reference Input Frequency = $F_{REF.}$ IF PD#/DIV is in MID level (R-reference divider = 2). Reference Input Frequency = F_{REF}x2.
13. Test Load = 20 pF, terminated to $V_{CC}/2$. All outputs are equally loaded.
14. t_{PD} is measured at 1.5V for V_{DD} = 3.3V and at 1.25V for V_{DD} = 2.5V with REF rise/fall times of 0.5 ns between 0.8V–2.0V.
15. t_{LOCK} is the time that is required before outputs synchronize to REF. This specification is valid with stable power supplies which are within normal operating limits.
16. Lock detector circuit may be unreliable for input frequencies lower than 4 MHz, or for input signals which contain significant jitter.

AC Timing Definitions

Figure 2. Timing Definition



With PE HIGH (LOW), the REF rising (falling) edges are aligned to the FB rising (falling) edges. Also, when PE is HIGH (LOW), all divided outputs' rising (falling) edges are aligned to the rising (falling) edges of the undivided, non-inverted outputs. Regardless of PE setting, divide-by-4 outputs', rising edges align to the divide-by-2 outputs' rising edges.

In cases where a non-divided output is connected to the FB input pin, the divided output rising edges can be either 0 or 180 degrees phase aligned to the REF input rising edges (as set randomly at power-up). If the divided outputs are required as rising-edge (falling-edge) aligned to the REF input's rising (falling) edge, set the PE pin HIGH (LOW) and connect the lowest frequency divided output to the FB input pin. This setup provides a consistent input-output and output-output phase relationship.

AC Test Loads and Waveforms

Figure 3. For Lock Output and all other Outputs

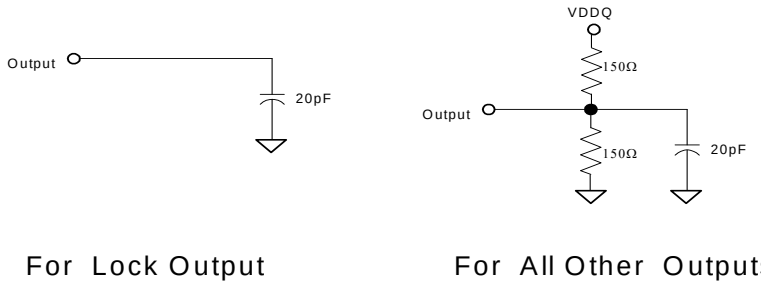


Figure 4. 3.3V LVTTL and 2.5V LVTTL Output Waveforms

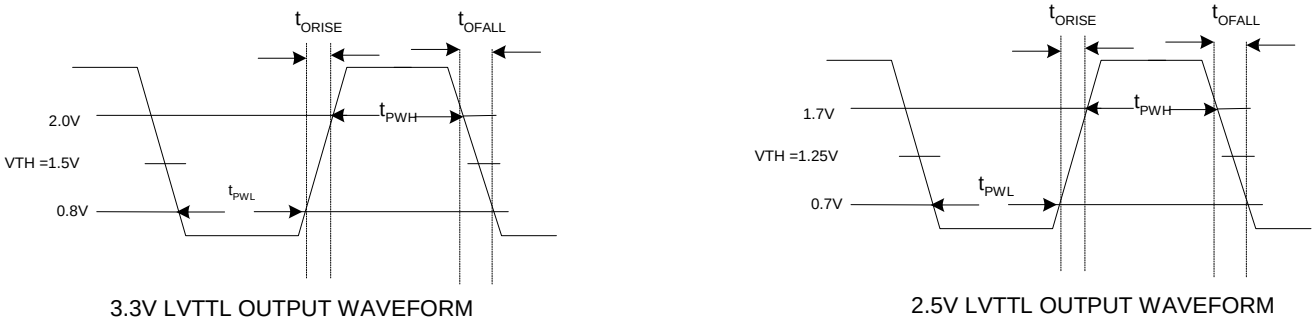
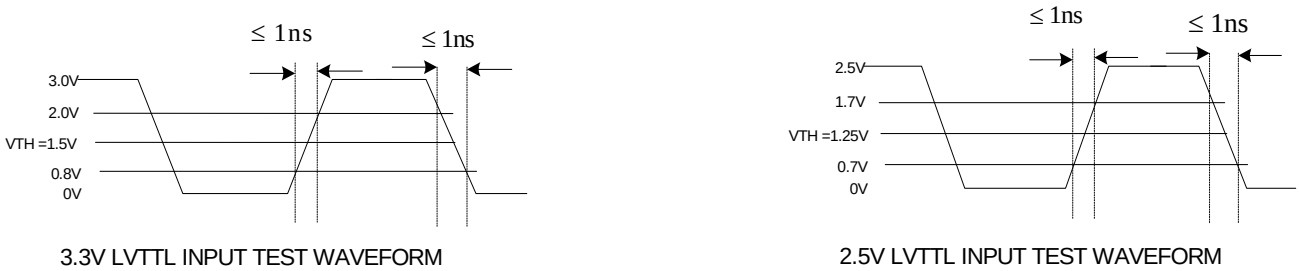


Figure 5. 3.3V LVTTL and 2.5V LVTTL Input Test Waveforms

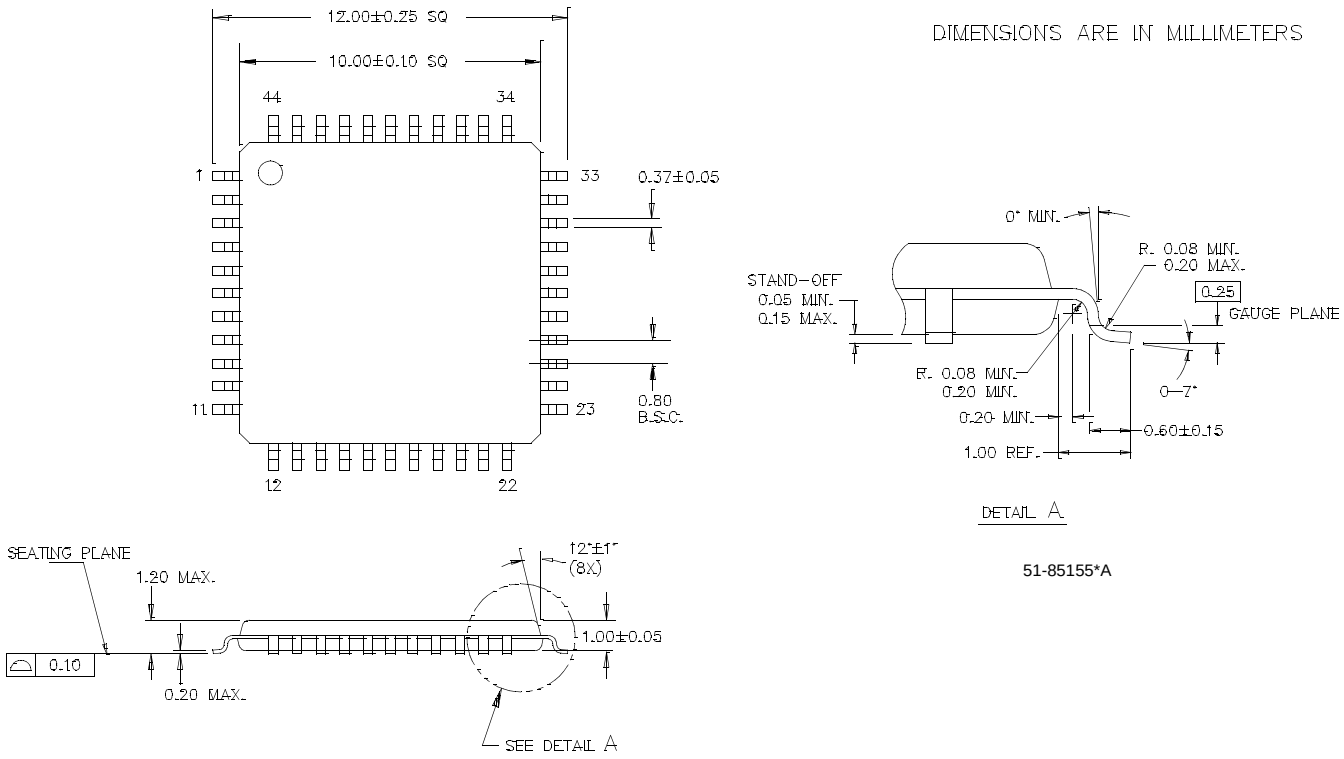


Ordering Information

Part Number	Package Type	Product Flow	Status
CY7B995AC	44 TQFP	Commercial, 0° to 70°C	Obsolete
CY7B995ACT	44 TQFP – Tape and Reel	Commercial, 0° to 70°C	Obsolete
CY7B995AI	44 TQFP	Industrial, –40° to 85°C	Not for new design
CY7B995AIT	44 TQFP – Tape and Reel	Industrial, –40° to 85°C	Obsolete
Pb-free			
CY7B995AXC	44 TQFP	Commercial, 0° to 70°C	Active
CY7B995AXCT	44 TQFP – Tape and Reel	Commercial, 0° to 70°C	Active
CY7B995AXI	44 TQFP	Industrial, –40° to 85°C	Active
CY7B995AXIT	44 TQFP – Tape and Reel	Industrial, –40° to 85°C	Active

Package Drawing and Dimension

Figure 6. 44-Pb Thin Plastic Quad Flat Pack (10 x 10 x 1.0 mm) A44SB



Document History Page

Document Title: CY7B995 Roboclock® 2.5/3.3V 200-MHz High-speed Multi-phase PLL Clock Buffer Document Number: 38-07337				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	122626	01/10/03	RGL	New Data Sheet
*A	205743	See ECN	RGL	Changed Pin 5 from VDD to VDDQ4, Pin 16 from VDD to VDDQ3 and Pin 29 from VDD to VDDQ1 Added pin 1 indicator in the Pin Configuration Drawing
*B	362760	See ECN	RGL	Added description on the AC Timing Waveforms Added typical value for cycle-to-cycle jitter
*C	389237	See ECN	RGL	Added Lead-free devices
*D	1562063	See ECN	PYG/AESA	Added Status column to Ordering Information table