

Advanced PayloadPlus® APP540 and APP520 Packet-Optimized Network Processors

Introduction

The Agere Systems Advanced PayloadPlus® APP540 and APP520 Network Processor devices are the latest addition to the PayloadPlus family of products. They offer a comprehensive programmable solution with 5Gbps of classification, network processing, and traffic management throughput in a single highly integrated chip. The APP540/520 integrate the functions of a network processor, traffic manager, search engine, and Ethernet MAC device to enable network system architects to build very high density, high performance multiprotocol packet processing systems. The devices are designed for high performance packet processing applications including Ethernet over SONET/SDH switches, packet edge routers, Cable Modem Termination Systems, IP DSLAMs, and layer 2/3/4 switches.

The PayloadPlus product family represents a technological revolution for intelligent communication equipment with Layer 2 and above processing capabilities. Agere Systems products focus on the wire-speed datapath functions and work in conjunction with physical interface devices, a low-speed microprocessor, and backplane fabric offerings for networking and communication applications.

Description

The APP540 and APP520 are complete, programmable, single-chip network processors with integrated classification and traffic management capabilities. Both devices are software-compatible with the other members of the PayloadPlus family of network processors from Agere Systems.

The APP520 has 2GbE MACs integrated and supports programmable policing and statistics using

on-chip memory. The APP540 has 4GbE MACs integrated and supports the use of external memory to store policing and statistics state information. Both devices also integrate 16 10/100 Ethernet MACs and support up to 5 Gb/s total processing throughput.

The APP540/520 accepts a data stream composed of either frames or cells/blocks from an industry-standard interface, analyzes and classifies the frames or cells/blocks, reassembles them into PDUs, classifies the resulting PDUs, updates policing, statistics, and other state information, and then performs buffer management, traffic scheduling/shaping, and data modification before it transmits the PDUs.

The APP540/520 supports the following interfaces:

- Media — supports the following standards:
 - POS-PHY Level 3
 - GMII (4/2 integrated GbE MACs)
 - SMII (16 integrated 10/100 MACs)
- Fabric — a second POS-PHY Level 3 interface that can be directed to a switch fabric or coprocessor for additional function support.
- PCI interface — a 32-bit/66 MHz Peripheral Component Interconnect (PCI) bus enables custom logic that is used to configure the APP540/520 and other system devices.

The APP540/520 supports robust multiprotocol packet processing capabilities, including support for:

- Rigorous bandwidth, delay, and jitter guarantees to support high-value service level agreements and enable frame relay-like service over Ethernet
- Hierarchical scheduling and shaping to provide QoS guarantees to groups of related traffic

- Dynamic bandwidth and QoS/CoS modification to enable real-time dynamic service provisioning
- Ethernet bridging/switching, including 802.1Q virtual LANs (VLANs), stacked VLANs, wire-path address learning for transparent bridging, and 802.1p priorities
- MPLS and Virtual Private LAN Service (VPLS), including support for label stack depths of 3 or more
- DRAM-based classification database which can contain 1 million or more routing table or other entries
- Programmable policing, statistics, billing, and RMON functionality
- Multifield classification and access control list capabilities
- Tunneling and protocol interworking, including support for PPPoE, L2TP, and other complex tunneling methods
- High performance multicast processing with the ability to individually schedule and individually modify each copy of a multicast packet
- Wire-speed IP fragmentation

The table below describes the high level features of the two devices.

| | APP540 | APP520 |
|----------------------------------|------------------------|------------------------|
| Line Speed (one direction) | 5Gbits/sec | 5Gbits/sec |
| Number of Queues | 8K | 8K |
| Number of Policing Connections | 2880 | 2880 |
| Number of Statistics Connections | 23040 32b | 23040 32b |
| Package | 1413 FCBGA | 1413 FCBGA |
| Integrated Ethernet MACs | (16) 10/100 (4) GbE | (16) 10/100 (2) GbE |

Figure 1 System Overview

The APP540 and APP520 are also pin compatible with the full-featured APP550 multiservice network processor.

Programmability

At the heart of the PayloadPlus product family are the Functional Programming Language (FPL) and patented Pattern

Processing Engine (PPE) technologies. Using powerful, high-level FPL code, the PPE implements complex pattern or signature recognition, and operates on the packets or cells containing those signatures. The APP540/520 can analyze and take action on patterns anywhere in the payload and headers of the data stream.

In addition, the APP540/520 contains programmable compute engines that work in concert with the classification engine to manage tasks such as buffer management, traffic shaping, data modifications, and policing.

And because the APP540/520 is a programmable processor rather than a fixed-function ASIC, it can handle new protocols or applications as they are developed or as new network functions are required.

Furthermore, as part of the PayloadPlus family, the APP540/520 offers the industry's most efficient application development model. Through a combination of high-level programming languages, application level APIs, a reference code library, and a robust development tool suite, the APP540/520 allows you to create feature-rich applications in a dramatically shortened development interval. The cycle-accurate simulator and software traffic generator allow you to build, run, and debug applications before you have hardware in your lab, thereby moving software and hardware development onto parallel paths.

Features and Benefits

High Level of Solution Integration

Integrated classifier, traffic manager, network processor, Ethernet MACs, and memory along with inexpensive external memory technology, enable you to design the industry's most cost-, power-, and space- efficient linecards.

True Line-Rate Performance

Configurations support full OC-48c performance with any packet size of 40 bytes or more, even when performing complex multifield classification and rigorous traffic management processing. This high level of performance provides headroom for future function expansion.

Ease of Programmability

Harnessing the processing power of the APP540/520 is straightforward due to the use of a simple single-threaded programming model and high-level languages: FPL and Network Processor C (formerly known as ASL). Even more importantly, no time is spent hand-optimizing in assembly or microcode to reach full performance.

Fast, Deterministic Classification

The APP540/520's patented search algorithm lets you create large tables and search them quickly using off-the-shelf DRAM. You can search for data patterns of any size, and search time is independent of the number of entries in the search table.

Sophisticated Scheduling and Shaping Capabilities

The APP540/520 supports robust hierarchical scheduling and shaping. You can assign per-queue minimum and maximum data rates for elegant handling of traffic destined for overprovisioned ports.

Integrated Ethernet MACs

Using the 4x1000 on the APP540, or the 2x1000 on the APP520, as well as 16x10/100 integrated Ethernet MACs, you can develop high port density, and space efficient Ethernet applications that support technology such as Ethernet over SONET/SDH, VLANs, and bridging.

User-Defined Header Creation and Data Tagging Capabilities

User-defined header creation and data tagging capabilities facilitate protocol interworking and the creation of multiprotocol tunneled applications to support Virtual Private Networks (VPNs).

Programmable Per-Flow Counters and Policing

Programmable per-flow counters and policing enable highly differential admission control and billing applications for carrier revenue generation.

Fully Scalable Software

Wire-path programs written in FPL and ASL transfer directly to the Agere Systems 10G Network Processor components (APP750). The high-level nature of the Agere Systems programming model, along with the scalable PayloadPlus hardware architecture, allows the entire PayloadPlus family to have a consistent wire-path and API software model. This transferability saves you months of software development in next-generation product development.

Support for Packet or Cell-Based Switch Fabrics

The flexible segmentation capabilities of the APP540/520 allow connection to fabrics with different payload size requirements.

Flexible Standard Interface Support

The use of multiple industry-standard interfaces provides the flexibility to build a wide range of applications.

Application Development

The Agere Systems APP540/520 handles complex multi-protocol information at wire speeds up to 2.5 Gbps or OC-48c. Supported protocols include IPv4 and IPv6, ATM, Ethernet, and Multiprotocol Label Switching (MPLS). Applications include:

- Protocol tunnel origination and termination for IP Security (IPSEC) and Level 2 Tunneling Protocol (L2TP)
- MPLS
- Ethernet bridging, VLANs, and VPLS
- Routing and switching
- Access Control List (ACL) processing
- Monitoring
- Ethernet over SONET/SDH

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January 2003

PB-03-048NP

