



ULTRA-PRECISION 1:8 FANOUT BUFFER WITH LVPECL OUTPUTS AND INTERNAL TERMINATION

Precision Edge®
SY58032U



Precision Edge®

FEATURES

- Precision 1:8, LVPECL fanout buffer
- Guaranteed AC performance over temperature and voltage:
 - Clock frequency range: DC to 4GHz
 - <110ps t_r / t_f times
 - <330ps t_{pd}
 - <20ps skew
- Low-jitter performance:
 - <10ps_{pp} total jitter (clock)
 - <1ps_{RMS} random jitter
- 100k LVPECL compatible outputs
- Fully differential inputs/outputs
- Accepts an input signal as low as 100mV
- Unique input termination and V_T pin accepts DC-coupled and AC-coupled differential inputs: (LVPECL, LVDS, and CML)
- Power supply 2.5V ±5% or 3.3V ±10%
- Industrial temperature range: -40°C to +85°C
- Available in 32-pin (5mm x 5mm) MLF® package

DESCRIPTION

The SY58032U is a 2.5V/3.3V precision, high-speed, fully differential LVPECL 1:8 fanout buffer. The SY58032U is optimized to provide eight identical output copies with less than 20ps of skew and less than 10ps_{pp} total jitter. It can process clock signals as fast as 4GHz.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows the SY58032U to directly interface to LVPECL, CML, and LVDS differential signals (AC- or DC-coupled) without any level-shifting or termination resistor networks in the signal path. The result is a clean, stub-free, low-jitter interface solution. The LVPECL (100k temperature compensated) outputs feature 800mV typical swing into 50Ω loads, and provide an extremely fast rise/fall time guaranteed to be less than 110ps.

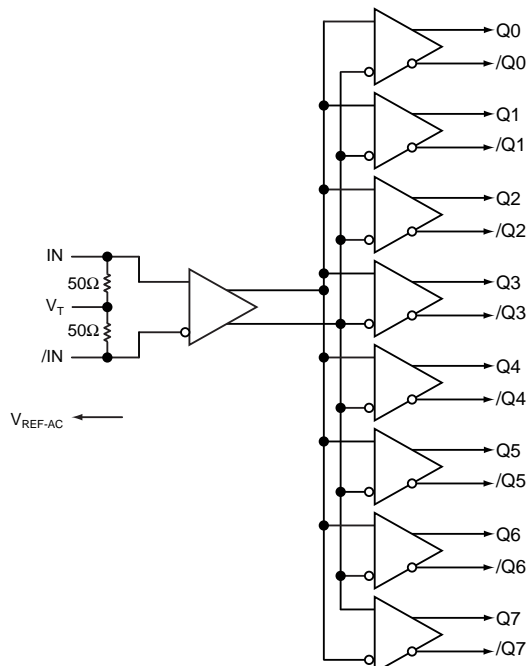
The SY58032U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (-40°C to +85°C). For applications that require a higher high-speed 1:8 fanout buffer, consider the SY58031U or SY58033U. The SY58032U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at www.micrel.com.

APPLICATIONS

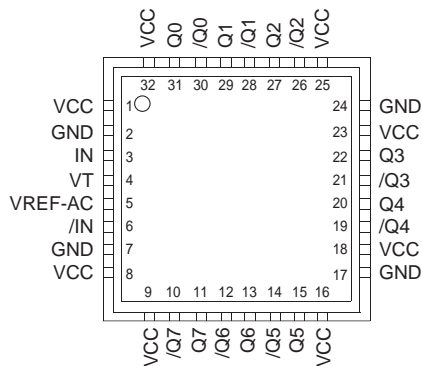
- All SONET and all GigE clock distribution
- All Fibre Channel clock and data distribution
- Network routing engine timing distribution
- High-end, low-skew multiprocessor synchronous clock distribution

FUNCTIONAL BLOCK DIAGRAM



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MicroLeadFrame and MLF are registered trademarks of Amkor Technology, Inc.

PACKAGE/ORDERING INFORMATION



32-Pin MLF® (MLF-32)

Ordering Information⁽¹⁾

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|--------------------------------|--------------|-----------------|--|----------------|
| SY58032UMI | MLF-32 | Industrial | SY58032U | Sn-Pb |
| SY58032UMITR ⁽²⁾ | MLF-32 | Industrial | SY58032U | Sn-Pb |
| SY58032UMG ⁽³⁾ | MLF-32 | Industrial | SY58032U with Pb-Free bar-line indicator | Pb-Free NiPdAu |
| SY58032UMGTR ^(2, 3) | MLF-32 | Industrial | SY58032U with Pb-Free bar-line indicator | Pb-Free NiPdAu |

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

PIN DESCRIPTION

| Pin Number | Pin Name | Pin Function |
|--|--|--|
| 3, 6 | IN, /IN | Differential Signal Input: Each pin of this pair internally terminates with 50Ω to the V _T pin. Note that this input will default to an indeterminate state if left open. See "Input Interface Applications" section. |
| 4 | VT | Input Termination Center-Tap: Each input terminates to this pin. The V _T pin provides a center-tap for each input (IN, /IN) to the termination network for maximum interface flexibility. See "Input Interface Applications" section. |
| 2, 7, 17, 24 | GND, Exposed Pad | Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin. |
| 1, 8, 9, 16, 18, 23, 25, 32 | VCC | Positive Power Supply: Bypass with 0.1μF™™0.01μF low ESR capacitors as close to the pins as possible. |
| 31, 30, 29, 28, 27, 26, 22, 21, 20, 19, 15, 14, 13, 12, 11, 10 | Q0, /Q0, Q1, /Q1, Q2, /Q2, Q3, /Q3, Q4, /Q4, Q5, /Q5, Q6, /Q6, Q7, /Q7 | 100k LVPECL Differential Output Pairs: Differential buffered output copy of the input signal. The LVPECL output swing is typically 800mV into 50Ω. Unused output pairs may be left floating with no impact on jitter. See "LVPECL Output" section. |
| 5 | VREF-AC | Bias Reference Voltage: Equal to V _{CC} -1.2V (typical), and used for AC-coupled applications. See "Input Interface Applications" section. When using V _{REF-AC} , bypass with 0.01μF capacitor to V _{CC} . Maximum sink/source current is 0.5mA. |

Absolute Maximum Ratings⁽¹⁾

Power Supply Voltage (V_{CC}) -0.5V to +4.0V
 Input Voltage (V_{IN}) -0.5V to V_{CC}
 Current (V_T)
 Source or sink current on V_T pin ±100mA
 Input Current (V_T)
 Source or sink current on IN, /IN ±50mA
 Current (V_{REF})
 Source or sink current on V_{REF-AC} ⁽³⁾ ±1.5mA
 Lead Temperature Soldering, (20 sec.) 260°C
 Storage Temperature Range (T_S) -65°C to +150°C

Operating Ratings⁽²⁾

Power Supply Voltage (V_{CC}) +2.375V to +3.60V
 Ambient Temperature Range (T_A) -40°C to +85°C
 Package Thermal Resistance⁽⁴⁾
 MLF® (θ_{JA})
 Still-Air 35°C/W
 MLF® (ψ_{JB})
 Junction-to-Board 20°C/W

DC ELECTRICAL CHARACTERISTICS⁽⁵⁾

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------------|---|--|--------------|--------------|--------------|----------|
| V_{CC} | Power Supply Voltage | 2.5V nominal 3.3V nominal | 2.375 3.0 | 2.5 3.3 | 2.625 3.6 | V |
| I_{CC} | Power Supply Current | $V_{CC} = \text{max.}$ No load. Includes current through 50 Ω pull-ups. | | 190 | 250 | mA |
| V_{IH} | Input HIGH Voltage | IN, /IN, Note 6 | $V_{CC}-1.6$ | | V_{CC} | V |
| V_{IL} | Input LOW Voltage | IN, /IN | 0 | | $V_{IH}-0.1$ | V |
| V_{IN} | Input Voltage Swing | IN, /IN, see Figure 1a. | 0.1 | | 1.7 | V |
| V_{DIFF_IN} | Differential Input Voltage Swing IN0, /IN0 , IN1, /IN1 | IN, /IN, see Figure 1b. | 0.2 | | | V |
| R_{IN} | In-to- V_T Resistance | | 40 | 50 | 60 | Ω |
| $V_{T\ IN}$ | Max. In-to- V_T (IN, /IN) | | | | 1.28 | V |
| V_{REF-AC} | | | $V_{CC}-1.3$ | $V_{CC}-1.2$ | $V_{CC}-1.1$ | V |

LVPECL DC ELECTRICAL CHARACTERISTICS⁽⁵⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $R_L = 50\Omega$ to $V_{CC}-2V$; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-----------------|----------------------------|----------------|----------------|------|----------------|-------|
| V_{OH} | Output HIGH Voltage | | $V_{CC}-1.145$ | | $V_{CC}-0.895$ | V |
| V_{OL} | Output LOW Voltage | | $V_{CC}-1.945$ | | $V_{CC}-1.695$ | V |
| V_{OUT} | Output Voltage Swing | see Figure 1a. | 500 | 800 | | mV |
| V_{DIFF_OUT} | Differential Voltage Swing | see Figure 1b. | 1000 | 1600 | 2000 | mV |

Notes:

1. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability, use for input of the same package only.
4. Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB. ψ_{JB} uses 4-layer θ_{JA} in still-air number unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above tables after thermal equilibrium has been established.
6. V_{IH} (min) not lower than 1.2V.

AC ELECTRICAL CHARACTERISTICS⁽⁷⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $R_L = 50\Omega$ to $V_{CC} - 2V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|------------------|--|-----------------------------------|-----|-----|-----|-------------------|
| f_{MAX} | Maximum Operating Frequency | $V_{OUT} \geq 400mV$ Clock | 4 | | | GHz |
| t_{pd} | Propagation Delay (IN-to-Q) | | 180 | 260 | 330 | ps |
| $t_{pd\ tempco}$ | Differential Propagation Delay Temperature Coefficient | | | 35 | | fs/°C |
| t_{SKEW} | Output-to-Output Skew (within Device) | Note 8 | | 7 | 20 | ps |
| | Part-to-Part Skew | Note 9 | | | 100 | ps |
| t_{JITTER} | Clock Cycle-to-Cycle Jitter | Note 10 | | | 1 | ps _{RMS} |
| | Total Jitter (Clock) | Note 11 | | | 10 | ps _{PP} |
| | Random Jitter (RJ) | Note 12 | | | 1 | ps _{RMS} |
| t_r, t_f | Output Rise/Fall Time | 20% to 80%, at full output swing. | 35 | 75 | 110 | ps |

Notes:

- High frequency AC electricals are guaranteed by design and characterization. All outputs loaded with 50Ω to $V_{CC} - 2V$, $V_{IN} \geq 100mV$.
- Output-to-output skew is measured between outputs under identical transitions.
- Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs. Part-to-part skew includes variation in t_{pd} .
- Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
- Total jitter definition: with an ideal clock input of frequency - f_{MAX} , no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
- Random jitter is measured with a K28.7 comma detect character pattern, measured at 1.25Gbps and 2.5Gbps.

SINGLE-ENDED AND DIFFERENTIAL SWINGS

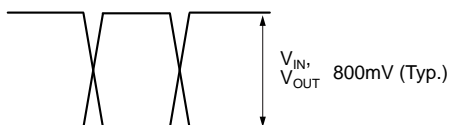


Figure 1a. Single-Ended Voltage Swing

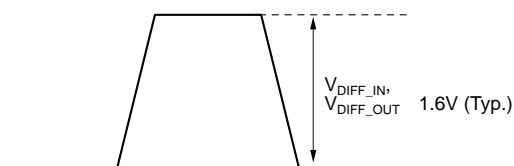
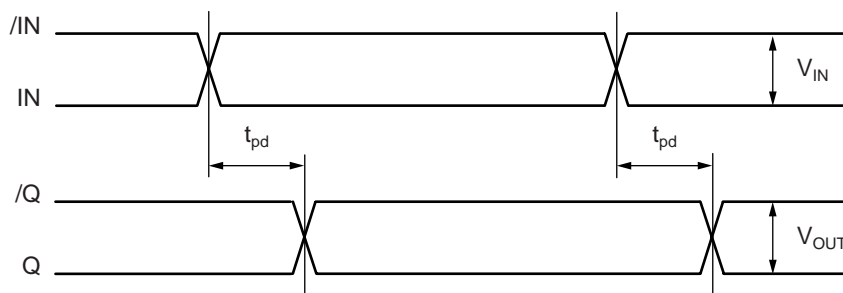


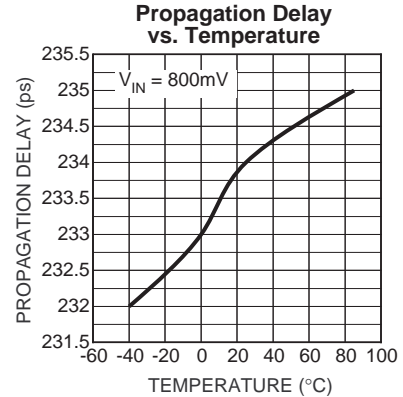
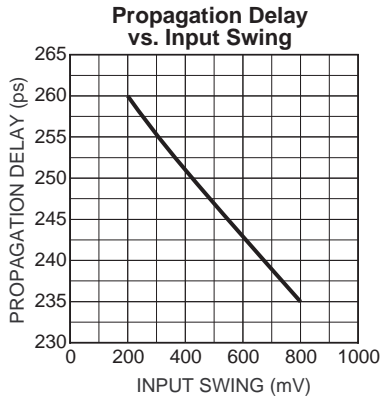
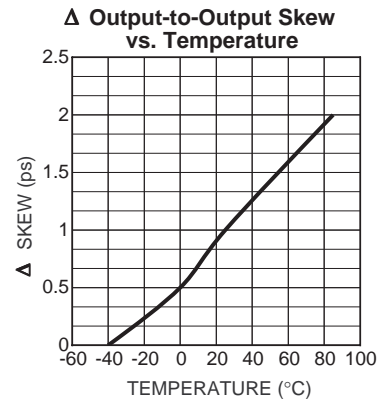
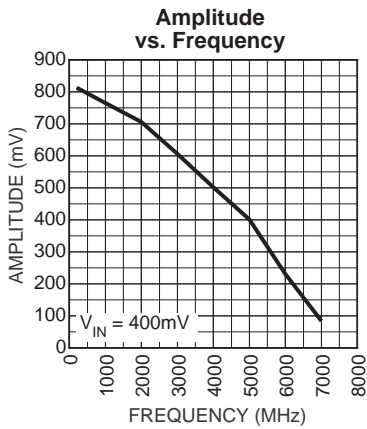
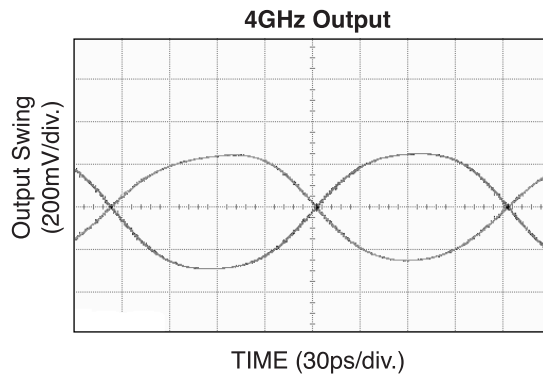
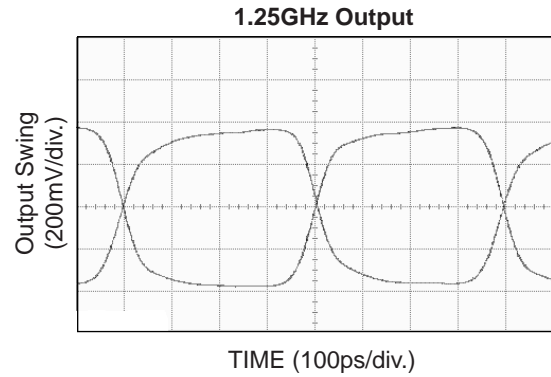
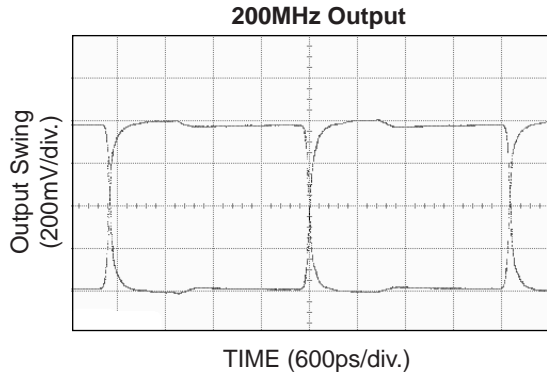
Figure 1b. Differential Voltage Swing

TIMING DIAGRAM



TYPICAL OPERATING CHARACTERISTICS

$V_{CC} = 2.5V$, $GND = 0$, $V_{IN} = 100mV$, $T_A = 25^\circ C$, unless otherwise stated.



INPUT BUFFER

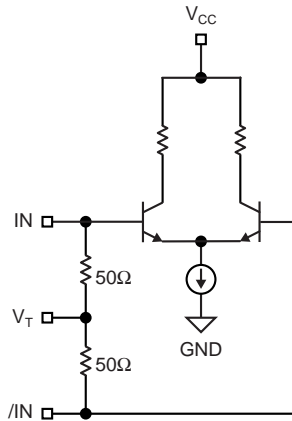


Figure 2. Simplified Differential Input Buffer

INPUT INTERFACE APPLICATIONS

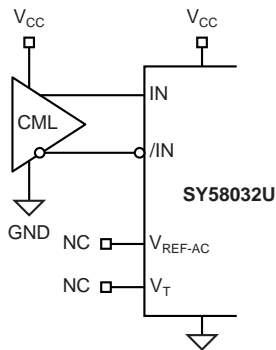


Figure 3a. DC-Coupled CML Input Interface
Option: May connect V_T to V_{CC} .

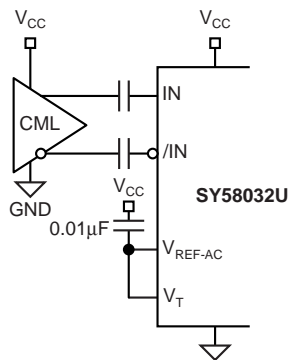


Figure 3b. AC-Coupled CML Input Interface

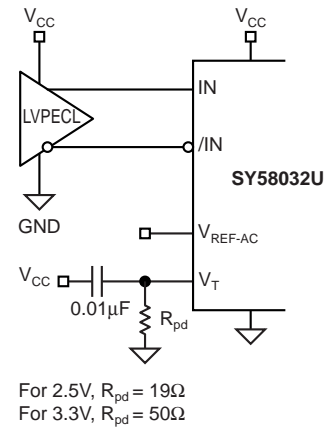


Figure 3c. LVPECL Input Interface

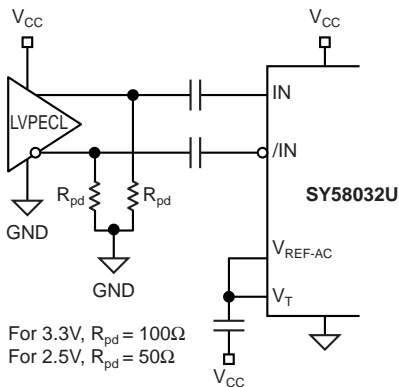


Figure 3d. AC-Coupled LVPECL Input Interface

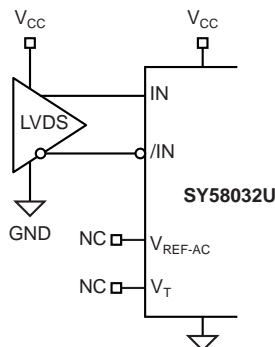


Figure 3e. LVDS Input Interface

LVPECL OUTPUT

LVPECL has high input impedance, and very low output impedance (open emitter), and small signal swing which results in low EMI. LVPECL is ideal for driving 50Ω and 100Ω controlled impedance transmission lines. There are several techniques for terminating the LVPECL

output: Parallel Termination-Thevenin Equivalent, Parallel Termination (3-resistor), and AC-coupled Termination. Unused output pairs may be left floating. However, single-ended outputs must be terminated, or balanced.

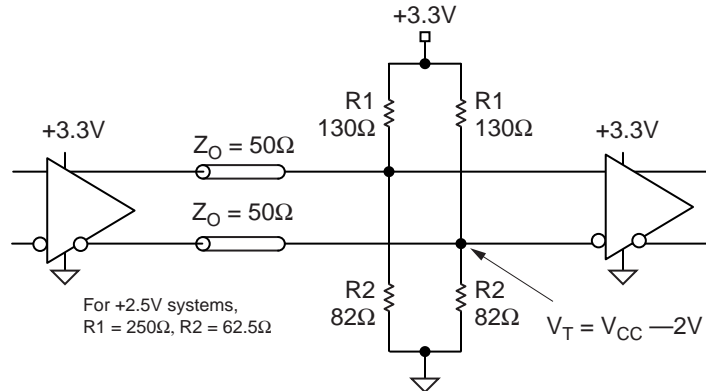
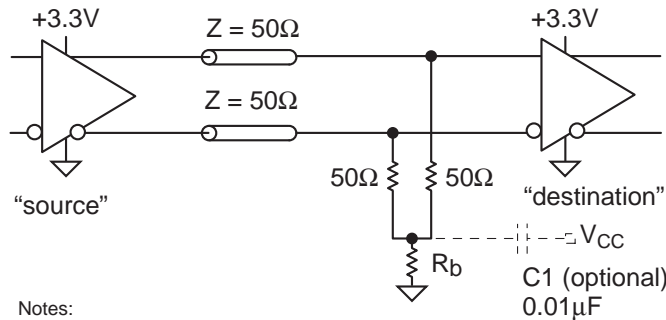


Figure 4. Parallel Termination-Thevenin Equivalent



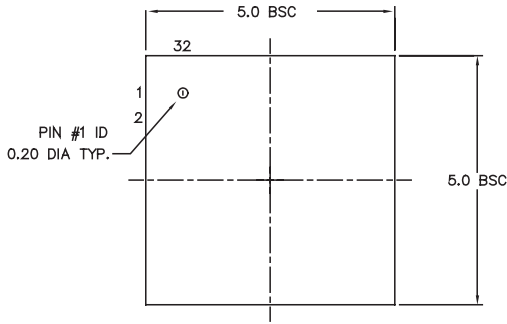
- Notes:
1. Power-saving alternative to Thevenin termination.
 2. Place termination resistors as close to destination inputs as possible.
 3. R_b resistor sets the DC bias voltage, equal to V_T.
 4. For 2.5V systems, R_b = 19Ω, For 3.3V systems, R_b = 50Ω

Figure 5. Parallel Termination (3-Resistor)

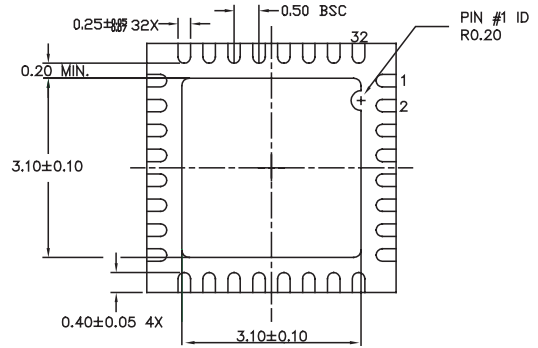
RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

| Part Number | Function | Data Sheet Link |
|-------------|---|--|
| SY58031U | Ultra-Precision 1:8 Fanout Buffer with 400mV CML Outputs and Internal I/O Termination | http://www.micrel.com/product-info/products/sy58031u.shtml |
| SY58032U | Ultra-Precision 1:8 Fanout Buffer with LVPECL Outputs and Internal Termination | http://www.micrel.com/product-info/products/sy58032u.shtml |
| SY58033U | Ultra-Precision 1:8 Fanout Buffer with 400mV LVPECL Outputs and Internal Termination | http://www.micrel.com/product-info/products/sy58033u.shtml |
| | 32-MLF® Manufacturing Guidelines Exposed Pad Application Note | www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf |
| | HBW Solutions | http://www.micrel.com/product-info/as/solutions.shtml |

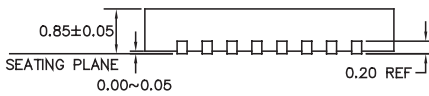
32-PIN MicroLeadFrame® (MLF-32)



TOP VIEW

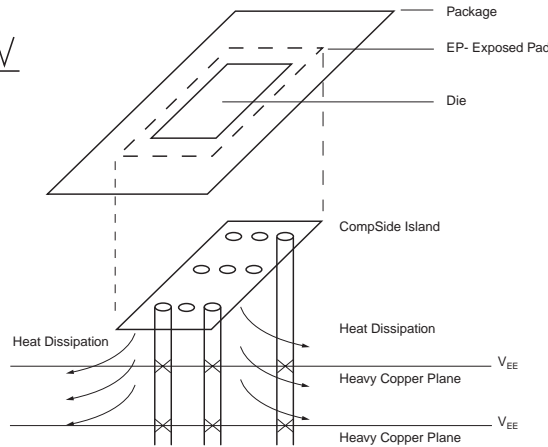


BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. MAX. PACKAGE WARPAGE IS 0.05 mm.
 3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
 4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



**PCB Thermal Consideration for 32-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)**

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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