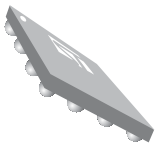
STCD22x0, STCD23x0, STCD24x0

Multichannel clock distribution circuit

Features

- 2, 3 or 4 output buffered clock distribution
- Single-ended square wave (or sine wave) clock input
- Rail-to-rail (0 V to VTCXO) square wave output
- Individual enable pin for each output
- 1.8 V, high PSRR LDO for external clock source voltage supply (VTCXO)
- No AC coupling capacitor needed
- Ultra-low phase noise and standby current
- Common system clock request, open drain, active low
- Clock enable signal polarities factory programmable (STCD23x0)
- Option pins allow clock enable polarities to be user configurable (STCD22x0 and STCD24x0)
- High isolation output-to-output & output-to-input
- 2.5 V to 5.1 V battery supply voltage
- 40 pF max load driving capability per output
- Available in chip scale package (CSP)
- Operating temperature : –20 °C to 85 °C



Flip Chip (12-bump, 16-bump)

Applications

- Multimode RF clock reference
- Baseband peripheral device clock reference
- Mobile Internet Devices (MIDs)

Table 1. Device summary

Reference	Part number	Channels	Enable polarity	Package
STCD22x0	STCD2200(1)	2-channel	User program	Flip Chip 12-bump (1.2 mm x 1.6 mm)
STCD24x0	STCD2400	4-channel	User program	Flip Chip 16-bump (1.6 mm x 1.6 mm)
	STCD2410(1)			
STCD23x0	STCD2300(1)	3-channel	Factory program	Flip Chip 12-bump (1.2 mm x 1.6 mm)
	STCD2310(1)			
	STCD2320(1)			
	STCD2330(1)			

1. Contact local ST sales office for availability.

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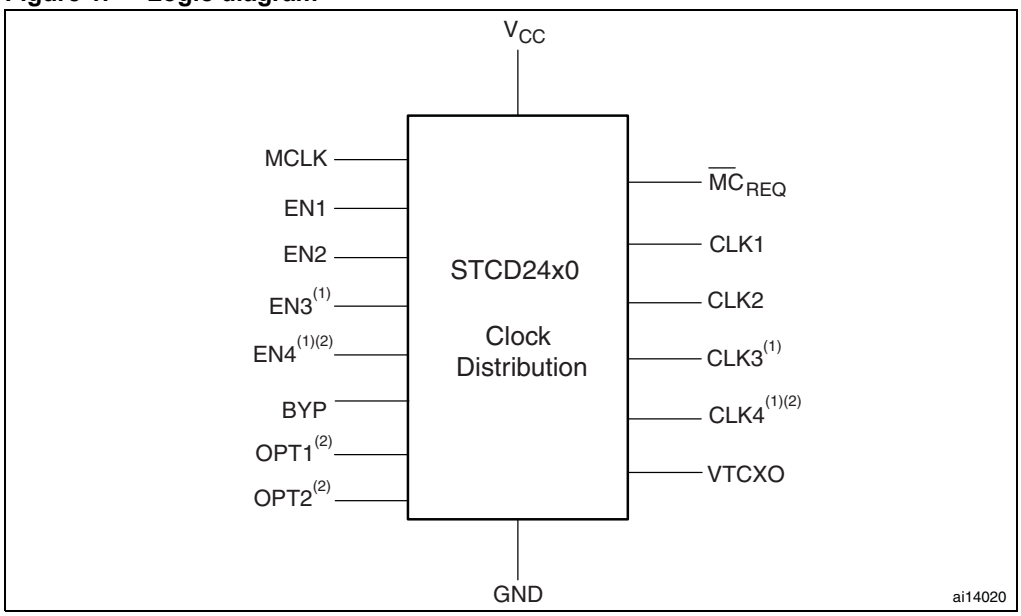
1 Description

The STCD22x0, STCD23x0 and STCD24x0 are 2, 3 or 4 output clock distribution circuits which accept external square wave or sine wave signals and output rail-to-rail (0 V to VTCXO) square wave signals. They are used to provide a common frequency clock to multimode mobile RF applications. They can also be used for those baseband peripheral applications in mobile phones such as WLAN, Bluetooth, GPS and DVB-H as the clock reference. The STCD22x0, STCD23x0 and STCD24x0 isolate each device driven by their clock outputs and minimize interference between the devices. Each of the clock buffers can be disabled to lower the power consumption whenever the connected device does not need the clock. The STCD22x0, STCD23x0 and STCD24x0 accept commonly used mobile master clock frequencies ranging from 10 MHz to 52 MHz.

The STCD22x0, STCD23x0 and STCD24x0 have a common clock request (open drain output, active low) controlling the external clock source. A 1.8 V, high PSRR LDO is also integrated in the STCD22x0, STCD23x0 and STCD24x0 to supply power to the external clock source (for example, TCXO). STMicroelectronics offers different versions for the enable polarities. The STCD22x0, STCD23x0 and STCD24x0 are available in, respectively, 1.2 mm x 1.6 mm (12-bump), 1.2 mm x 1.6 mm (12-bump) and 1.6 mm x 1.6 mm (16-bump) chip scale packages and can be operated with a battery supply voltage ranging from 2.5 V to 5.1 V. The operating temperature is –20 to +85 °C.

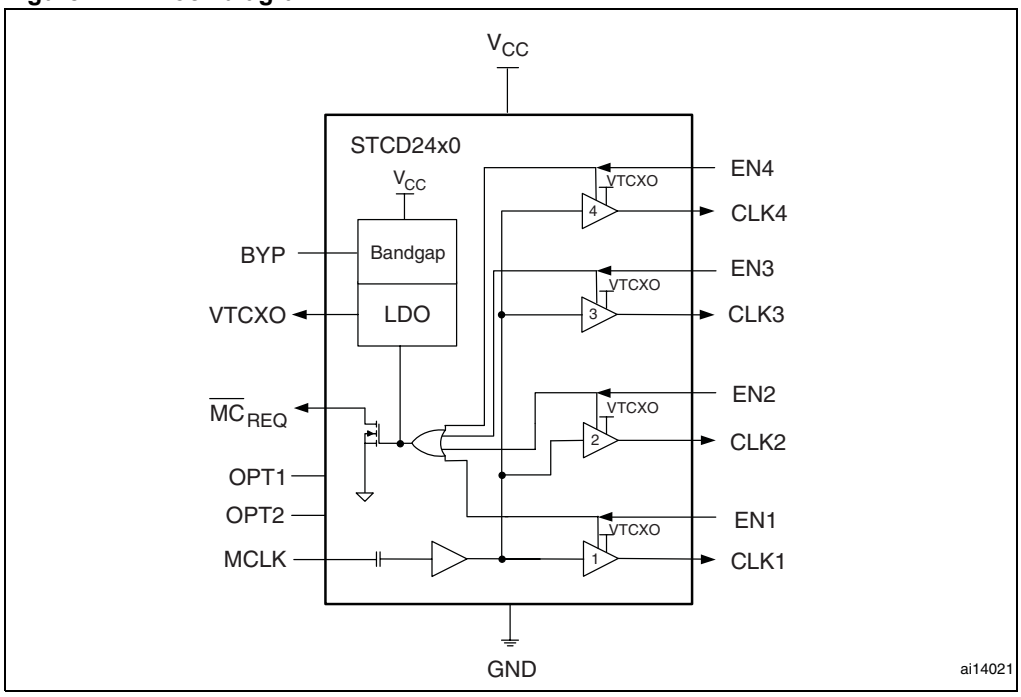
2 Device overview

Figure 1. Logic diagram



1. EN3, CLK3, EN4, and CLK4 do not exist for STCD22x0.
2. OPT1, OPT2, EN4, and CLK4 do not exist for STCD23x0.

Figure 2. Block diagram



Note: Enable signals (EN1-4) can be factory programmed either active high or active low for STCD23x0 and can have different polarity options by configuring OPT1 and OPT2 for STCD22x0 and STCD24x0. Master clock request ($\overline{MC}_{REQ}$) is open drain output and active low.

Figure 3. Hardware hookup (master clock enable active low)

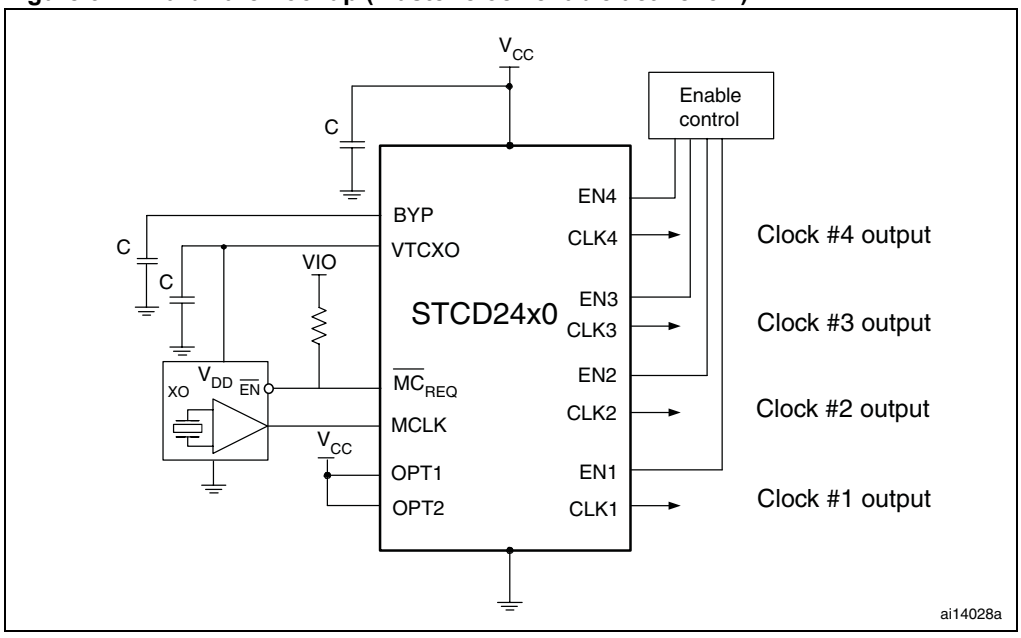


Figure 4. Hardware hookup (master clock enable active high)

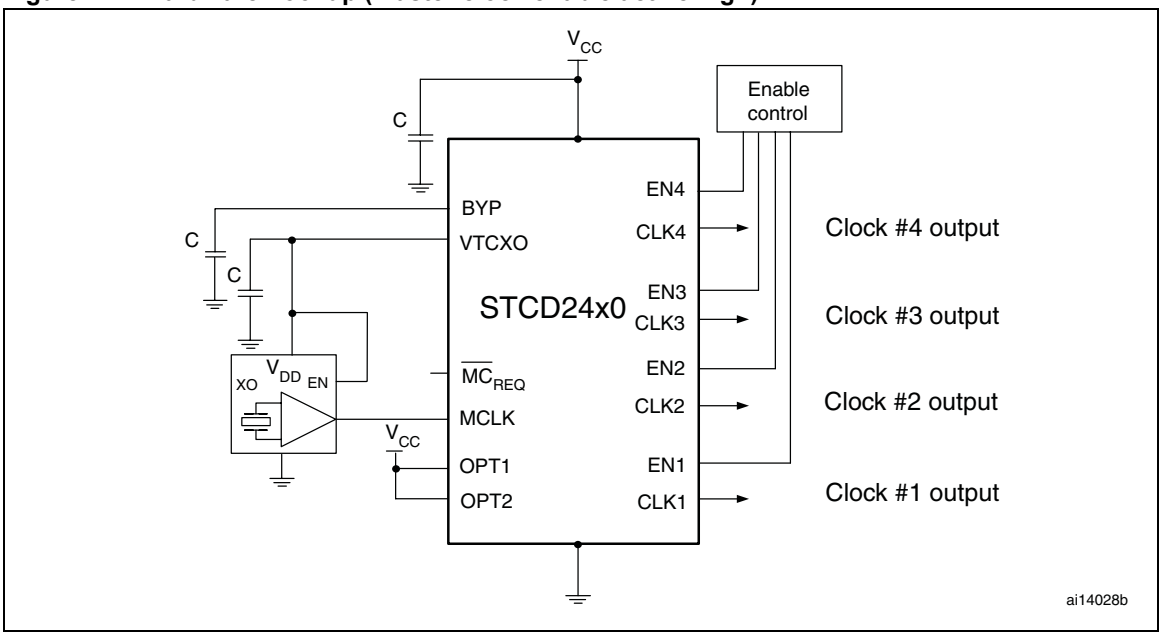
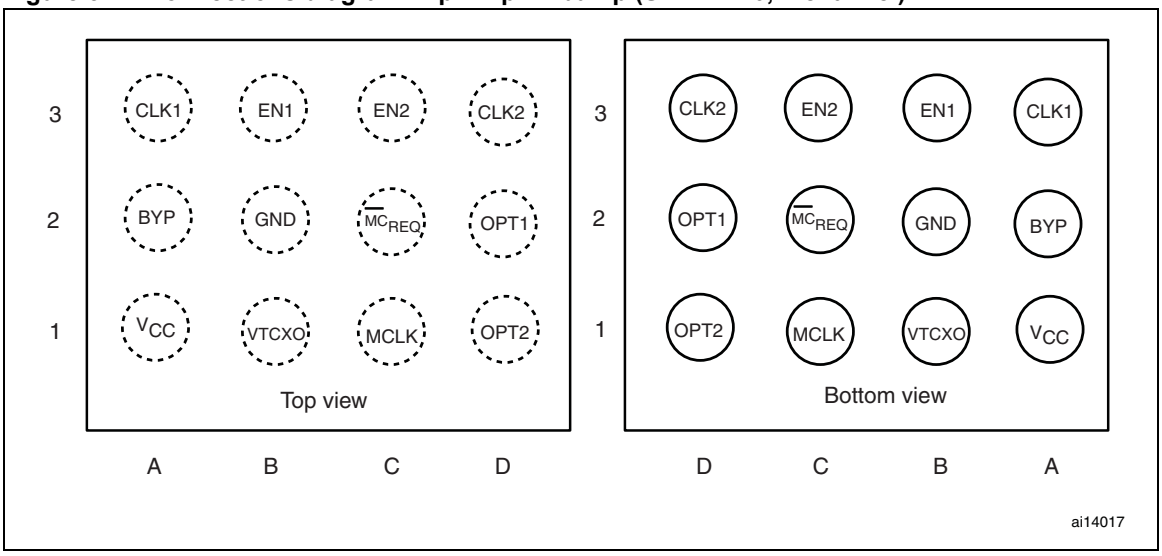
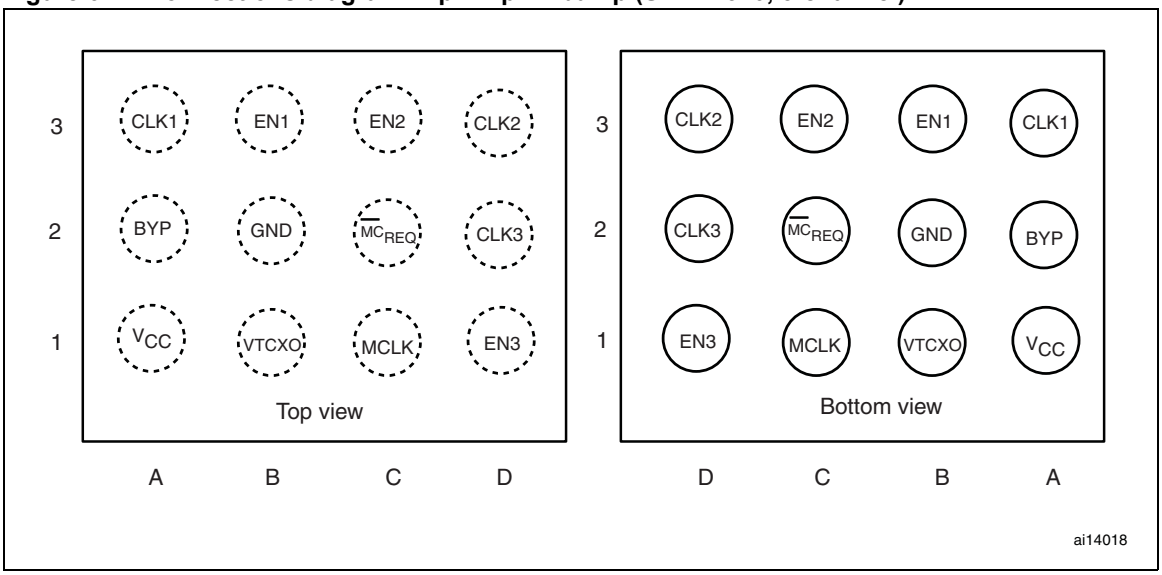


Figure 5. Connections diagram Flip Chip 12-bump (STCD22x0, 2-channel)



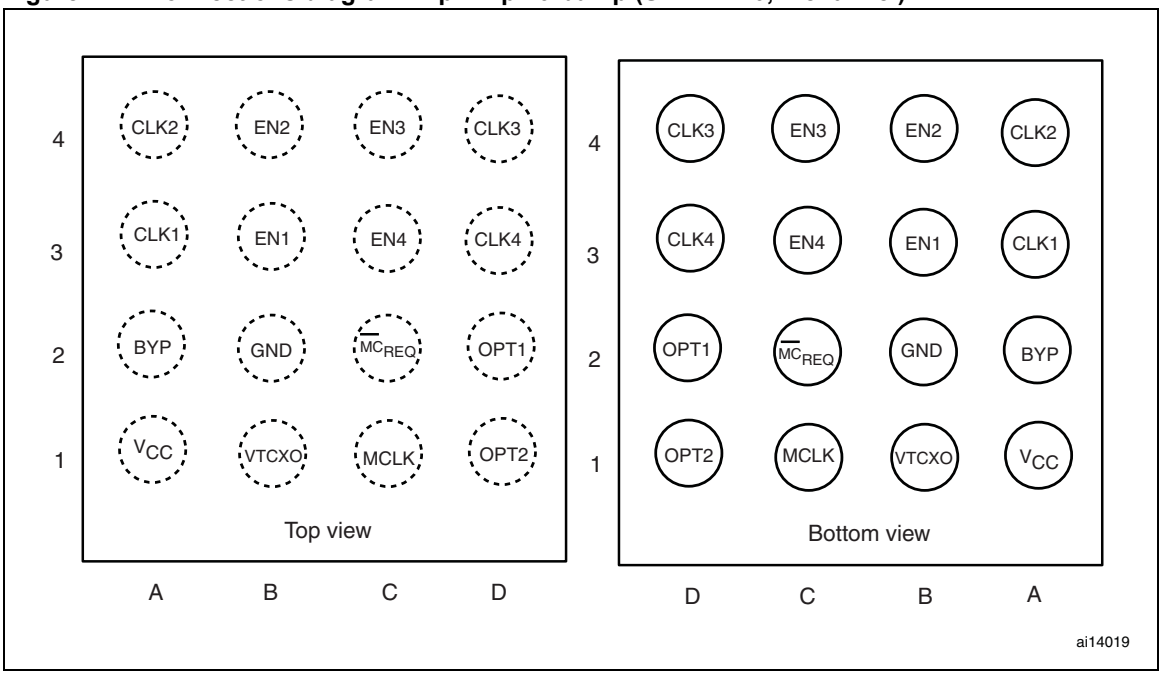
Note: OPT1 is used to configure EN1 polarity. Connect OPT1 to V_{CC} to configure EN1 active high or connect OPT1 to GND to configure EN1 active low. In the same way OPT2 is used to configure EN2.

Figure 6. Connections diagram Flip Chip 12-bump (STCD23x0, 3-channel)



Note: EN1~EN3 can be active high or active low. STMicroelectronics offers several polarity options, refer to Section 3.2: Enable polarity for detailed information.

Figure 7. Connections diagram Flip Chip 16-bump (STCD24x0, 4-channel)



Note: OPT1 is used to configure EN1 and EN2 polarity. Connect OPT1 to V_{CC} to configure EN1 and EN2 active high or connect OPT1 to GND to configure EN1 and EN2 active low. In the same way OPT2 is used to configure EN3 and EN4. STMicroelectronics offers different control options, refer to Section 3.2: Enable polarity for detailed information.

Table 2. Pin functions (STCD22x0, 2-channel)

Pin number	Pin name	Description
A1	V_{CC}	Supply voltage (decouple with a 1 µF capacitor to GND)
B1	VTCXO	LDO output for external clock source (decouple with a 1 µF capacitor to GND)
C1	MCLK	Master clock input
D1	OPT2	Optional pin 2. Connect to V_{CC} or GND on PC board to field configure EN2 active high/low. Refer to *Section 3.2: Enable polarity* for detailed information.
A2	BYP	Bypass capacitor input pin (10 nF capacitor should be connected to GND in order to improve thermal noise performance)
B2	GND	Supply ground
C2	$\overline{MC}_{REQ}$	Master clock request signal (open drain, active low)
D2	OPT1	Optional pin 1. Connect to V_{CC} or GND on PC board to field configure EN1 active high/low. Refer to *Section 3.2: Enable polarity* for detailed information.
A3	CLK1	Clock output channel - output 1
B3	EN1	Clock output channel enable-1 (active high/low OPT1 field programmable)
C3	EN2	Clock output channel enable-2 (active high/low OPT2 field programmable)
D3	CLK2	Clock output channel - output 2

Table 3. Pin functions (STCD23x0, 3-channel)

Pin number	Pin name	Description
A1	V_{CC}	Supply voltage (decouple with a 1 µF capacitor to GND)
B1	VTCXO	LDO output for external clock source (decouple with a 1 µF capacitor to GND)
C1	MCLK	Master clock input
D1	EN3	Clock output channel enable-3 (active high/low factory laser programmable)
A2	BYP	Bypass capacitor input pin (10 nF capacitor should be connected to GND in order to improve thermal noise performance)
B2	GND	Supply ground
C2	$\overline{MC}_{REQ}$	Master clock request signal (open drain, active low)
D2	CLK3	Clock output channel - output 3
A3	CLK1	Clock output channel - output 1
B3	EN1	Clock output channel enable-1 (active high/low factory laser programmable)
C3	EN2	Clock output channel enable-2 (active high/low factory laser programmable)
D3	CLK2	Clock output channel - output 2

Table 4. Pin functions (STCD24x0, 4-channel)

Pin number	Pin name	Description
A1	V_{CC}	Supply voltage (decouple with a 1 µF capacitor to GND)
B1	VTCXO	LDO output for external clock source (decouple with a 1 µF capacitor to GND)
C1	MCLK	Master clock input
D1	OPT2	Optional pin 2. Connect to V_{CC} or GND on PC board to field configure EN3 and EN4 active high/low. Refer to *Section 3.2: Enable polarity* for detailed information.
A2	BYP	Bypass capacitor input pin (10 nF capacitor should be connected to GND in order to improve thermal noise performance)
B2	GND	Supply ground
C2	$\overline{MC}_{REQ}$	Master clock request signal (open drain, active low)
D2	OPT1	Optional pin 1. Connect to V_{CC} or GND on PC board to field configure EN1 and EN2 active high/low. Refer to *Section 3.2: Enable polarity* for detailed information.
A3	CLK1	Clock output channel - output 1
B3	EN1	Clock output channel enable-1 (active high/low OPT1 field programmable)
C3	EN4	Clock output channel enable-4 (active high/low OPT2 field programmable)
D3	CLK4	Clock output channel - output 4
A4	CLK2	Clock output channel - output 2
B4	EN2	Clock output channel enable-2 (active high/low OPT1 field programmable)
C4	EN3	Clock output channel enable-3 (active high/low OPT2 field programmable)
D4	CLK3	Clock output channel - output 3

3 Device operation

3.1 Operation

The STCD22x0, STCD23x0 and STCD24x0 are 2, 3 or 4 buffered clock distribution circuits. They accept the clock (either square wave or sine wave) input from an external clock source and send 2, 3 or 4 buffered rail-to-rail (0 V to VTCXO) square wave outputs to different devices. A 1.8 V, high PSRR LDO (VTCXO) is also integrated in the STCD22x0, STCD23x0 and STCD24x0 which can be used as a voltage supply for the external master clock source (such as a TCXO). This LDO stops the current increase through PMOS when the load current reaches the limit value of the current-limit protection circuit. When the load current falls below the limit values, the current limit is released.

Each of the STCD22x0, STCD23x0 and STCD24x0 clock outputs can be enabled individually. If the device connected to the output is in standby, and does not require a clock, the buffered output can be disabled to save power consumption. Once the buffered output is disabled, it is pulled down to GND internally. If all the devices connected are in standby, the STCD22x0, STCD23x0 and STCD24x0 are also put into standby mode (the internal LDO is also shut down) for further power consumption savings. All of the output enable signals are logic ORed with an open drain output ($\overline{MC}_{REQ}$) to control the output of the source clock. If the output clock is required by at least one device, the LDO wakes up and the $\overline{MC}_{REQ}$ activates the clock source. The truth table for enable signals, the master clock request signal and the VTCXO is given in *Table 5*. The truth table for enable signals, output clock signals and the master clock is given in *Table 6*.

The STCD22x0, STCD23x0 and STCD24x0 have the master clock input detector integrated. If the input master clock peak-to-peak voltage is below the minimum specified level, even if the outputs are enabled, there are no clock outputs and STCD22x0, STCD23x0 and STCD24x0 enter standby mode. Once the master clock peak-to-peak voltage level reaches the minimum value, the output clocks are asserted if the enable pins are active.

In *Table 5* and *6*, the enable signals are active high and the $\overline{MC}_{REQ}$ is active low. These enable signals can be active high or active low. The enable polarity is described in *Section 3.2: Enable polarity*. Customers can select different polarity options for different applications. Contact the STMicroelectronics local sales office for availability.

Table 5. Truth table for clock enable (EN1-4), master clock request ($\overline{MC}_{REQ}$) and VTCXO

EN1	EN2	EN3	EN4	$\overline{MC}_{REQ}$	VTCXO
0	0	0	0	1	GND
1	0	0	0	0	1.8 V
1	1	0	0	0	1.8 V
-	-	-	-	0	1.8 V
1	1	1	1	0	1.8 V

Note: "0" means logic low which disables the clock output and "1" means logic high which enables the clock output. This is an active high truth table. Refer to Section 3.2: Enable polarity for the detailed enable active high/low options.

Table 6. Truth table for enable signals (EN1-4), master clock input (MCLK) and output clocks (CLK1-4)

EN1	EN2	EN3	EN4	MCLK	CLK1	CLK2	CLK3	CLK4
0	0	0	0	X	NO CLOCK	NO CLOCK	NO CLOCK	NO CLOCK
1	0	0	0	CLOCK	CLOCK	NO CLOCK	NO CLOCK	NO CLOCK
1	1	0	0	CLOCK	CLOCK	CLOCK	NO CLOCK	NO CLOCK
-	-	-	-	-	-	-	-	-
1	1	1	1	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK

Note: "0" means logic low and "1" means logic high. When there is NO CLOCK output, the CLKx pin stays at logic low. "X" means don't care. This is an active high truth table. Refer to Section 3.2: Enable polarity for the detailed enable active high/low options.

3.2 Enable polarity

In different applications, the user may have different requirements for enable active high or active low (enable polarities). $\overline{MC}_{REQ}$ is active low. STMicroelectronics offers different solutions for the user to obtain different enable polarities.

In the STCD22x0 and STCD24x0, the user can configure the enable active high or active low on the PC board by connecting OPT1 and OPT2 to either V_{CC} or ground. Refer to *Table 7* for detailed information.

In the STCD23x0, STMicroelectronics offers 4 enable polarity options by factory programming for the user. Refer to *Table 7* for detailed information.

The user should note that OPT1 and OPT2 must be connected to either V_{CC} or GND on the PC board and floating on these pins could cause problems.

Table 7. STCD22x0, STCD23x0 and STCD24x0 and enable polarity options

Part number	Enable polarities (OPT1, OPT2)	Enable polarity program method
STCD2200	OPT1 connected to V_{CC}, EN1 active high OPT1 connected to GND, EN1 active low OPT2 controls EN2	User program
STCD2400	OPT1 connected to V_{CC}, EN1 and EN2 active high OPT1 connected to GND, EN1 and EN2 active low OPT2 controls EN3 and EN4	
STCD2410	OPT1 connected to V_{CC}, EN1 active high OPT1 connected to GND, EN1 active low OPT2 controls EN2, EN3, and EN4	
STCD2300	EN1, EN2 and EN3 all active low	Factory program
STCD2310	EN1, EN2 active low, and EN3 active high	
STCD2320	EN1, EN2 active high and EN3 active low	
STCD2330	EN1, EN2 and EN3 all active high	

4 Application information

4.1 LDO input capacitor

A 1 µF input capacitor is required for the input of the LDO of the STCD22x0, STCD23x0 and STCD24x0 (the amount of capacitance can be increased without limit). This capacitor must be located as close as possible to the V_{CC} pin on the PC board and return to a clean analog ground. Any good quality ceramic, tantalum or film capacitor can be used for this capacitor.

4.2 LDO output capacitor

A 1 µF external capacitor is required for the output VTCXO of the LDO of the STCD22x0, STCD23x0 and STCD24x0. The STCD22x0, STCD23x0 and STCD24x0 are designed to work with low ESR (equivalent series resistance) ceramic capacitors. Make sure the ESR is lower than 500 mΩ to stabilize the VTCXO. Also, capacitor tolerance and variation with temperature must be considered to assure the minimum amount of capacitance provided at all times. This capacitor should be located as close as possible to the VTCXO pin on the PC board.

4.3 LDO BYP pin

A 10 nF ceramic capacitor is required for the LDO BYP pin to ensure lower noise. Any good quality ceramic, tantalum or film capacitor can be used. The capacitor should be located as close as possible to the BYP pin on the PC board.

4.4 $\overline{MC}_{REQ}$ pin

In the STCD22x0, STCD23x0, and STCD24x0, the $\overline{MC}_{REQ}$ pin is open drain and active low.

Since $\overline{MC}_{REQ}$ is active low, if none of the clock output is required, the STCD22x0, STCD23x0 and STCD24x0 are set to standby mode which turns off the internal LDO VTCXO.

$\overline{MC}_{REQ}$ is designed as an open drain structure. A pull-up resistor (50 kΩ recommended) is needed on the PC board to connect this pin to an external 1.8 V supply. Make sure the current flowing through this pin is kept within 3 mA to guarantee the proper function of the circuit.

If the $\overline{MC}_{REQ}$ function is not used in the application, the user can connect this pin to GND or leave it unconnected. Other functions of the STCD2xx0 will not be affected.

4.5 Phase noise

Phase noise is a frequency domain phenomenon and is a critical specification in reference clocks. It is illustrated by a continuous spreading of the energy of the wave mainly caused by random noise. The phase noise is normally specified with a unit of dBc/Hz at a given offset in frequency (for example, 10 kHz) from the carrier wave (for example, 26 MHz). The value of the phase noise is the difference of the power contained within 1 Hz bandwidth of the offset frequency to the power at the carrier frequency. The total phase noise of the clock tree is obtained by adding the additive phase noise of STCD22x0, STCD23x0 and STCD24x0 and the phase noise of the clock source (for example, TCXO) in power which is illustrated in *Equation 1*.

Equation 1

$$PN_T = 10\log(10^{\frac{PN_C}{10}} + 10^{\frac{PN_X}{10}}) < PN_A$$

where:

PN_T is the total phase noise in dBc/Hz

PN_C is the additive phase noise of STCD22x0, STCD23x0 and STCD24x0 and

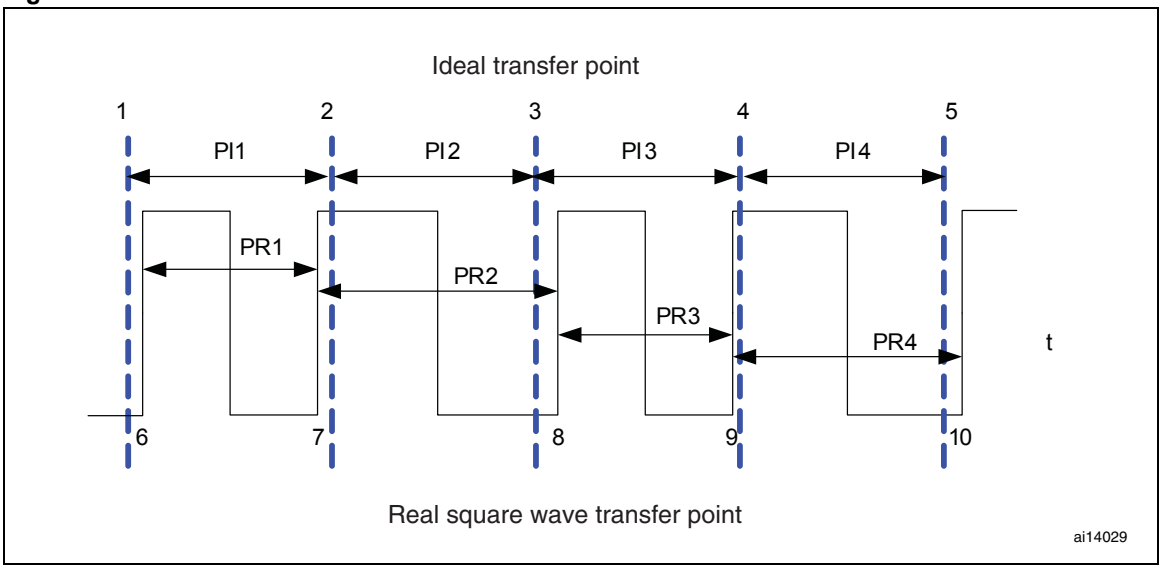
PN_X is the phase noise of clock source

Make sure the total phase noise is kept within the phase noise requirement of each application PN_A. The user should choose the right TCXO with proper phase noise to meet the requirement.

4.6 Jitter

In the time domain, energy spreading can result in jitter, which is the same phenomenon as phase noise in the frequency domain. As a sine wave passes its zero-crossing or a square wave changes state, the real clock signal transition is not exactly the same as the ideal case, thus causing variation in the waveform transition point. This deviation of the transition point is known as jitter as illustrated in *Figure 8*.

Figure 8. Jitter



In *Figure 8* the square wave ideal transition point should happen at points 1, 2, 3, 4 and 5, and each "ideal" period PI1 to PI4 should be the same, thus no time jitter has occurred. Actually, the real transition point happens at points 6, 7, 8, 9 and 10, thus causing "real" periods PR1 to PR4 to not be the same, and exhibit visible jitter. If each of the real periods of the cycles (PR1 to PR4) is measured, period jitter is obtained. The cycle-to-cycle jitter is also obtained by calculating the difference between two adjacent periods (for example, PR2-PR1, PR3-PR2 …).

These periods of jitter are described as peak-to-peak jitter and are calculated by subtracting the minimum value from the maximum value or may also be described by the root-mean-square (RMS) value, representing one standard deviation of the Gaussian distribution.

4.7 Output trace line

The STCD22x0, STCD23x0 and STCD24x0 is designed with maximum 50 Ω impedance output. On the PC board, a 50 Ω transmission line with proper series termination should be used to avoid signal distortion and reflection.

4.8 Typical application connections

The STCD2400 clock distribution circuit requires a source clock input as the reference clock (for example, XO). At most 4 devices can be connected to the outputs. The typical application circuit using STCD2400 is shown in *Figure 9* and *10* . The $\overline{MC}_{REQ}$ is open drain output and active low. A pull-up resistor is needed to connect to an external 1.8 V supply VIO. If the clock source enable is active high, the user can use VTCXO as the master clock enable control signal, please refer to *Figure 4* for the detailed connection.

In *Figure 9*, the clock from XO is distributed to the TD-SCDMA transmitter and receiver and GSM transceiver separately to be used as reference clocks.

In *Figure 10*, the buffer #4 output is fed into the Bluetooth system. In order to allow minimum power consumption, a Bluetooth system always has a clock request feature. If the Bluetooth system does not require the clock, the clock request disables the clock output. The enable pins can also be connected to an external 1.8 V supply to force the buffer to always be on.

In *Figure 9* and *10*, all the output clock enables are active high since both OPT1 and OPT2 are connected to V_{CC}.

Figure 9. Typical application circuit using STCD24x0 for RF ends of TD-SCDMA/GSM dual-mode mobile phone

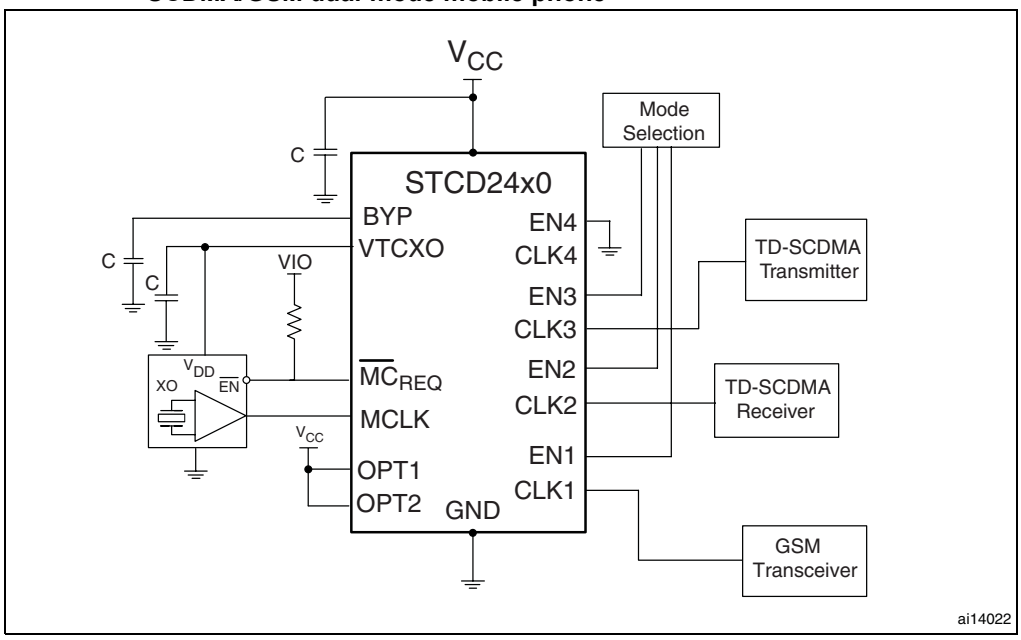
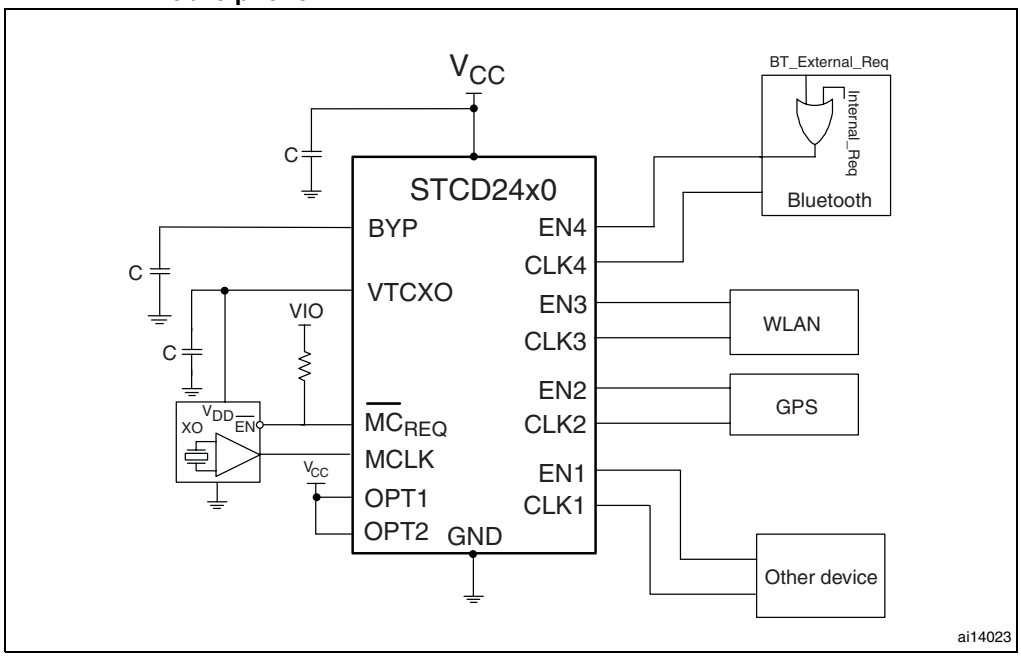


Figure 10. Typical application circuit using STCD24x0 for baseband peripherals in mobile phone



5 Typical operating characteristics

Typical operating characteristics are at T_A = 25 °C, C_{load} = 20 pF at each channel, V_{CC} = 3.8 V, f_{MCLK} = 26 MHz.

Figure 11. Quiescent current vs. supply voltage (EN1 = EN2 = EN3 = EN4 = 1, no master clock input)

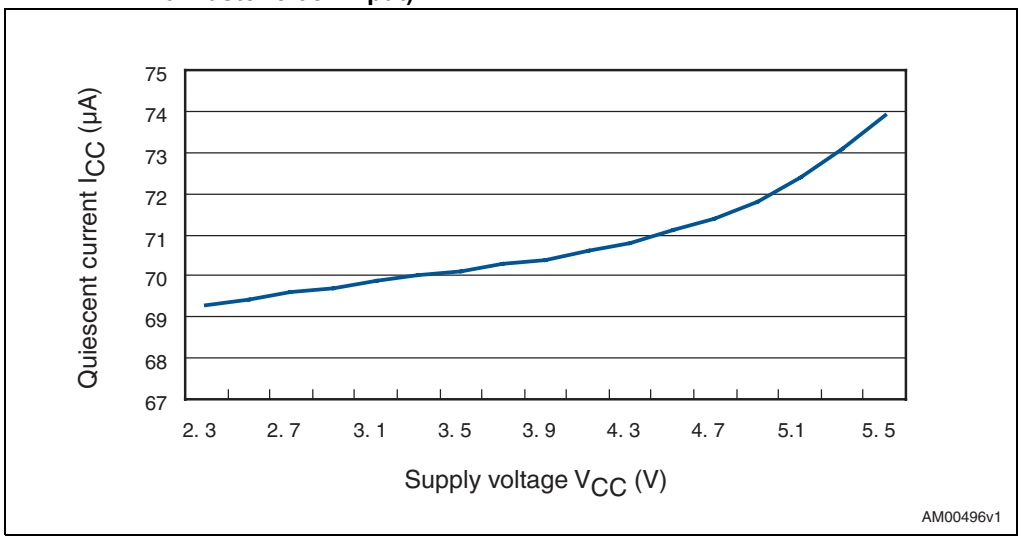


Figure 12. Quiescent current vs. temperature (EN1 = EN2 = EN3 = EN4 = 1, C_{load} = 20 pF, no master clock input)

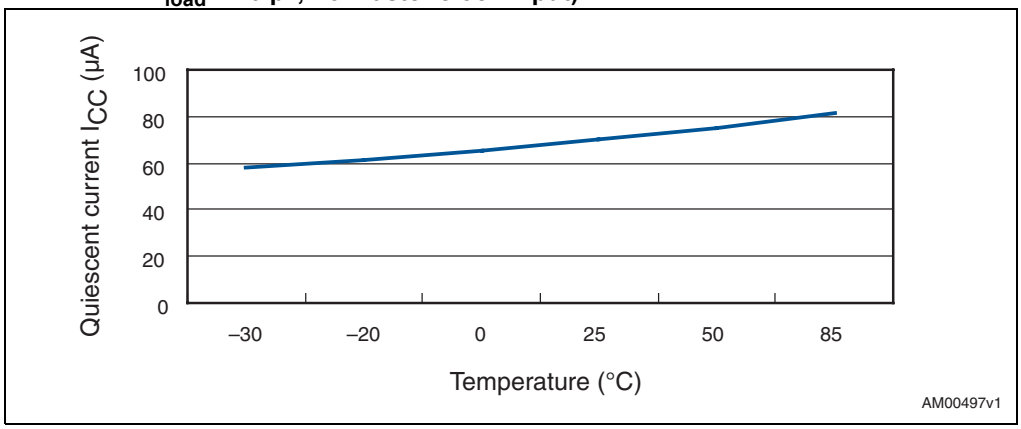


Figure 13. Active current vs. temperature (EN1 = EN2 = EN3 = EN4 = 1, C_{load} = 20 pF, V_{CC} = 3.8 V, f_{MCLK} = 26 MHz)

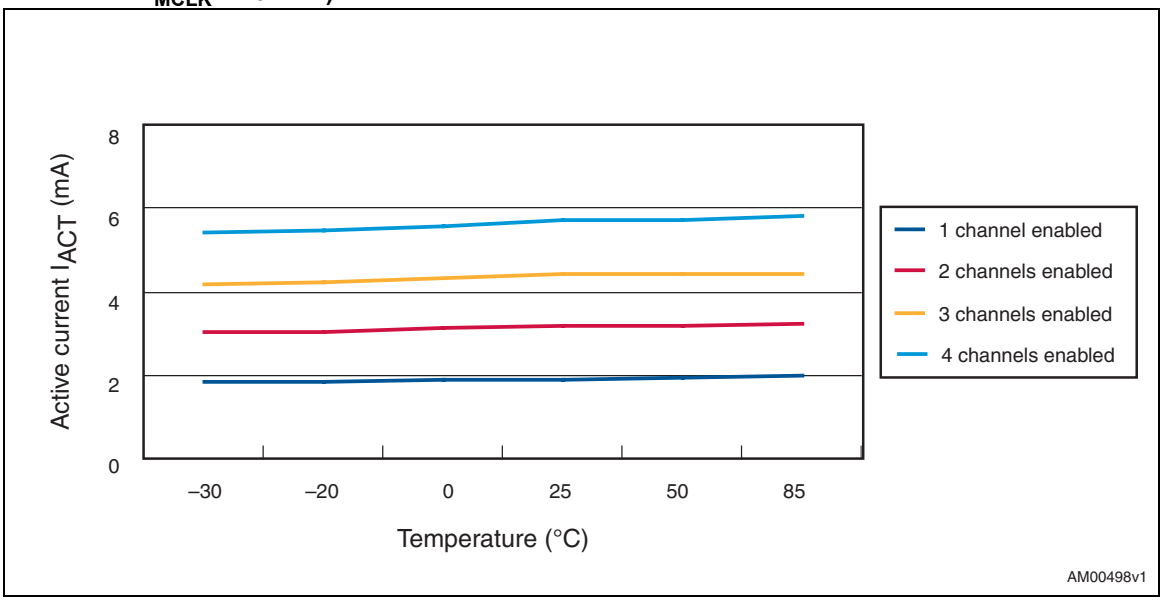


Figure 14. Standby current vs. supply voltage (EN1 = EN2 = EN3 = EN4 = 0, no master clock input)

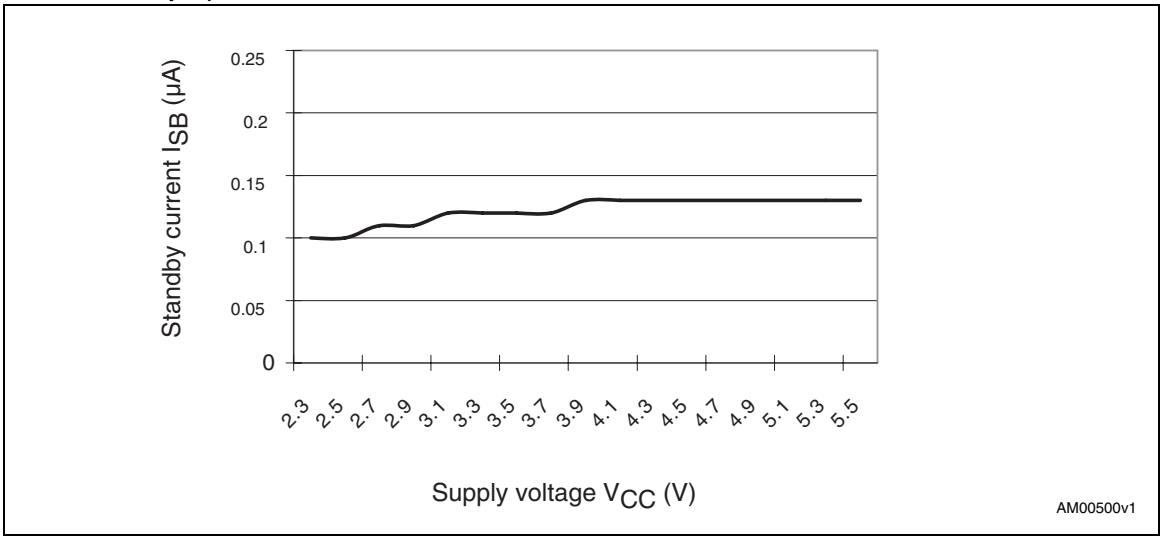


Figure 15. Active current vs. supply voltage (EN1 = EN2 = EN3 = EN4 = 1, f_{MCLK} = 26 MHz, C_{load} = 20 pF)

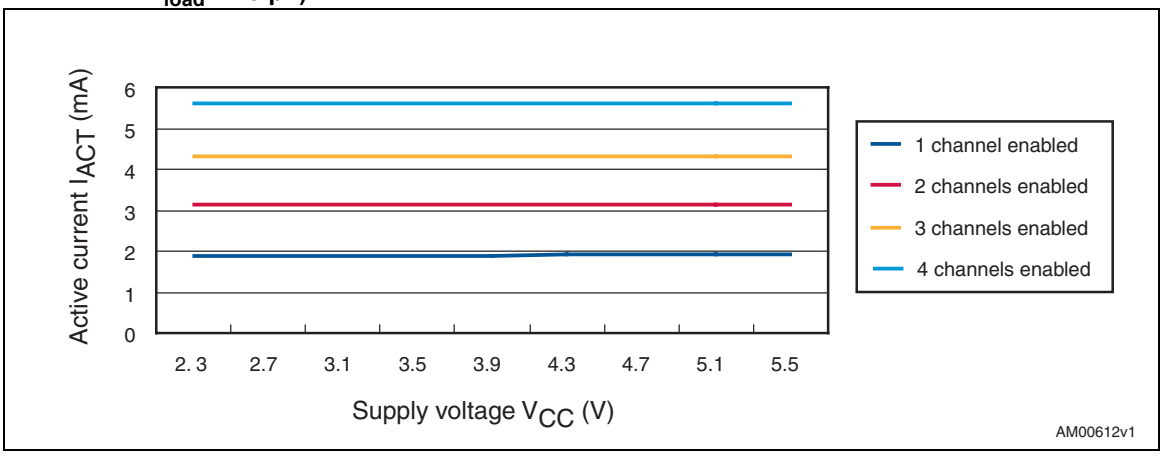


Figure 16. Active current vs. master clock input voltage level (EN1 = EN2 = EN3 = EN4 = 1, f_{MCLK} = 26 MHz, C_{load} = 20 pF)

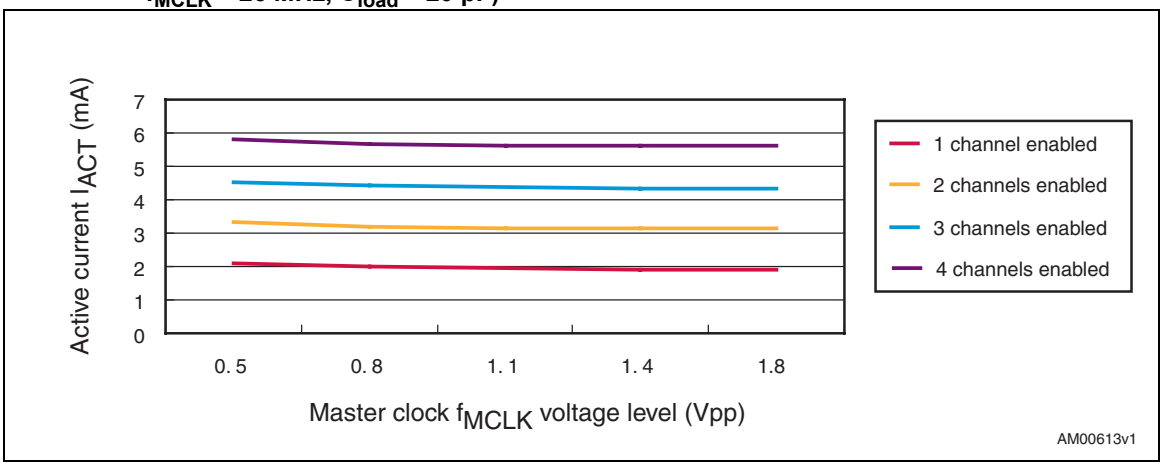


Figure 17. Active current vs. master clock frequency (EN1 = EN2 = EN3 = EN4 = 1, C_{load} = 20 pF)

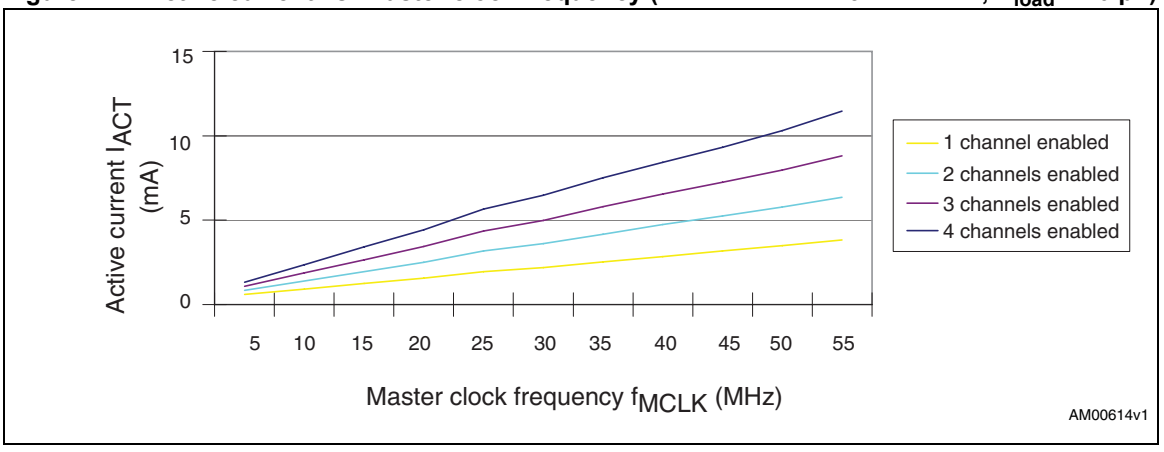


Figure 18. STCD2400 recovery time from standby to active (VTCXO is on)

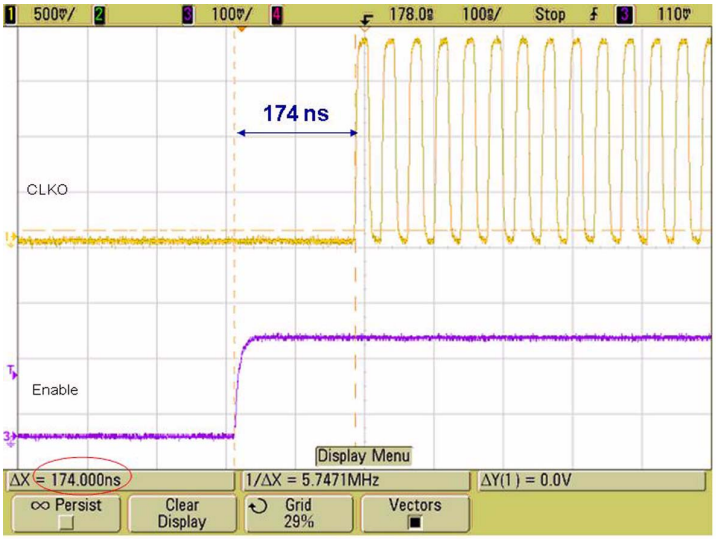


Figure 19. STCD2400 recovery time from off to on (VTCXO first in standby)

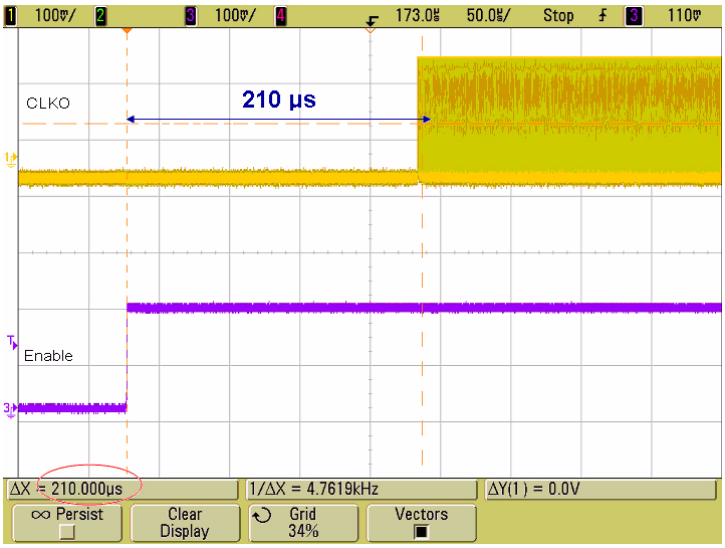


Figure 20. Output clock rise/fall time (C_{load} = 40 pF)

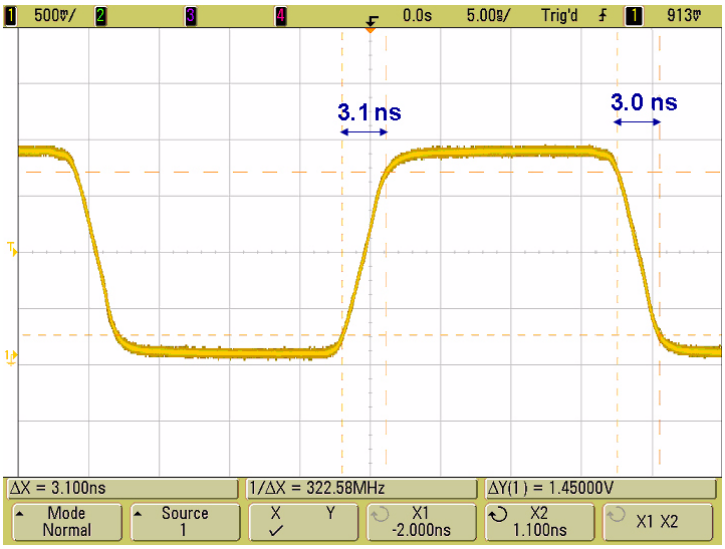


Figure 21. STCD2400 power-up sequence

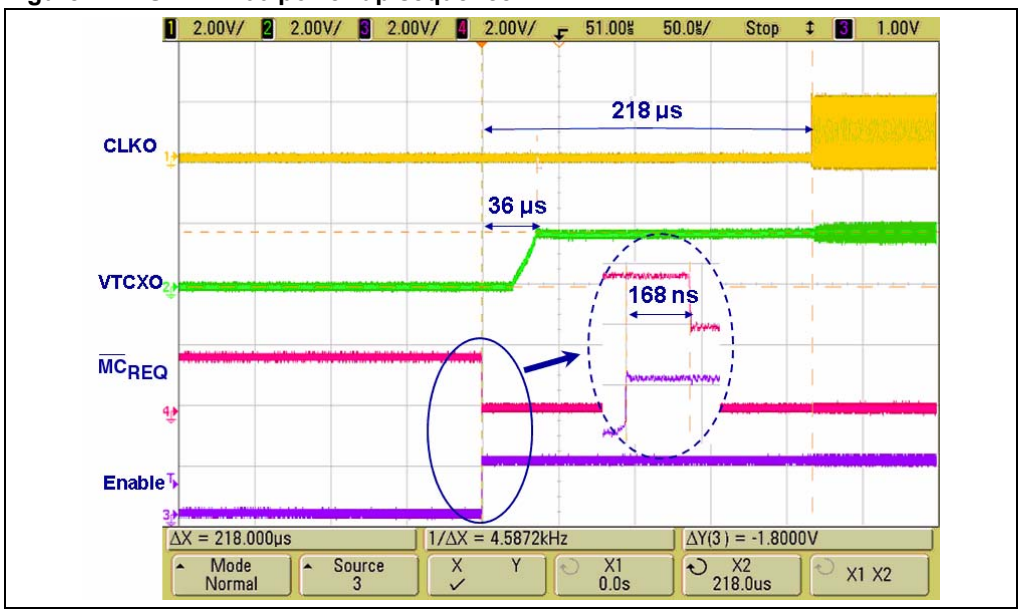


Figure 22. STCD2400 power-down sequence

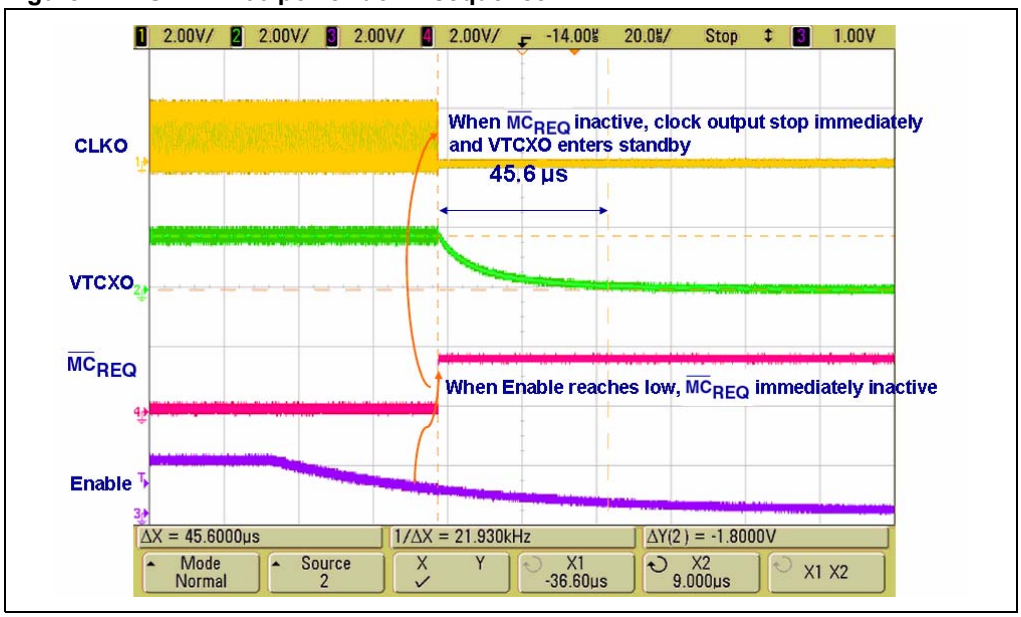


Figure 23. Phase noise input (from the clock source, 26 MHz square wave XO KC2520C26 from Kyocera)

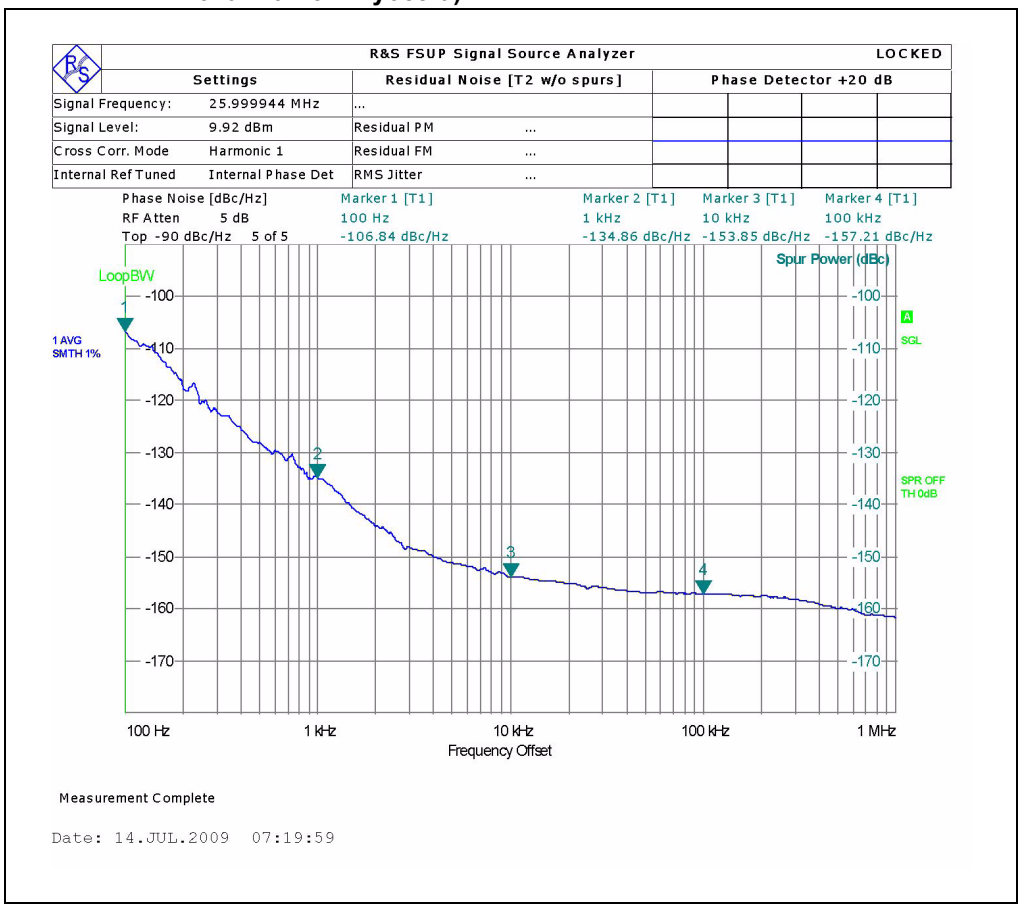
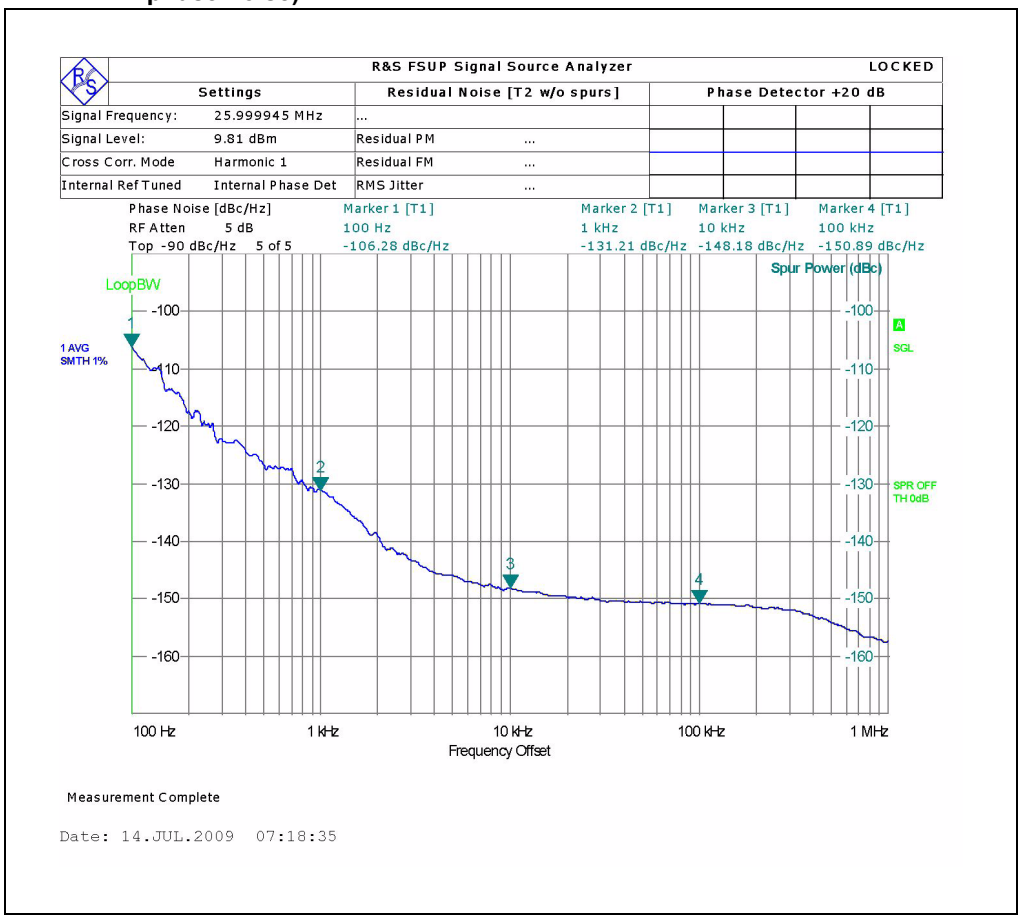


Figure 24. Phase noise output (include the clock source and STCD2400 additive phase noise)



6 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 8. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature (V_{CC} off)	–55 to 150	°C
T_{SLD}(1)	Lead-free bump solder temperature for 10 seconds	260	°C
T_J	Maximum junction temperature	150	°C
V_{CC}	Supply voltage	–0.3 to 6	V
V_{IN}	Input clock voltage	–0.3 to 3.6	V
V_{EN}	Voltage on enable pins	–0.3 to 3.6	V
V_{OPT}	Optional pins voltage	–0.3 to 6	V
$\overline{MC}_{REQ}$	Master clock request	–0.3 to 3.6	V

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.

7 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow are derived from tests performed under the measurement conditions summarized in *Table 9*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 9. Operating and AC measurement conditions

Parameter	Condition	Unit
V_{CC} supply	2.5 to 5.1	V
Input source clock voltage (MCLK)	0 to 1.8	V
Output clock voltage (CLK1-4)	0 to 1.8	V
Device enable voltage (EN1-4)	0 to 1.8	V
Source clock request voltage ($\overline{MC}_{REQ}$)	0 to 1.8	V
Optional pins voltage (OPT1, OPT2)	0 to V_{CC}	V
Ambient operating temperature (T_A)	–20 to +85	°C
Flip-chip thermal resistance (R_{thja})	90	°C/W

Table 10. DC and AC characteristics

Sym.	Parameter	Condition[1]	Min	Typ	Max	Unit
VTCXO (low dropout output)						
V_{CC}	Supply voltage		2.5		5.1	V
V_{TCXO}	Output voltage	I_{LOAD} = 5 mA	1.75	1.8	1.85	V
I_O	Maximum output current				20	mA
V_{OACC}	Total output accuracy[2]		–5%		5%	
I_{CL}	Current limit protection	V_{TCXO} = 0 V		30	90	mA
V_{REG}	Line regulation[3]	I_{LOAD} = 20 mA		0.5	10	mV
I_{REG}	Load regulation[3]	I_{LOAD} = 10 µA to 20 mA		0.4	10	mV
I_{TR}	Load transient[3]	I_{LOAD} = 10 µA to 20 mA I_{TR} = 1 µs		100	110	mV
		I_{LOAD} = 20 mA to 10 µA I_{TR} = 1 µs		100	110	mV

Table 10. DC and AC characteristics (continued)

Sym.	Parameter	Condition(1)	Min	Typ	Max	Unit
PSRR	Power supply rejection ratio(3)(4)	V_{CC} = 2.5 V to 5.1 V, F_{ripple} = 217 Hz, I_{LOAD} = 20 mA	60	67		dB
		V_{CC} = 2.5 V to 5.1 V, F_{ripple} = 1 kHz, I_{LOAD} = 20 mA	40	60		
		V_{CC} = 2.5 V to 5.1 V, F_{ripple} = 1 MHz, I_{LOAD} = 20 mA	40			
		V_{CC} = 2.5 V to 5.1 V, F_{ripple} = 3.25 MHz, I_{LOAD} = 20 mA	40			
e_N	Output noise voltage(3)	I_{LOAD} = 5 mA, 10 Hz to 100 kHz		45		μV_{rms}
t_{ST}	Startup time(3)	V_{TCXO} > 90%, I_{LOAD} = 10 µA to 20 mA		150	400	µs
t_F	Output voltage falling time(3)	V_{TCXO} < 10%, I_{LOAD} = 0		120	400	µs
Clock distribution						
f_{MCLK}	Master clock (from external clock source)	Square wave / sine wave	10	26	52	MHz
	f_{CLK} duty cycle		40	50	60	%
V_{IN}	Input clock voltage level(5)	Square wave	0.8	1.8	VTCXO + 0.2	Vpp
		Sine wave	0.8	1	VTCXO + 0.2	Vpp
V_{OH}	Output high	C_L = 20 pF	VTCXO – 0.05	VTCXO		V
V_{OL}	Output low	C_L = 20 pF			0.05	V
$T_{r/f}$	Rise/fall time(6)	C_L =10 pF~ 40 pF	1	2	5	ns
I_{QC}	Quiescent current(7) (including LDO)	1 channel enabled		80	200	µA
		2 channels enabled		80	200	
		3 channels enabled		80	200	
		4 channels enabled		80	200	
I_{CC}	Active current(8)	1 channel enabled		1.9		mA
		2 channels enabled		3.0		
		3 channels enabled		4.1		
		4 channels enabled		5.2		
I_{SB}	Standby current (including LDO)	All buffers off		0.2	1	µA
R_{IN}	Input impedance			> 100		kΩ

Table 10. DC and AC characteristics (continued)

Sym.	Parameter	Condition[1]	Min	Typ	Max	Unit
C_{IN}	Input capacitance			3	4	pF
I_{OO}	Output to output isolation			45		dB
I_{OI}	Output to input isolation			45		dB
V_{ENH}	Enable voltage high[9]	For EN1-EN4	1.2			V
V_{ENL}	Enable voltage low[9]	For EN1-EN4			0.6	V
V_{OPTH}	OPT pins voltage high	For OPT1 and OPT2	V_{CC} –0.3	V_{CC}		V
V_{OPTL}	OPT pins voltage low	For OPT1 and OPT2		GND	GND+0.3	V
P_N	Additive phase noise[3][10]	at 1 kHz offset		–135		dBc/Hz
		at 10 kHz offset		–145		
		at 100 kHz offset		–150		
t_{JP}	Additive period jitter[3]	rms value		10		ps
t_{JC}	Additive cycle-cycle jitter[3]	rms value		10		ps
t_{RECB}	Buffer recovery time from off to on	STCD2xx0 active		1	10	µs
t_{RECC}	STCD2xx0 recovery time from standby to active (include LDO wakeup time)				500	µs
t_{PD}	Input to output propagation delay[3]	Voltage transfer at 50%		3.5	6	ns
C_L	Capacitive load for each channel			20	40	pF
R_L	Resistive load for each channel		10			kΩ
Z_{OUT}	Output impedance for each channel				50	Ω

1. Valid for ambient operating temperature: T_A = –20 °C to 85 °C; V_{CC} = 2.5 V to 5.1 V; typical T_A = 25 °C; load capacitance = 20 pF, f_{MCLK} = 26 MHz (except where noted).
2. Total accuracy includes line and load regulation, temperature and process condition. It does not include load and line transients.
3. Simulated and determined via design and not 100% tested.
4. Ripple voltage = 0.1 Vpp.
5. Clock input voltage level should not exceed VTCXO voltage.
6. The rise time is measured when clock edge transfers from 10% V_{CC} to 90%V_{CC}. The fall time is measured when clock edge transfers from 90%V_{CC} to 10%V_{CC}. The output rise/fall time is guaranteed for all input slew rates.
7. The quiescent current is measured when the enable pins are active, but with no input master clock signal (f_{MCLK} = 0 Hz).
8. The active current depends on the input master clock Vpp and frequency and the load condition. The typical test condition is 26 MHz with 1.8 Vpp master clock input, C_L = 20 pF.
9. The test condition is V_{ENH} = 1.8 V and V_{ENL} = 0 V. When output enables simultaneously, there is no intentional skew in design between the output clocks.
10. Guaranteed for all input clock slew rates.

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 25. Flip Chip 12-bump, package mechanical outline

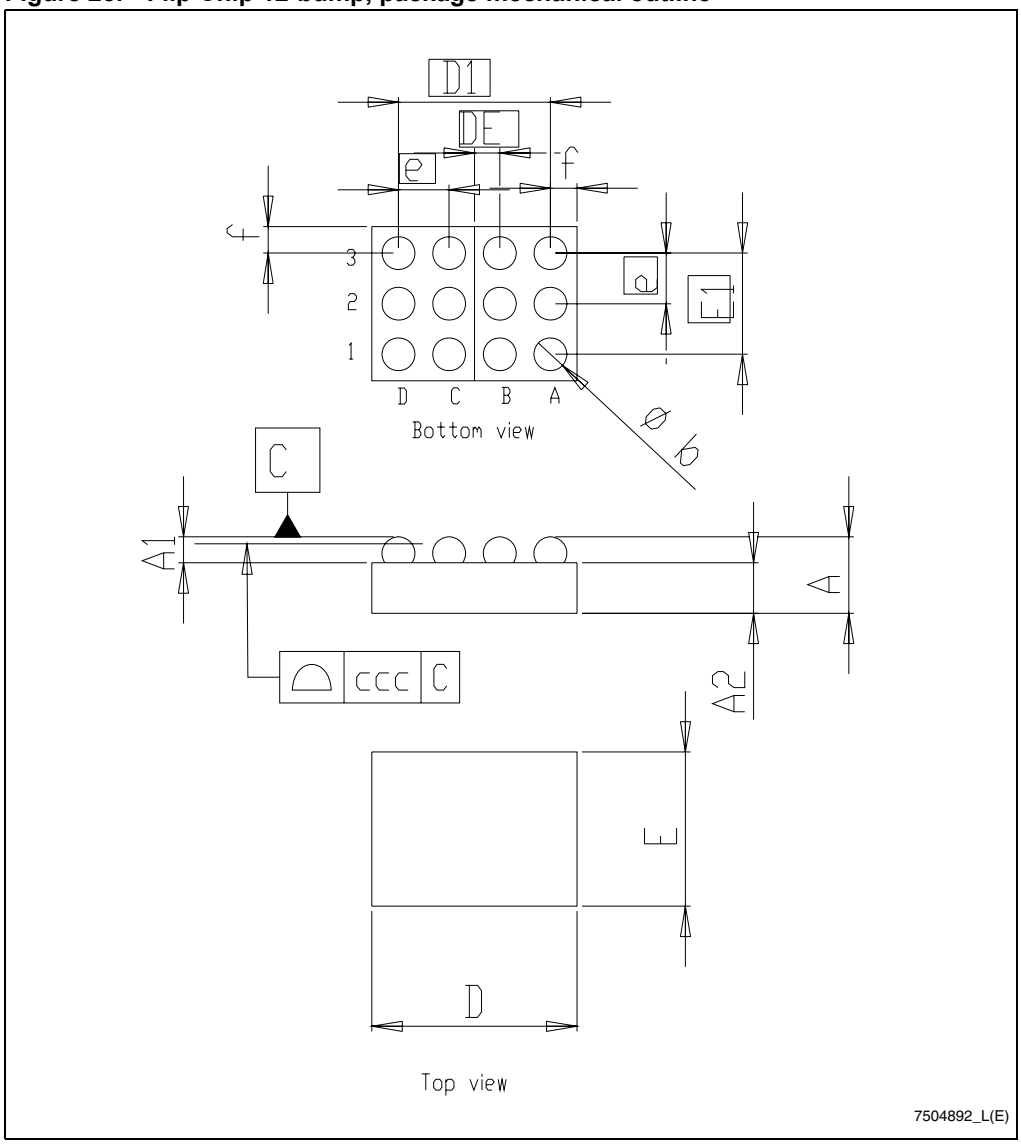


Table 11. Flip Chip 12-bump, package mechanical data

Symbol	mm			in		
	Min	Typ	Max	Min	Typ	Max
A	0.55	0.61	0.66	0.022	0.024	0.026
A1	0.17	0.21	0.24	0.007	0.008	0.009
A2	0.38	0.40	0.42	0.015	0.016	0.017
b	0.22	0.26	0.30	0.008	0.010	0.012
D	1.55	1.60	1.65	0.061	0.063	0.065
D1		1.20			0.047	
E	1.15	1.20	1.25	0.045	0.047	0.049
E1		0.80			0.031	
e	0.36	0.40	0.44	0.014	0.016	0.017
DE	0.18	0.20	0.22	0.007	0.008	0.009
f	0.185	0.195	0.210	0.007	0.008	0.008
ccc		0.05			0.002	

Figure 26. Flip Chip 16-bump, package mechanical outline

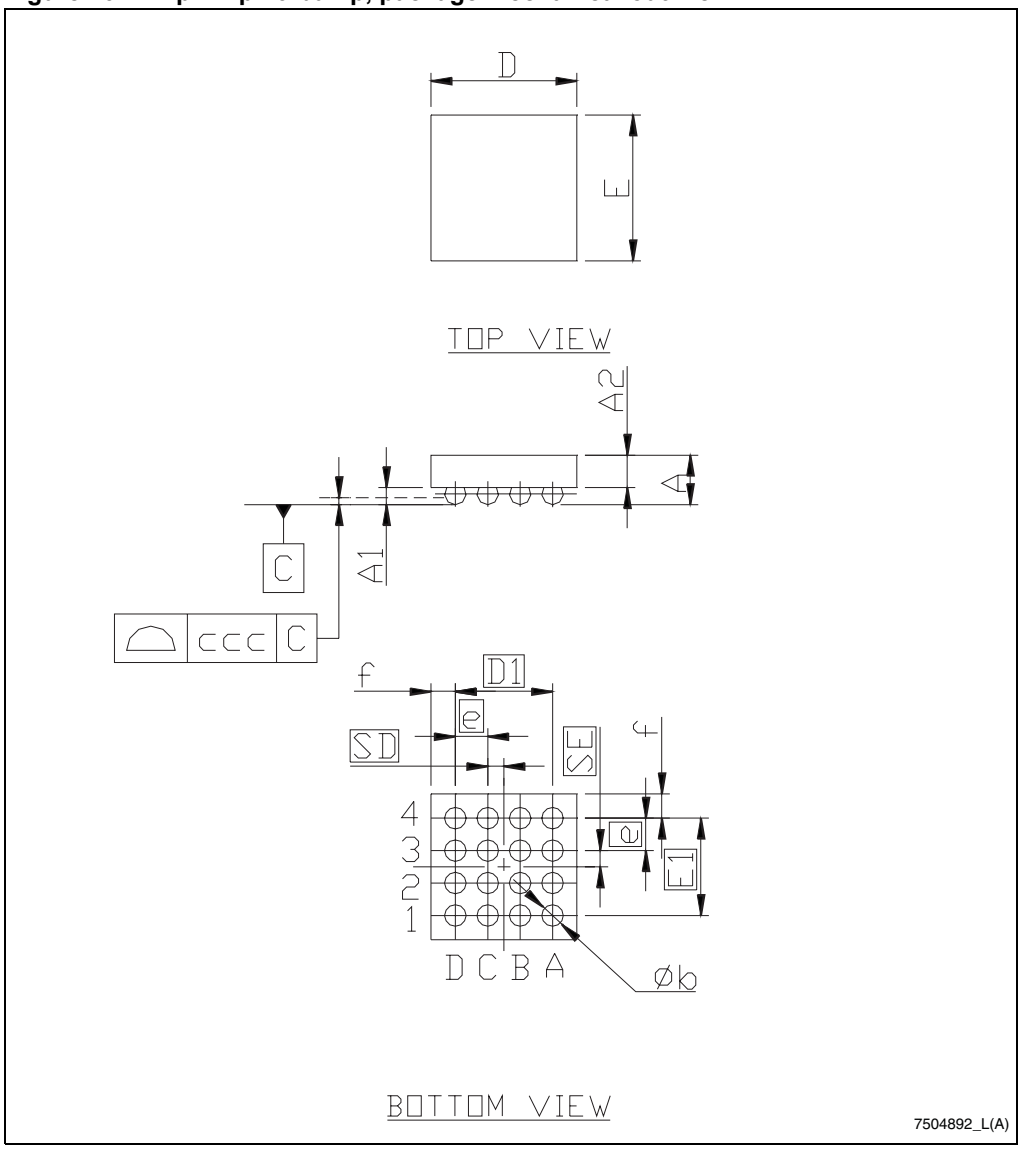


Table 12. Flip Chip 16-bump, package mechanical data

Symbol	mm			in		
	Min	Typ	Max	Min	Typ	Max
A	0.55	0.61	0.66	0.022	0.024	0.026
A1	0.17	0.21	0.24	0.007	0.008	0.009
A2	0.38	0.40	0.42	0.015	0.016	0.017
b	0.22	0.26	0.30	0.008	0.010	0.012
D	1.55	1.60	1.65	0.061	0.063	0.065
D1		1.20			0.047	
E	1.55	1.60	1.65	0.061	0.063	0.065
E1		1.20			0.047	
e	0.36	0.40	0.44	0.014	0.016	0.017
SD	0.18	0.20	0.22	0.007	0.008	0.009
SE	0.18	0.20	0.22	0.007	0.008	0.009
f	0.185	0.195	0.210	0.007	0.008	0.008
ccc		0.05			0.002	

Figure 27. Flip Chip 12-bump tape and reel specifications

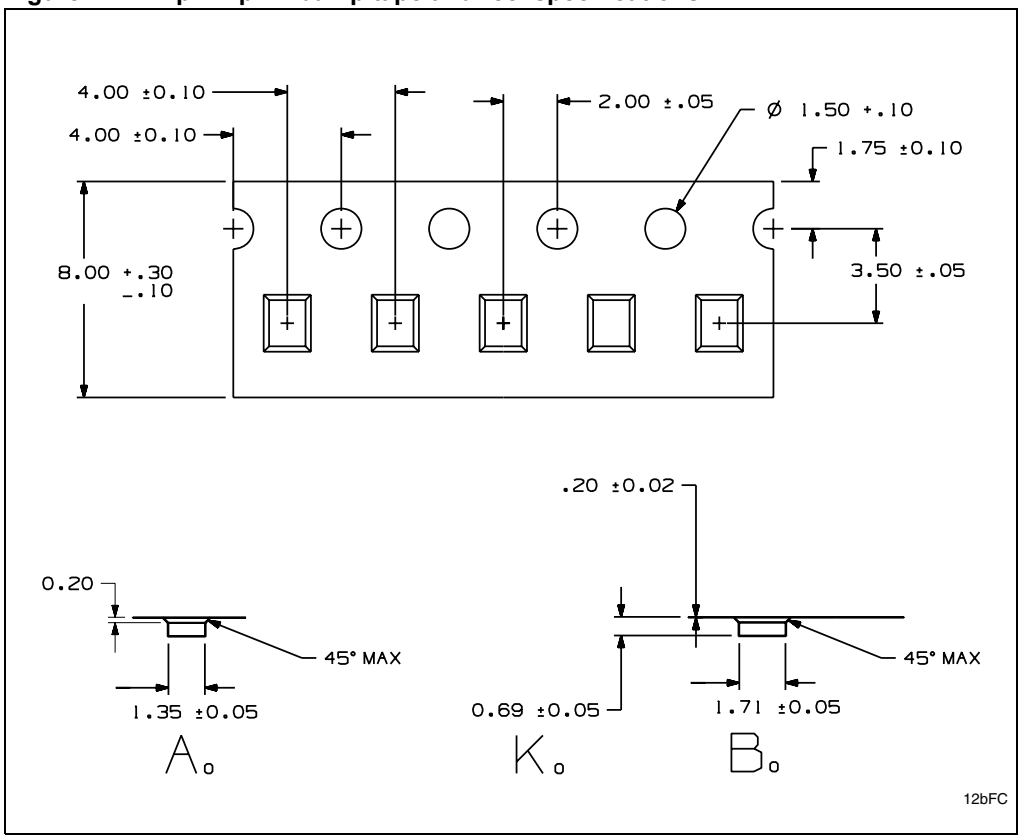
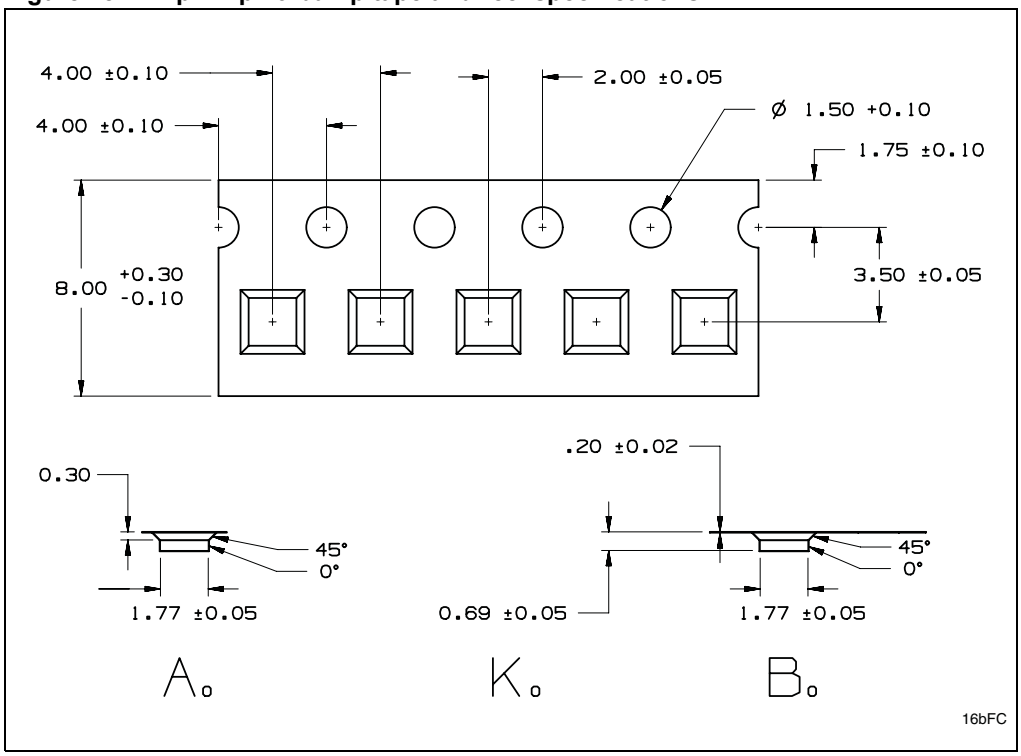


Figure 28. Flip Chip 16-bump tape and reel specifications



9 Part numbering

Table 13. Ordering information scheme

Example: STCD 22 0 0 F3 5 F

Device type

STCD = clock distribution

Channels

22 = 2-channel(1)

23 = 3-channel(1)

24 = 4-channel

Enable polarity

STCD22x0 (user programmable)

0 = OPT1 sets EN1, OPT2 sets EN2

STCD23x0 (factory programmable)

0 = $\overline{EN1}$, $\overline{EN2}$, $\overline{EN3}$

1 = $\overline{EN1}$, $\overline{EN2}$, EN3

2 = EN1, EN2, $\overline{EN3}$

3 = EN1, EN2, EN3

STCD24x0 (user programmable)

0 = OPT1 sets EN1 and EN2, OPT2 sets EN3 and EN4

1 = OPT1 sets EN1, OPT2 sets EN2, EN3, and EN4(1)

Master clock request ($\overline{MC}_{REQ}$)

0 = $\overline{MC}_{REQ}$ active low

Package

F3 = Flip chip, lead-free, pitch = 400 µm, bump = 250 µm

(12-bump for 2- or 3-channel, 16-bump for 4-channel)

Temperature range

5 = –20 °C to +85 °C

Shipping method

F = ECOPACK® package, tape & reel

1. Contact local ST sales office for availability.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

10 Revision history

Table 14. Document revision history

Date	Revision	Changes
26-Aug-2009	1	Initial release.
11-Jan-2010	2	Updated footnote *5* in *Table 10: DC and AC characteristics*.