W83176R-733

W83176G-733

Winbond Dual Bank DDR BUFFER For VIA CHIPSET

Date: Mar/22/2006 Revision: 1.0

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DUAL BANK DDR BUFFER FOR VIA CHIPSET

W83176R-733/W83176G-733 Data Sheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1					All of the versions before 0.50 are for internal use.
2	n.a.	09/09/03	0.5	n.a.	First published preliminary version.
3	3,4,5,8	12/18/03	0.6	n.a.	Correction IC version, correction some description and default value
4		03/22/2006	1.0	1.0	Update on Web and add lead free part
5					
6					
7					
8					
9					
10					

LIFE SUPPORT APPLICATIONS

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DUAL BANK DDR BUFFER FOR VIA CHIPSET

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DUAL BANK DDR BUFFER FOR VIA CHIPSET

1. GENERAL DESCRIPTION

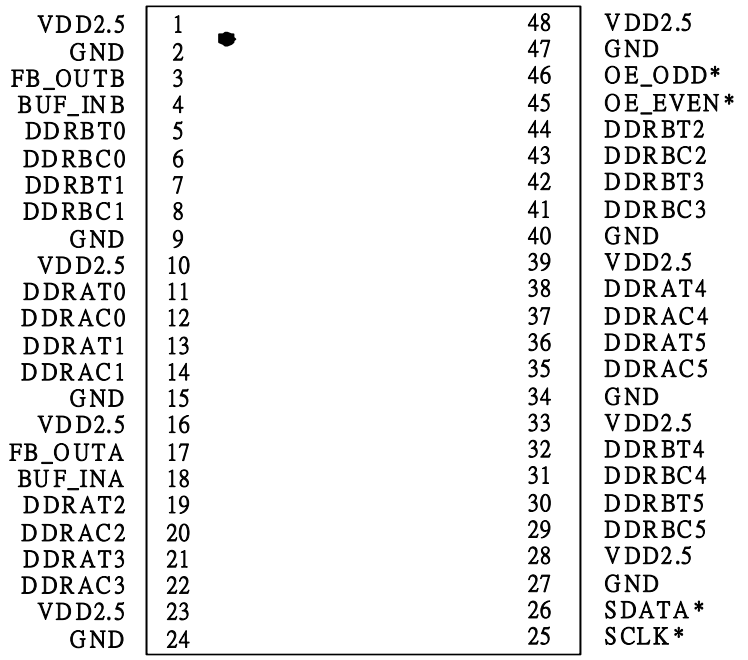
The W83176R-733 is a 2.5V Dual Bank D.D.R. Clock buffer designed for VIA system. W83176R-733 can support 4 D.D.R. DRAM DIMMs.

The W83176R-733 provides I^2C serial bus interface to program the registers to enable or disable each clock outputs. The W83176R-733 accepts a reference clock as its input and runs on 2.5V supply.

2. PRODUCT FEATURES

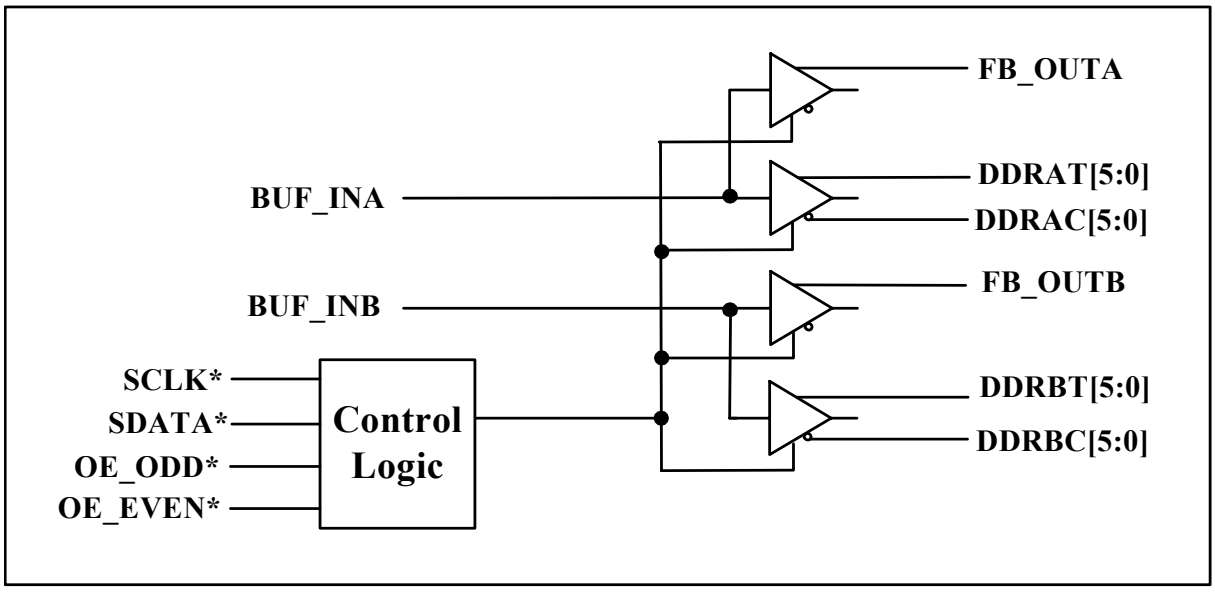
- Low Skew outputs (< 100ps)
- Two Feedback pins for synchronous for each bank.
- Supports up to 4 D.D.R. DIMMs
- Supports PC3200 D.D.R. SDRAM
- I^2C 2-Wire serial interface and supports Byte or Block Date RW
- 48-pin SSOP package

3. PIN CONFIGURATION



*: Internal pull-up resistor 120K to VDD

4. BLOCK DIAGRAM



5. PIN DESCRIPTION

BUFFER TYPE SYMBOL	DESCRIPTION
IN	Input
OUT	Output
I/OD	Bi-directional Pin, Open Drain
*	Internal 120kΩ pull-up

5.1 Clock Function Pins

PIN	PIN NAME	TYPE	DESCRIPTION
18	BUF_INTA	IN	Bank A DDR Buffer True reference clock input.
36,35,38,37,21,22,20,19,14,13,11,12	DDRAT/C [5:0]	OUT	Bank A DDR Buffer clocks of differential pair outputs.
17	FB_OUTA	OUT	Bank A DDR Buffer True Feedback output, dedicated for external feedback.
4	BUF_INTB	IN	Bank B DDR Buffer True reference clock input.
30,29,32,31,42,41,44,43,7,8,5,6	DDRBT/C [5:0]	OUT	Bank B DDR Buffer clocks of differential pair outputs.
3	FB_OUTB	OUT	Bank B DDR Buffer True Feedback output, dedicated for external feedback.

5.2 Control Signal Pins

PIN	PIN NAME	TYPE	DESCRIPTION
26	SDATA *	I/OD	Serial data of I^2C 2-wire control interface Internal pull-up resistor 120K to VDD2.5
25	SCLK *	IN	Serial clock of I^2C 2-wire control interface Internal pull-up resistor 120K to VDD2.5
45	OE_EVEN*	IN	OE_EVEN=1 Enable, OE_EVEN=0 Disable, Even Buffer clock output pairs (DDR0, 2,4), Internal pull-up resistor 120K to VDD2.5
46	OE_ODD*	IN	OE_ODD=1 Enable, OE_ODD=0 Disable, ODD Buffer clock output pairs (DDR1, 3, 5), Internal pull-up resistor 120K to VDD2.5

6. POWER PINS

PIN	PIN NAME	DESCRIPTION
2,9,15,24,27,34,40,47	GND	Ground
1,10,16,23,28,33,39,48	VDD2.5	Power Supply 2.5V

7. I2C CONTROL AND STATUS REGISTERS

7.1 Register 0 ~ Register 5 RESERVED

7.2 Register 6: Output Control (1 = Enable, 0 = Disable) (Default: FFh)

BIT	PIN NO	PWD	DESCRIPTION
7	Reserved	1	Reserved
6	17	1	FB_OUTA output control
5	36,35	1	DDRA_T5/C5 output control
4	38,37	1	DDRA_T4/C4 output control
3	21,22	1	DDRA_T3/C3 output control
2	20,19	1	DDRA_T2/C2 output control
1	13,14	1	DDRA_T1/C1 output control
0	11,12	1	DDRA_T0/C0 output control

7.3 Register 7: Output Control (1 = Enable, 0 = Disable) (Default: FFh)

Bit	Pin No	PWD	Description
7	Reserved	1	Reserved
6	3	1	FB_OUTB output control
5	30,29	1	DDRB_T5/C5 output control
4	32,31	1	DDRB_T4/C4 output control
3	42,41	1	DDRB_T3/C3 output control
2	44,43	1	DDRB_T2/C2 output control
1	7,8	1	DDRB_T1/C1 output control
0	5,6	1	DDRB_T0/C0 output control

7.4 REGISTER 8 ~ Register 17 RESERVED

7.5 Skew step reference Table

SKEW<2:0>/<1:0>	DELAY TIME (PS)
000	0
001	250
010	500
011	750
100	1000
101	1250
110	1500
111	1750

7.6 Register 18: Skew Control (Default: 88h)

BIT	NAME	PWD	DESCRIPTION
7	Reserved	1	Reserved
6	DDRA_TSKEW<2>	0	DDRA True clock outputs with FB_OUTA True clock SKEW control bits
5	DDRA_TSKEW<1>	0	
4	DDRA_TSKEW<0>	0	
3	Reserved	1	Reserved
2	DDRA_CSKEW<2>	0	DDRA Complementary clock outputs with FB_OUTA True clock SKEW control bits
1	DDRA_CSKEW<1>	0	
0	DDRA_CSKEW<0>	0	

7.7 Register 19: Skew Control (Default: 80h)

BIT	NAME	PWD	DESCRIPTION
7	Reserved	1	Reserved
6	DDRB_CSKEW<2>	0	DDRB Complementary clock outputs with FB_OUTB True clock SKEW control bits
5	DDRB_CSKEW<1>	0	
4	DDRB_CSKEW<0>	0	
3	FAOUT_SKEW<1>	0	FB_OUTA, DDRA clock outputs with BUF_INA clock SKEW control bits
2	FAOUT_SKEW<0>	0	
1	FBOUT_SKEW<1>	0	FB_OUTB, DDRB clock outputs with BUF_INB clock SKEW control bits
0	FBOUT_SKEW<0>	0	

7.8 Slew rate reference table

SR<1:0>	STATUS
10/01	Normal (default)
11	Strong
00	Weak

7.9 Register 20: Skew & Slew Rate Control (Default: 8Ah)

BIT	NAME	PWD	DESCRIPTION
7	Reserved	1	Reserved
6	DDRB_TSKEW<2>	0	DDRB True clock outputs with FB_OUTB True clock SKEW control bits
5	DDRB_TSKEW<1>	0	
4	DDRB_TSKEW<0>	0	
3	DDRAT/C0_SR<1>	1	DDRAT/C0 slew rate control bits
2	DDRAT/C0_SR<0>	0	
1	DDRAT/C1_SR<1>	1	DDRAT/C1 slew rate control bits
0	DDRAT/C1_SR<0>	0	

7.10 Register 21: Slew Rate Control (Default: AAh)

BIT	NAME	PWD	DESCRIPTION
7	DDRAT/C2_SR<1>	1	DDRAT/C2 slew rate control bits
6	DDRAT/C2_SR<0>	0	
5	DDRAT/C3_SR<1>	1	DDRAT/C3 slew rate control bits
4	DDRAT/C3_SR<0>	0	
3	DDRAT/C4_SR<1>	1	DDRAT/C4 slew rate control bits
2	DDRAT/C4_SR<0>	0	
1	DDRAT/C5_SR<1>	1	DDRAT/C5 slew rate control bits
0	DDRAT/C5_SR<0>	0	

7.11 Register 22: Slew Rate Control (Default: AAh)

BIT	NAME	PWD	DESCRIPTION
7	DDRBT/C0_SR<1>	1	DDRBT/C0 slew rate control bits
6	DDRBT/C0_SR<0>	0	
5	DDRBT/C1_SR<1>	1	DDRBT/C1 slew rate control bits
4	DDRBT/C1_SR<0>	0	
3	DDRBT/C2_SR<1>	1	DDRBT/C2 slew rate control bits
2	DDRBT/C2_SR<0>	0	
1	DDRBT/C3_SR<1>	1	DDRBT/C3 slew rate control bits
0	DDRBT/C3_SR<0>	0	

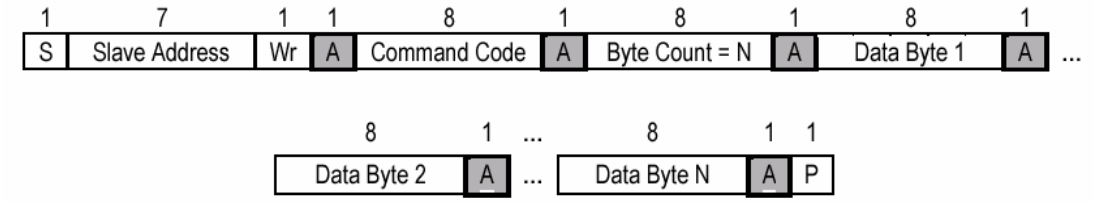
7.12 Register 23: Slew Rate Control (Default: AAh)

BIT	NAME	PWD	DESCRIPTION
7	DDRBT/C4_SR<1>	1	DDRBT/C4 slew rate control bits
6	DDRBT/C4_SR<0>	0	
5	DDRBT/C5_SR<1>	1	DDRBT/C5 slew rate control bits
4	DDRBT/C5_SR<0>	0	
3	FBOUT_SR<1>	1	FB_OUTB slew rate control bits
2	FBOUT_SR<0>	0	
1	FAOUT_SR<1>	1	FB_OUTA slew rate control bits
0	FAOUT_SR<0>	0	

8. ACCESS INTERFACE

The W83176R-733 provides I²C Serial Bus for microprocessor to read/write internal registers. In the W83176R-733 is provided Block Read/Block Write and Byte-Data Read/Write protocol. **The I²C write address is defined at 0xD4. The I²C read address is defined at 0xD5.**

8.1 Block Write Protocol

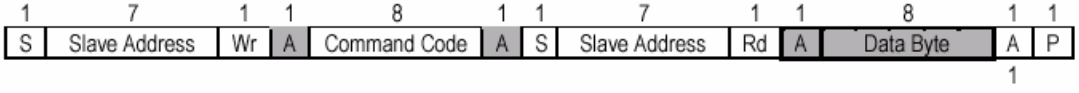


8.2 Block Read Protocol

In block mode, the command code must filled '00h'

8.3 Byte Write Protocol

8.4 Byte Read Protocol



9. SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD2.5).

PARAMETER	RATING
Voltage on any pin with respect to GND	- 0.5 V to + 3.6 V
Storage Temperature	- 65°C to + 150°C
Ambient Temperature	- 55°C to + 125°C
Operating Temperature	0°C to + 70°C
Input ESD protection (Human body model)	2000V

9.2 AC CHARACTERISTICS

VDD2.5 = 2.5V ± 5 %, T_A = 0℃ to +70℃, Test load = 10 pF						
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**TEST CONDITIONS**
Operating clock frequency	F_{IN}	100		200	MHz	
Input Clock Duty Cycle	Dtin	45		55	%	
Dynamic Supply Current	Idd			200	mA	Fin=100 to 200Mhz
Cycle to Cycle Jitter	C-Cjitter			200	ps	Fout=100 to 200Mhz
Output to Output Skew	Tskew			100	ps	Fout=100 to 200Mhz
Output clock Rise time	Tor	650		950	ps	Fout=100 to 200Mhz
Output clock Fall time	Tof	650		950	ps	Fout=100 to 200Mhz
Output clock Duty Cycle	Dtot	45		55	%	Fout=100 to 200Mhz
Output differential-pair crossing voltage	Voc	(Vdd/2) -0.2	Vdd/ 2	(Vdd/2) + 0.2	V	Fout=100 to 200Mhz

9.3 DC CHARACTERISTICS

VDD2.5= 2.5V ± 5 %, T_A = 0℃ to +70℃						
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**TEST CONDITIONS**
SDATA, SCLK Input Low Voltage	SV_{IL}			1.0	V_{dc}	
SDATA, SCLK Input High Voltage	SV_{IH}	2.2			V_{dc}	
BUF_IN Input Voltage Low	V_{IL}			0.4	V_{dc}	Fin=100 to 200Mhz
BUF_IN Input Voltage High	V_{IH}	2.1			V_{dc}	Fin=100 to 200Mhz
Input Pin Capacitance	C_{IN}			5	pF	
Output Pin Capacitance	C_{OUT}			6	pF	
Input Pin Inductance	L_{IN}			7	nH	

10. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83176R-733	48 PIN SSOP	Commercial, 0°C to +70°C
W83176G-733	48 PIN SSOP(Lead free part)	Commercial, 0°C to +70°C

11. HOW TO READ THE TOP MARKING

1st line: Winbond logo and the type number:

Normal:W83176R-733, Lead free part: W83176G-733

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 342 G E D SA

342: packages made in '2003, week 42

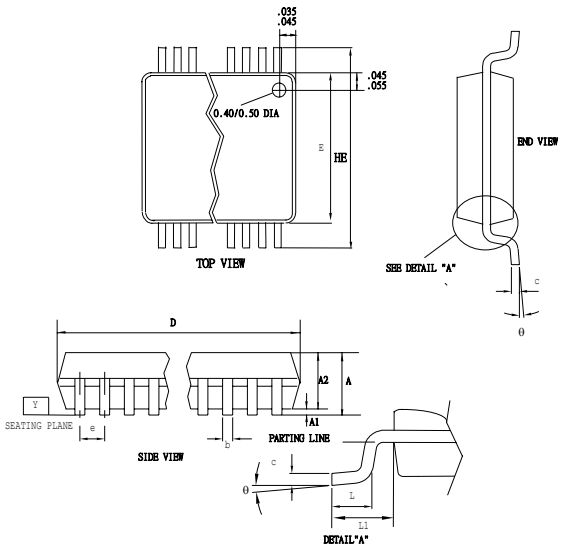
G: assembly house ID; O means OSE, G means GR

A: Internal use code

A: IC revision

SA: Internal use code

12. PACKAGE DRAWING AND DIMENSIONS



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	2.41	2.57	2.79	0.095	0.101	0.110
A1	0.20	0.30	0.41	0.008	0.012	0.016
A2	2.24	2.29	2.34	0.088	0.090	0.092
b	0.20	0.25	0.34	0.008	0.010	0.0135
c	0.13	—	0.25	0.005	—	0.010
D	18.2	18.42	18.54	0.720	0.725	0.730
H_E	10.16	10.31	10.41	0.400	0.406	0.410
E	7.42	7.52	7.59	0.292	0.296	0.299
e	0.51	0.64	0.76	0.020	0.025	0.030
L	0.61	0.81	1.02	0.024	0.032	0.040
L1	—	1.40	—	—	0.055	—
Y	—	—	0.08	—	—	0.003
θ	0	—	8	0	—	8

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