Winbond CLOCK GENERATOR
W83195BR-120/W83195BG-120
For INTEL 915/945 Chipset

Date: Jan./23/2006 Revision: 0.61

W83195BR-120 Data Sheet Revision History

	Pages	Dates	Version	Web Version	Main Contents
1		02/21/2005	0.5	n.a.	All of the versions before 0.50 are for internal use.
2	1-4,6,8, 10-15,18	03/25/2005	0.6	n.a.	Please see red text
3	1,3-8, 10,12,13	01/23/2006	0.61	n.a.	Modify some description and add lead free part number.
4					
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LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

Table of Content-

1. GENERAL DESCRIPTION

The W83195BR-120 is a Clock Synthesizer for Intel 915/945 chipsets. W83195BR-120 provides all clocks required for the high-speed microprocessor and provides step-less frequency programming and 32 different frequencies of CPU, PCI, and PCI-E clocks setting, support SRC 100MHz for SATA and DOT 96MHz clock outputs, all clocks are externally selectable with smooth transitions.

The W83195BR-120 provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and provides -0.5% down type spread spectrum or programmable S.S.T. scale to reduce EMI.

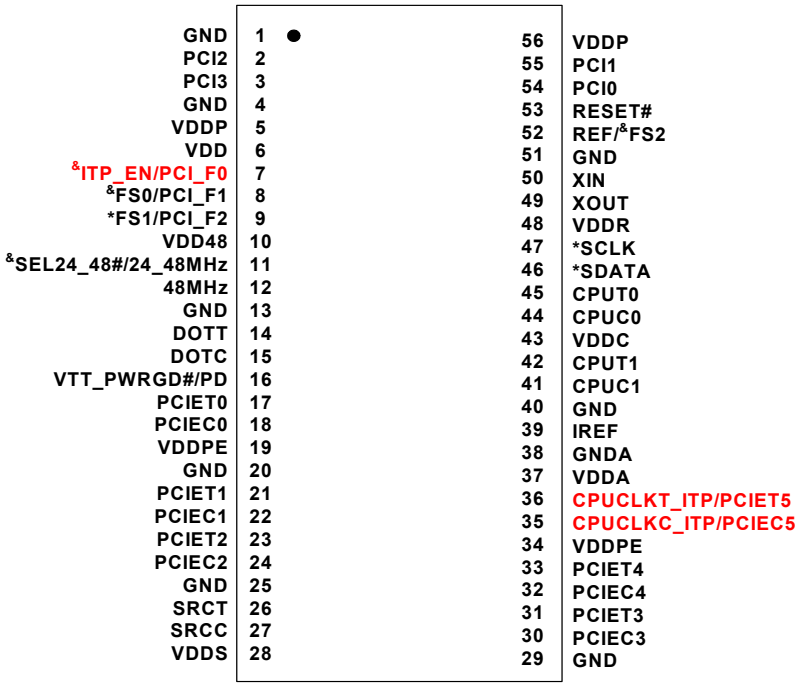
The W83195BR-120 also has watchdog timer and reset output pin to support auto-reset when systems stop functioning caused by improper frequency setting.

The W83195BR-120 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply.

2. PRODUCT FEATURES

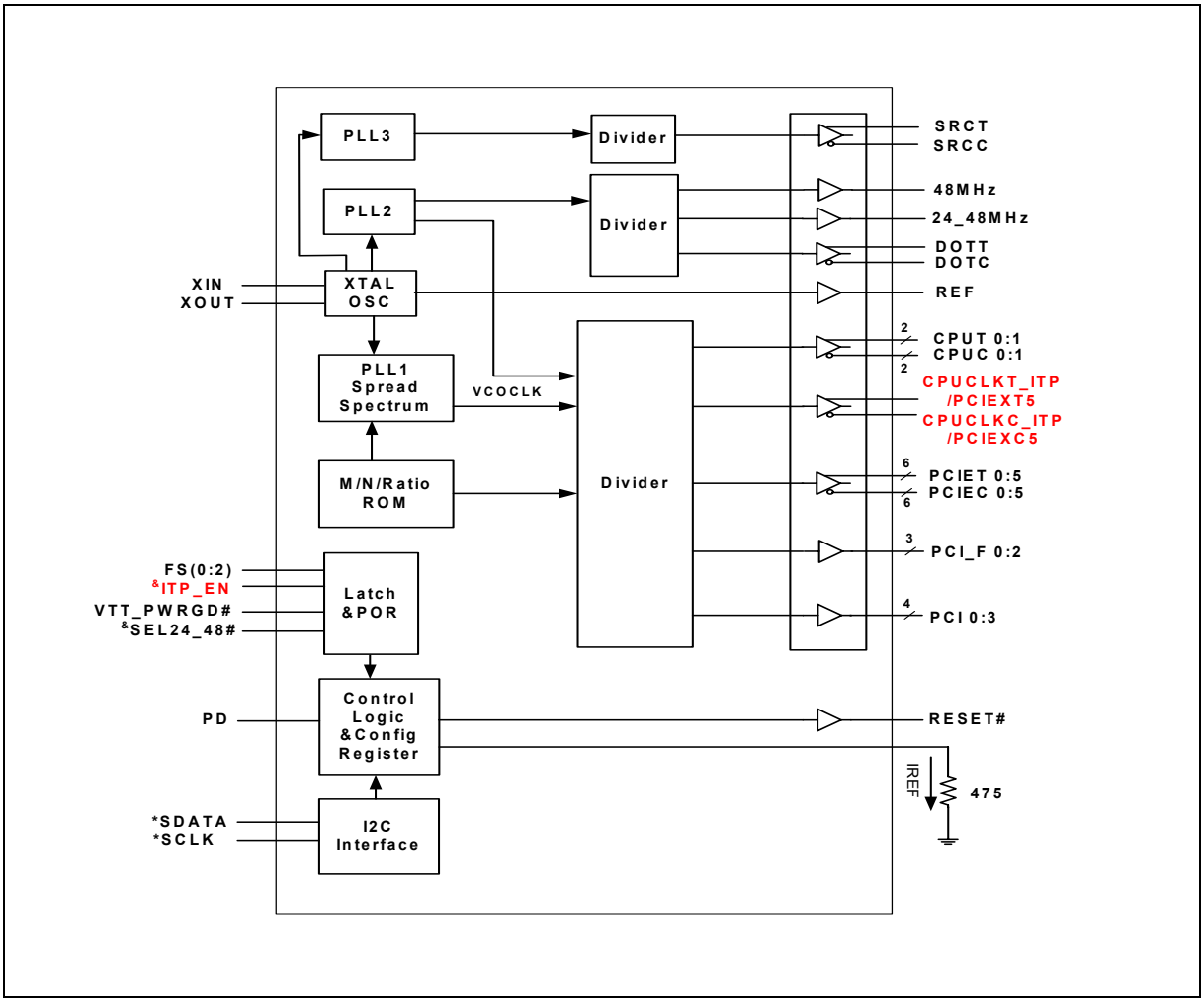
- 2 pair 0.7 V current mode Differential clock outputs for CPU.
- 1 pair 0.7V current mode Differential clock 100MHz outputs for SRC.
- 1 pair 0.7V current mode Differential 96MHz clock outputs for DOT.
- 6 pair 0.7V current mode Differential clock outputs for PCI-Express.
- 1 pair 0.7 V current mode Differential clock outputs select for CPUCLK_ITP.
- 7 PCI synchronous clocks include 3 PCI clock free running.
- 1 24_48Mhz clock output for super I/O.
- 1 48 MHz clock output for USB.
- 1 14.318MHz REF clock outputs.
- Smooth frequency switch with selections from 100 to 400MHz.
- Step-less frequency programming.
- I^2C 2-wire serial interface and support byte read/write and block read/write.
- -0.5% down type spread spectrum in H/W and software select mode.
- Programmable S.S.T. scale to reduce EMI in M/N mode.
- Programmable registers to enable/disable each output and select modes.
- Programmable clock outputs slew rate control and skew control.
- Watch Dog Timer and RESET# output pins.
- 56 pin SSOP package.

3. PIN CONFIGURATION



#: Active low
*: Internal pull up resistor 120K to VDD
&: Internal Pull-down resistor 120K to GND

4. BLOCK DIAGRAM



5. PIN DESCRIPTION

BUFFER TYPE SYMBOL	DESCRIPTION
IN	Input
IN_{tp120k}	Latched input at power up, internal 120kΩ pull up.
IN_{td120k}	Latched input at power up, internal 120kΩ pull down.
OUT	Output
OD	Open Drain
I/OD	Bi-directional Pin, Open Drain.
#	Active Low
*	Internal 120kΩ pull-up
&	Internal 120 kΩ pull-down

5.1 Crystal I/O

PIN	PIN NAME	TYPE	DESCRIPTION
50	XIN	IN	Crystal input with internal loading capacitors (18pF) and feedback resistors.
49	XOUT	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors (18pF).

5.2 CPU, SRC, and PCI_E, PCI, Clock Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
45,44,42,41	CPUT [0:1] CPUC [0:1]	OUT	Low skew (<125ps) 0.7V Current mode differential clock outputs for host frequencies of CPU
17,18,21,22,23,24,31,30,33,32,	PCIET [0:5] PCIEC [0:5]	OUT	Low skew (<125ps) 0.7V Current mode differential clock outputs for PCI-Express
36,35	PCIET/C 5	OUT	0.7V Current mode differential clock outputs for PCI-Express (default), select by ITP_EN pin =0.
	CPUCLKT/C_ITP	OUT	0.7V Current mode differential clock outputs for host frequency, select by ITP_EN pin =1.
7	PCI_F0	OUT	3.3V free running PCI clock output.
	&ITP_EN	IN_{td120k}	Latched input for at initial power up to select CPUCLK_ITP/PCIEX5 output. 1: CPUCLK clock output. 0: PCIEX clock output. This pin has internal 120K pull down.
8	PCI_F1	OUT	3.3V free running PCI clock output.
	&FS0	IN_{td120k}	Latched input for FS0 at initial power up for H/W selecting the output frequency. This pin has internal 120K pull down.
9	PCI_F2	OUT	3.3V free running PCI clock output.
	*FS1	IN_{tp120k}	Latched input for FS1 at initial power up for H/W selecting the output frequency. This pin has internal 120K pull up.
54,55,2,3	PCI [0:3]	OUT	Low skew (< 500ps) 3.3V PCI clock outputs

5.3 Fixed Frequency Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
52	REF	OUT	3.3V REF 14.318 Mhz clock output.
	&FS2	IN_{td120k}	Latched input for FS2 at initial power up for H/W selecting the output frequency, This pin has internal 120K pull down.
11	24_48MHz	OUT	24MHz or 48MHz (default) clock output, In power on reset period, it is a hardware-latched pin, and it can be R/W by I2C control after power on reset period. Select by register 5 bit 7.
	&SEL24_48#	IN_{td120k}	Latched input for 24MHz or 48MHz select pin. This pin has internal 120K pull down default 48MHz. In power on reset period, it is a hardware-latched pin, and it can be R/W by I2C control after power on reset period. Select by register 5 bit 7.
12	48MHz	OUT	48MHz clock output for USB.
26,27	SRCT/C	OUT	• 0.7V current mode 100MHz differential clock outputs for S-ATA
14,15	DOTT/C	OUT	0.7V current mode 96MHz differential clock outputs for DOT

5.4 I2C Control Interface

PIN	PIN NAME	TYPE	DESCRIPTION
46	*SDATA	I/OD	Serial data of I^2C 2-wire control interface with internal pull-up resistor.
47	*SCLK	IN	Serial clock of I^2C 2-wire control interface with internal pull-up resistor

5.5 Power Management Pins

PIN	PIN NAME	TYPE	DESCRIPTION
39	IREF	OUT	Deciding the reference current for the differential pairs. The pin was connected to the precision resistor tied to ground to decide the appropriate current; 475 ohm is the standard value.
53	RESET#	OD	250mS low level system reset signal when Watchdog Timer times out. Application circuit must add external pull high.
16	VTT_PWRGD#	IN	Power good Latched input signal comes from ACPI with low active. This 3.3V input is level sensitive strobe used to determine FS [2:0] input are valid and is ready to sample. This pin is low active.
	PD	IN_{td120k}	High active input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal oscillator are stopped. This pin has internal 120KΩ pull down

5.6 Power Pins

PIN	PIN NAME	TYPE	DESCRIPTION
37	VDDA	PWR	3.3V power supply for PLL core.
5,56	VDDP	PWR	3.3V power supply for PCI.
6	VDD	PWR	3.3V power supply
19,34	VDDPE	PWR	3.3V power supply for PCI express pair.
28	VDDS	PWR	3.3V power supply for SRC pair.
10	VDD48	PWR	3.3V power supply for 48MHz.
43	VDDC	PWR	3.3V power supply for CPU.
48	VDDR	PWR	3.3V power supply for REF.
38	GNDA	PWR	Ground pin for PLL core.
1,4,13,20,25, 29,40,51	GND	PWR	Ground pin

6. FREQUENCY SELECTION BY HARDWARE OR SOFTWARE

This frequency table is used at power on latched FS [2:0] value or software programming at SSEL [4:0] (Register 0 bit 7 ~ 3). If FS [3:0] no any external circuit to modify power on status the Gray shading is Hardware default frequency.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	CPU (MHZ)	PCIE (MHZ)	SRC (MHZ)	PCI (MHZ)
FS4	FS3	FS2	FS1	FS0				
0	0	0	0	0	266.66	100.00	100.00	33.33
0	0	0	0	1	133.33	100.00	100.00	33.33
0	0	0	1	0	200.00	100.00	100.00	33.33
0	0	0	1	1	166.66	111.11	100.00	33.33
0	0	1	0	0	333.33	111.11	100.00	33.33
0	0	1	0	1	100.00	100.00	100.00	33.33
0	0	1	1	0	400.00	100.00	100.00	33.33
0	0	1	1	1	200.00	100.00	100.00	33.33
0	1	0	0	0	266.66	133.33	100.00	33.33
0	1	0	0	1	133.33	133.33	100.00	33.33
0	1	0	1	0	200.00	133.33	100.00	33.33
0	1	0	1	1	166.66	111.11	100.00	33.33
0	1	1	0	0	333.33	111.11	100.00	33.33
0	1	1	0	1	100.00	133.33	100.00	33.33
0	1	1	1	0	400.00	133.33	100.00	33.33
0	1	1	1	1	200.00	100.00	100.00	33.33
1	0	0	0	0	269.33	101.00	100.00	33.67
1	0	0	0	1	134.66	101.00	100.00	33.67
1	0	0	1	0	202.00	101.00	100.00	33.67
1	0	0	1	1	168.33	112.22	100.00	33.67
1	0	1	0	0	274.66	103.00	100.00	34.33
1	0	1	0	1	137.33	103.00	100.00	34.33
1	0	1	1	0	206.00	103.00	100.00	34.33
1	0	1	1	1	171.66	114.44	100.00	34.33
1	1	0	0	0	279.99	105.00	100.00	35.00
1	1	0	0	1	140.00	105.00	100.00	35.00
1	1	0	1	0	210.00	105.00	100.00	35.00
1	1	0	1	1	174.99	116.66	100.00	35.00
1	1	1	0	0	287.99	108.00	100.00	36.00
1	1	1	0	1	144.00	108.00	100.00	36.00
1	1	1	1	0	216.00	108.00	100.00	36.00
1	1	1	1	1	179.99	120.00	100.00	36.00

7. I2C CONTROL AND STATUS REGISTERS

PWD: Power on default value

7.1 Regisbit 0: Frequency Select (Default: 10h)

BIT	NAME	PWD	DESCRIPTION
7	SSEL [4]	0	Frequency selection by software via I^2C
6	SSEL [3]	0	
5	SSEL [2]	0	
4	SSEL [1]	1	
3	SSEL [0]	0	
2	EN_SSEL	0	Enable software table selection FS [4:0]. 0 = Hardware table setting. 1 = Software table setting through Bit 7~3.
1	EN_SPSP	0	Enable spread spectrum mode at clock outputs 0 = Spread Spectrum mode disable 1 = Spread Spectrum mode enable
0	EN_SAFE_FREQ	0	After watchdog timeout 0 = Reload the hardware FS [2:0] latched pins setting. 1 = Reload the frequency table selection as defined in Reg-5 Bit 4~0.

7.2 Register 1: CPU Clock Control (1 = Enable, 0 = Disable) (Default: E2h)

BIT	PIN NO	PWD	DESCRIPTION
7	36,35	1	CPUCLK_ITP/PCIEX5 output control
6	42,41	1	CPUT1 / C1 output control
5	45,44	1	CPUT0 / C0 output control
4	-	0	Reserved (Read only).
3	-	0	Reserved (Read only).
2	-	X	Power on latched value of FS2 pin, Default: 0 (Read only).
1	-	X	Power on latched value of FS1 pin, Default: 1 (Read only).
0	-	X	Power on latched value of FS0 pin, Default: 0 (Read only).

7.3 Register 2: PCI Clock Control (1 = Enable, 0 = Disable) (Default: FFh)

BIT	PIN NO	PWD	DESCRIPTION
7	9	1	PCI_F2 output control
6	8	1	PCI_F1 output control
5	7	1	PCI_F0 output control
4	Reserved	1	Reserved
3	Reserved	1	Reserved
2	Reserved	1	Reserved
1	2,3	1	PCI2, PCI3 output control 1= PCI2 and PCI3 output clock are enabled simultaneously 0= PCI2 and PCI3 output clock are disable simultaneously
0	Reserved	1	Reserved

7.4 Register 3: PCI Clock Control (1 = Enable, 0 = Disable) (Default: FFh)

BIT	PIN NO	PWD	DESCRIPTION
7	55,54	1	PCI1, PCI0 output control. 1= PCI1 and PCI0 output clock are enabled simultaneously 0= PCI1 and PCI0 output clock are stopped simultaneously
6	Reserved	1	Reserved
5	Reserved	1	Reserved
4	Reserved	1	Reserved
3	Reserved	1	Reserved
2	Reserved	1	Reserved
1	Reserved	1	Reserved
0	Reserved	1	Reserved

7.5 Register 4: 24_48MHz, 48MHz, REF Control (1 = Enable, 0 = Disable) (Default: FFh)

BIT	PIN NO	PWD	DESCRIPTION
7	11	1	24_48MHz output control
6	14,15	1	DOT_T/C output control
5	12	1	48MHz output control
4	Reserved	1	Reserved
3	Reserved	1	Reserved
2	52	1	REF output control
1	Reserved	1	Reserved
0	Reserved	1	Reserved

7.6 Register 5: Watchdog Control (Default: 02h)

BIT	NAME	PWD	DESCRIPTION
7	SEL24_48	X	24 / 48 MHz output selection, 1: 24 MHz, 0: 48 MHz (Default). Default value follow hardware trapping data on SEL24_48# pin.
6	EN_WD	0	Program this bit => 1: Enable Watchdog Timer feature. 0: Disable Watchdog Timer feature. Enable WD sequence => Program this bit to 1 firstly, then program the Reg-20 to start the counting Read-back this bit => During timer count down, reading this bit returns 1. If count to zero, reading this bit returns 0.
5	WD_TIMEOUT	0	Read only. Timeout Flag. 1: Watchdog has ever started and counts to zero. 0: Watchdog is restarted and counting.
4	SAF_FREQ [4]	0	When Watchdog Timer times out and EN_SAFE_FREQ=1, these bits will be reloaded to Reg-0 bit 7~3 to select the clock frequencies.
3	SAF_FREQ [3]	0	
2	SAF_FREQ [2]	0	
1	SAF_FREQ [1]	1	
0	SAF_FREQ [0]	0	

7.7 Register 6: PCIE Control (1 = Enable, 0 = Disable) (Default: FEh)

BIT	NAME	PWD	DESCRIPTION
7	SRCEN	1	SRCCLKT/C output control
6	Reserved	1	Reserved
5	PCIEEN<4>	1	PCIET4/C4 output control
4	PCIEEN<3>	1	PCIET3/C3 output control
3	PCIEEN<2>	1	PCIET2/C2 output control
2	PCIEEN<1>	1	PCIET1/C1 output control
1	PCIEEN<0>	1	PCIET0/C0 output control
0	Reserved	0	Reserved

7.8 Register 7: Winbond Chip ID (Default: 22h) (Read Only)

BIT	NAME	PWD	DESCRIPTION
7	CHPI_ID [7]	0	Winbond Chip ID. W83195BR-120
6	CHPI_ID [6]	0	Winbond Chip ID.
5	CHPI_ID [5]	1	Winbond Chip ID.
4	CHPI_ID [4]	0	Winbond Chip ID.
3	CHPI_ID [3]	0	Winbond Chip ID.
2	CHPI_ID [2]	0	Winbond Chip ID.
1	CHPI_ID [1]	1	Winbond Chip ID.
0	CHPI_ID [0]	0	Winbond Chip ID.

7.9 Register 8: M/N Program (Default: 90h)

BIT	NAME	PWD	DESCRIPTION
7	N_DIV [8]	1	Programmable N divisor value. Bit 7 ~0 are defined in the Register 9.
6	N_DIV [9]	0	Programmable N divisor value. Bit 7 ~0 are defined in the Register 9.
5	M_DIV [5]	0	Programmable M divisor value.
4	M_DIV [4]	1	
3	M_DIV [3]	0	
2	M_DIV [2]	0	
1	M_DIV [1]	0	
0	M_DIV [0]	0	

7.10 Register 9: M/N Program Register (Default: BBh)

BIT	NAME	PWD	DESCRIPTION
7	N_DIV [7]	1	Programmable N divisor value bit 7 ~0. The bit 8 is defined in Register 8.
6	N_DIV [6]	0	
5	N_DIV [5]	1	
4	N_DIV [4]	1	
3	N_DIV [3]	1	
2	N_DIV [2]	0	
1	N_DIV [1]	1	
0	N_DIV [0]	1	

7.11 Register 10: Reserved (Default: 3Bh)

BIT	NAME	PWD	DESCRIPTION
7	SRC_SPSPEN	0	Enable SRCLOOP spread spectrum feature 1: Enable, 0: Disable
6	N3VAL<6>	0	Programmable N3 divisor bit 6 ~0 for programmable
5	N3VAL<5>	1	
4	N3VAL<4>	1	
3	N3VAL<3>	1	
2	N3VAL<2>	0	
1	N3VAL<1>	1	
0	N3VAL<0>	1	

7.12 Register 11: Spread Spectrum Programming (Default: 0Eh)

BIT	NAME	PWD	DESCRIPTION
7	SP_UP [3]	0	Spread Spectrum Up Counter bit 3 ~ bit 0.
6	SP_UP [2]	0	
5	SP_UP [1]	0	
4	SP_UP [0]	0	
3	SP_DOWN [3]	1	Spread Spectrum Down Counter bit 3 ~ bit 0 2's complement representation. Ex: 1 -> 1111; 2 -> 1110; 7 -> 1001; 8 -> 1000
2	SP_DOWN [2]	1	
1	SP_DOWN [1]	1	
0	SP_DOWN [0]	0	

7.13 Register 12: Divisor Control (Default: 08h)

BIT	NAME	PWD	DESCRIPTION
7	Reserved	0	Reserved
6	KVAL6	X	Define the PCI divider ratio Table-2 integrate the all divider configuration
5	KVAL5	X	
4	KVAL4	X	Define the PCIE divider ratio Refer to Table-2
3	KVAL3	X	
2	KVAL2	X	Define the CPU divider ratio Refer to Table-2
1	KVAL1	X	
0	KVAL0	X	

Table-2 PCI, PCIE, CPU divider ratio selection Table

LSB		PCI		PCIE		CPU			
		BIT5		BIT3		BIT1, 0			
MSB		0	1	0	1	00	01	10	11
Bit2/ Bit4/ Bit6	0	Div12	Div16	Div3	Div4	Div2	Div3	Div4	Div6
	1	Div20	Div24	Div8	Div6	Div8	Div8	Div8	Div8

7.14 Register 13: Step-less Enable Control (Default: 0Ah)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	EN_MN_PROG	0	0: using frequency table 1: using M/N register to synthesize clock frequency The equation is **VCO =14.318MHz*(N+4)/ M**. Once the watchdog timer times out, the bit will be cleared. Then the frequency will be decided by hardware strapping FS<2:0> or frequency select bits SAF_FREQ [4:0] when EN_SAFE_FREQ (Reg0 - bit 0) is set.	R/W
6	N<10>	0	Programmable N divisor bit 10.	R/W
5	Reserved	0	Reserved	R/W
4	Reserved	0	Reserved	R/W
3	IVAL<3>	1	Charge pump current selection	R/W
2	IVAL<2>	0		R/W
1	IVAL<1>	1		R/W
0	IVAL<0>	0		R/W

7.15 Register 14: Control (Default: 10h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	DRI_CONT	0	CPUT / SRCT / PCIE_T / DOT_T output state in during POWER DOWN assertion. 1: Driven (2*Iref), 0: Tristate (Floating) CPUT / SRCT / PCIE_T / DOT_T output state in during STOP Mode assertion. 1: Driven (6*Iref), 0: Tristate (Floating) Complementary parts always tri-state (floating) in power down or stop mode.	R/W
6	Reserved	0	Reserved	R/W
5	SPCNT [5]	0	Spread Spectrum Programmable time, the resolution is 280ns. Default period is 11.8us	R/W
4	SPCNT [4]	1		R/W
3	SPCNT [3]	0		R/W
2	SPCNT [2]	0		R/W
1	SPCNT [1]	0		R/W
0	SPCNT [0]	0		R/W

7.16 Register 15: SST Control (Default: ECh)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	INV_CPU	1	Invert the CPU phase, 1: Default, 0: Inverse	R/W
6	Reserved	1	Reserved	R/W
5	SPSP_TYPE	1	Spread spectrum implementation method 1 : Pendulum type 0 : Original	R/W
4	Reserved	0	Reserved	R/W
3	Reserved	1	Reserved	R/W
2	Reserved	1	Reserved	R/W
1	Reserved	0	Reserved	R/W
0	Reserved	0	Reserved	R/W

7.17 Register 16: Skew Control (Default: E4h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	INV_PCIE	1	Invert the PCIE phase, 1: Default, 0: Inverse	R/W
6	INV_PCI	1	Invert the PCI phase, 1: Default, 0: Inverse	R/W
5	CSKEW [2]	1	CPU1 to CPU0 skew control, Skew resolution is 300ps The decision of skew direction is same as CSKEW<2:0> setting	R/W
4	CSKEW [1]	0		R/W
3	CSKEW [0]	0		R/W
2	PSKEW [2]	1	CPU1 to PCI skew control, Skew resolution is 300ps The decision of skew direction is same as PSKEW [2:0] setting	R/W
1	PSKEW [1]	0		R/W
0	PSKEW [0]	0		R/W

7.18 Note: The skew rate control select bit fit value Please felloe below table

SKEW bit[2:0]	000	001	010	011	100	101	110	111
Unit	-4	-3	-2	-1	0	1	2	3

Note: Each unit means 300ps

Note: skew bits only for Winbond internal and BOIS program use; the release version please reserved these bits.

7.19 Register 17: Slew rate Control (Default: 00h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	ITP_EN	X	CPUCLK_ITP/PCIEX5 output selection, 1: CPUCLK_ITP, 0: PCIEX5 (Default). Default value follow hardware trapping data on ITP_EN/PCICLK_F0 pin.	R/W
6	INV_48MHz	0	Invert the 48MHz phase, 0: In phase with 24_48MHz 1: 180 degrees out of phase	R/W
5	PCI_F0_S2	0	PCI_F0 slew rate control	R/W
4	PCI_F0_S1	0	11 : Strong , 00 : Weak , 10/01 : Normal	R/W
3	Reserved	0	Reserved	R/W
2	Reserved	0	Reserved	R/W
1	Reserved	0	Reserved	R/W
0	Reserved	0	Reserved	R/W

7.20 Register 18: Reserved (Default: 00h)

7.21 Register 19: Skew Control (Default: DAh)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	Reserved	1	Reserved	R/W
6	Reserved	1	Reserved	R/W
5	PCIESKEW<2>	0	CPU1 to PCIE skew control	R/W
4	PCIESKEW<1>	1	Skew resolution is 300ps	R/W
3	PCIESKEW<0>	1	The decision of skew direction is same as PCIESKEW<2:0> setting	R/W
2	Reserved	0	Reserved	R/W
1	Reserved	1	Reserved	R/W
0	Reserved	0	Reserved	R/W

7.22 Register 20: Watch dog timer (Default: 88h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	Reserved	1	Reserved	R/W
6	WD_TIME [6]	0	Watchdog Timer timeout duration. The bit resolution is 250mS. The default time is 8*250mS = 2.0 seconds. If Watchdog Timer is started, this register will down count. Reading this register will return the down count value.	R/W
5	WD_TIME [5]	0		R/W
4	WD_TIME [4]	0		R/W
3	WD_TIME [3]	1		R/W
2	WD_TIME [2]	0		R/W
1	WD_TIME [1]	0		R/W
0	WD_TIME [0]	0		R/W

7.23 Register21: Asynchronous mode Control (Default: 4Bh)

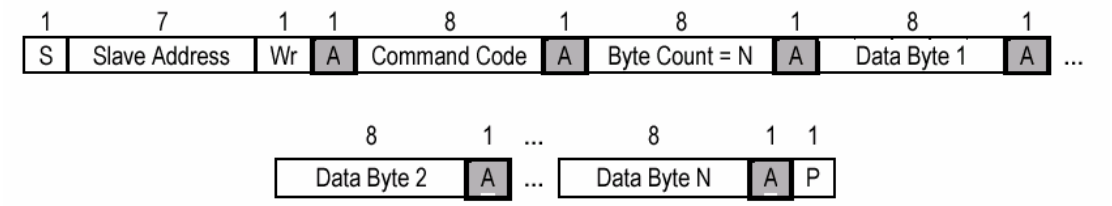
BIT	NAME	PWD	DESCRIPTION	TYPE
7	Tri-state	0	Tri-state all output if set 1	R/W
6	Reserved	1	Reserved	R/W
5	Reserved	0	Reserved	R/W
4	Reserved	0	Reserved	R/W
3	Reserved	1	Reserved	R/W
2	SRC_BASE3	0	1: Asynchronous PCIE / PCI always at 100MHz / 33MHz 0: PCIE / PCI frequency are follow Bit1, 0 setting	R/W
1	FIX_ADDR<1>	1	Asynchronous PCIE / PCI frequency table selection FIX_ADDR<1:0> => 00: 96 / 36MHz 01 : 96 / 32MHz 10: 128 / 38.4MHz 11 : Output from PLL1	R/W
0	FIX_ADDR<0>	1		R/W

8. ACCESS INTERFACE

The W83195BR-120 provides I^{2}C Serial Bus for microprocessor to read/write internal registers. In the W83195BR-120 is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I^{2}C address is defined at 0xD2.
The register number is increased by one if using byte data read/write protocol.

Example: In block mode, byte number of program register is 1
In byte mode, byte number of program register is 2 (Byte number of block mode +1)

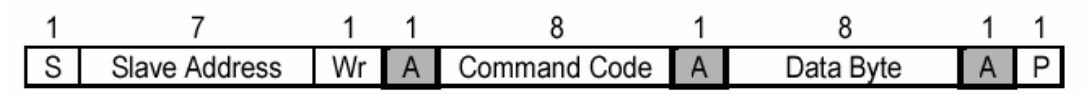
8.1 Block Write protocol



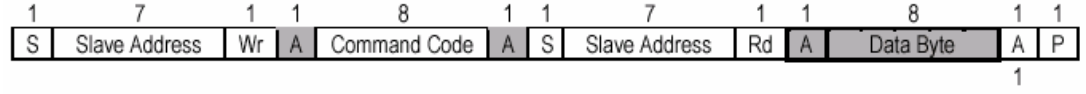
8.2 Block Read protocol

In block mode, the command code must filled 8'h00

8.3 Byte Write protocol



8.4 Byte Read protocol



9. SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD).

PARAMETER	RATING
Absolute 3.3V Core Supply Voltage	-0.5V to +4.6V
Absolute 3.3V I/O Supple Voltage	- 0.5V to + 4.6V
Operating 3.3V Core Supply Voltage	3.135V to 3.465V
Operating 3.3V I/O Supple Voltage	3.135V to 3.465V
Storage Temperature	- 65°C to + 150°C
Ambient Temperature	- 55°C to + 125°C
Operating Temperature	0°C to + 70°C
Input ESD protection (Human body model)	2000V

9.2 General Operating Characteristics

VDD= 3.3V ± 5 %, TA = 0℃ to +70℃,					
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Input Low Voltage	V_{IL}		0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0		V_{dc}	
Output Low Voltage	V_{OL}		0.4	V_{dc}	
Output High Voltage	V_{OH}	2.4		V_{dc}	
Operating Supply Current	I_{dd}		350	mA	CPU = 100 to 400 MHz PCI = 33.3 Mhz with load
Input pin capacitance	Cin		5	pF	
Output pin capacitance	Cout		6	pF	
Input pin inductance	Lin		7	nH	

9.3 Skew Group timing clock

VDD = 3.3V ± 5 %, TA = 0℃ to +70℃, Cl=10pF				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
CPU pair to CPU pair Skew		125	ps	Measure Crossing point
PCIE pair to PCIE pair Skew		125	ps	Measure Crossing point
PCI to PCI Skew		500	ps	Measured at 1.5V
48MHz to 48MHz Skew		1000	ps	Measured at 1.5V

9.4 CPU 0.7V Electrical Characteristics

*VDDC= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 Cl=2pF, Vol=0.175V, Voh=0.525V, Vr=475, IREF=2.32mA, Ioh=6*IREF*				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	175	700	ps	Measure Single Ended waveform
Fall Time	175	700	ps	Measure Single Ended waveform
Absolute crossing point Voltages	250	550	mV	Measure Single Ended waveform
Voltage High	660	850	mV	Measure Single Ended waveform
Voltage Low	-150		mV	Measure Single Ended waveform
Cycle to Cycle jitter		125	ps	Measure Differential waveform
Duty Cycle	45	55	%	Measure Differential waveform

9.5 SRC 0.7V Electrical Characteristics

*VDDS= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 Cl=2pF, Vol=0.175V, Voh=0.525V, Vr=475, IREF=2.32mA, Ioh=6*IREF*				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	175	700	ps	Measure Single Ended waveform
Fall Time	175	700	ps	Measure Single Ended waveform
Absolute crossing point Voltages	250	550	mV	Measure Single Ended waveform
Voltage High	660	850	mV	Measure Single Ended waveform
Voltage Low	-150		mV	Measure Single Ended waveform
Cycle to Cycle jitter		100	ps	Measure Differential waveform
Duty Cycle	45	55	%	Measure Differential waveform

9.6 PCIE 0.7V Electrical Characteristics

*VDDPE= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 Cl=2pF, Vol=0.175V, Voh=0.525V, Vr=475, IREF=2.32mA, Ioh=6*IREF*				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	175	700	ps	Measure Single Ended waveform
Fall Time	175	700	ps	Measure Single Ended waveform
Absolute crossing point Voltages	250	550	mV	Measure Single Ended waveform
Voltage High	660	850	mV	Measure Single Ended waveform
Voltage Low	-150		mV	Measure Single Ended waveform
Cycle to Cycle jitter		100	ps	Measure Differential waveform
Duty Cycle	45	55	%	Measure Differential waveform

9.7 PCI Electrical Characteristics

VDDP= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	2000	ps	Vol=0.4V, Voh=2.4V
Fall Time	500	2000	ps	Voh=2.4V, Vol=0.4V
Cycle to Cycle jitter		250	ps	Measured at 1.5V
Duty Cycle	45	55	%	Measured at 1.5V
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.8 24M, 48M Electrical Characteristics

VDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	2000	ps	Vol=0.4V, Voh=2.4V
Fall Time	500	2000	ps	Voh=2.4V, Vol=0.4V
Long term jitter		500	ps	Measured at 1.5V
Duty Cycle	45	55	%	Measured at 1.5V
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.9 REF Electrical Characteristics

VDD= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	500	2000	ps	Vol=0.4V, Voh=2.4V
Fall Time	500	2000	ps	Voh=2.4V, Vol=0.4V
Cycle to Cycle jitter		1000	ps	Measured at 1.5V
Duty Cycle	45	55	%	Measured at 1.5V
Pull-Up Current Min	-29		mA	Vout=1.0V
Pull-Up Current Max		-23	mA	Vout=3.135V
Pull-Down Current Min	29		mA	Vout=1.95V
Pull-Down Current Max		27	mA	Vout=0.4V

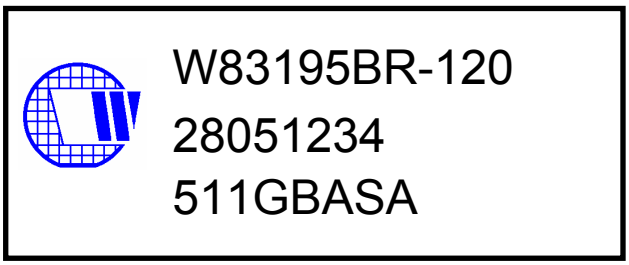
9.10 DOT 0.7V Electrical Characteristics

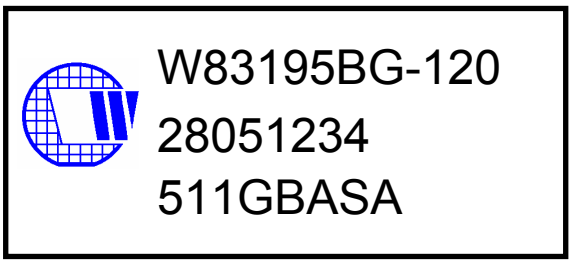
*VDD= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 Cl=2pF, Vol=0.175V, Voh=0.525V, Vr=475, IREF=2.32mA, Ioh=6*IREF*				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	175	700	ps	Measure Single Ended waveform
Fall Time	175	700	ps	Measure Single Ended waveform
Absolute crossing point Voltages	250	550	mV	Measure Single Ended waveform
Voltage High	660	850	mV	Measure Single Ended waveform
Voltage Low	-150		mV	Measure Single Ended waveform
Cycle to Cycle jitter		250	ps	Measure Differential waveform
Duty Cycle	45	55	%	Measure Differential waveform

10. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83195BR-120	56 PIN SSOP	Commercial, 0°C to +70°C
W83195BG-120	56PIN SSOP (Lead free package)	Commercial, 0°C to +70°C

11. HOW TO READ THE TOP MARKING





1st line: Winbond logo and the type number:

Normal part:W83195BR-120 , Lead free part: W83195BG-120

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 511 G B A SA

511: packages made in '2005, week 11

G: assembly house ID; O means OSE, G means GR

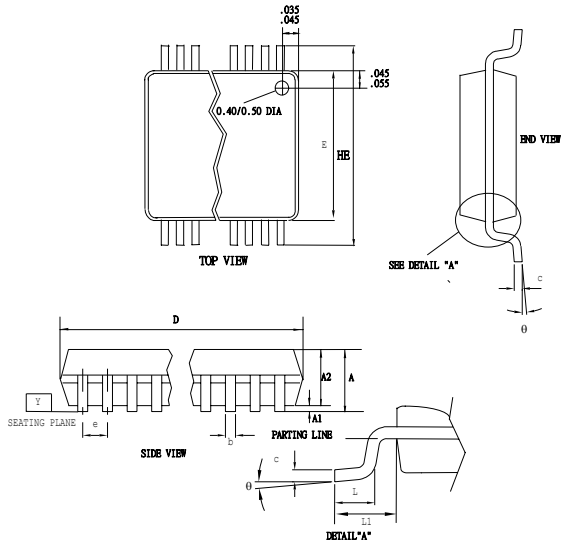
B: Internal use code

A: IC revision

SA: Internal use code

12. PACKAGE DRAWING AND DIMENSIONS

56 PIN SSOP-300mil



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	2.41	2.57	2.79	0.095	0.101	0.110
A1	0.20	0.30	0.41	0.008	0.012	0.016
A2	2.24	2.29	2.34	0.088	0.090	0.092
b	0.20	0.25	0.34	0.008	0.010	0.0135
c	0.13	—	0.25	0.005	—	0.010
D	18.2	18.42	18.54	0.720	0.725	0.730
H_E	10.16	10.31	10.41	0.400	0.406	0.410
E	7.42	7.52	7.59	0.292	0.296	0.299
e	0.51	0.64	0.76	0.020	0.025	0.030
L	0.61	0.81	1.02	0.024	0.032	0.040
L1	—	1.40	—	—	0.055	—
Y	—	—	0.08	—	—	0.003
θ	0	—	8	0	—	8

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