W83195BR-202

W83195BG-202

Winbond Clock Generator for AMD K8 System Series Chipsets

Date: 4/10/2006 Revision: 0.6

W83195BR-202/W83195BG-202 Data Sheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1	n.a.	01/11/2005	0.5	n.a.	All of the versions before 0.50 are for internal use.
2	n.a.	04/10/2006	0.6	n.a.	Modify registers with blue text Add Pb-free part no:W83195BG-202
3					
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LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

Table of Content-

CLOCK GEN. FOR AMD K8 SYSTEM SERIES CHIPSET

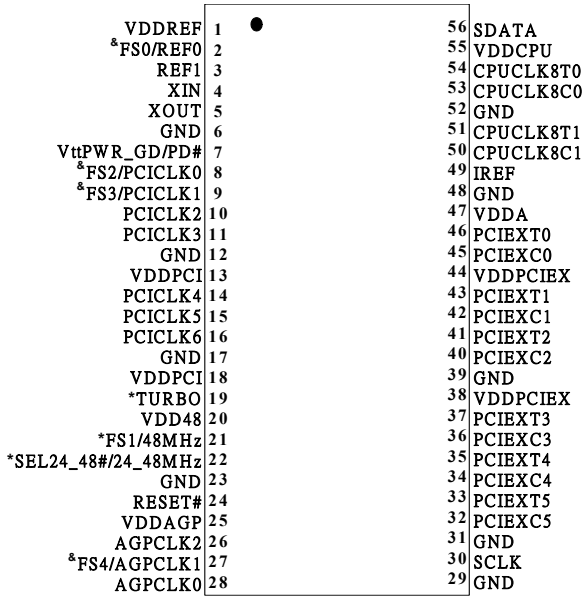
1. GENERAL DESCRIPTION

The **W83195BR-202** is a Clock Synthesizer meets AMD ATHLON 64 and OPTERON Processors series chipset. The **W83195BR-202** provides all clocks required for high-speed microprocessor and provides step-less frequency programming and 32 different frequencies of CPU, AGP, PCI, PCI-Express clocks setting. All clocks are externally selectable with smooth transitions. Employing the use of a serially programmable I^2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. By the way, the W83195BR-202 also has watchdog timer and reset out pin to support auto-reset when systems hanging caused by improper frequency setting.

2. PRODUCT FEATURES

- 2 pair 3.3V push-pull differential clock outputs for CPU and Chipset
- 6 PCI-Ex differential pairs
- 3 AGP clock output
- 7 PCI synchronous clocks
- 1 48MHz clock outputs
- 1 24_48MHz for I/O chip, default 24MHz
- 2 REF 14.318MHz clock outputs
- I^2C 2-Wire serial interface supports block and byte mode read/write
- Step-less frequency programming
- Smooth frequency switch with selections from 100 to 400MHz
- Programmable clock outputs Slew rate control and Skew control
- +/- 0.5% center type spread spectrum in table mode
- Programmable S.S.T. scale to reduce EMI
- Programmable registers to enable/stop each output and select modes
- Watch dog timer and RESET# output pins
- 56-pin SSOP package

3. PIN CONFIGURATION

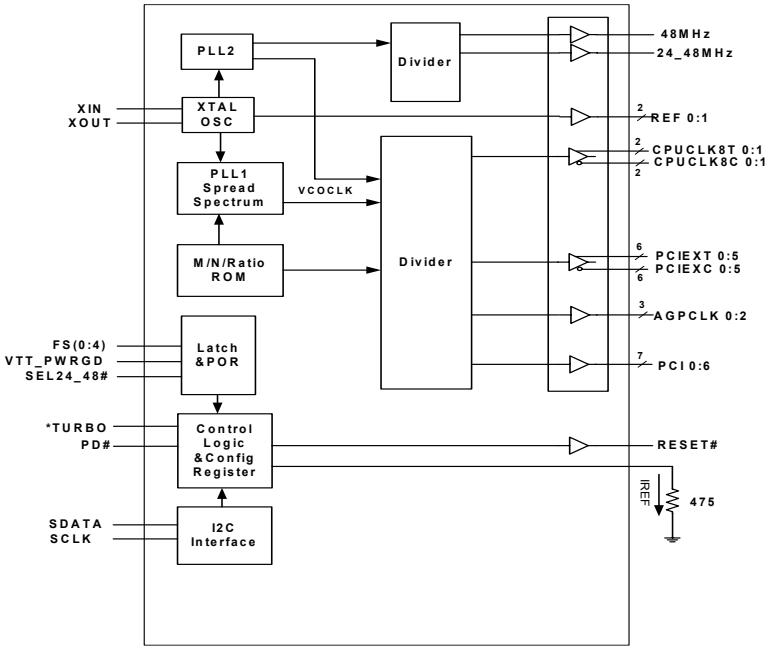


#: Active low

*: Internal pull up resistor 120KΩ to VDD

&: Internal Pull-down resistor 120KΩ to GND

4. BLOCK DIAGRAM



5. PIN DESCRIPTION

BUFFER TYPE SYMBOL	DESCRIPTION
IN	Input
IN_{td120k}	Latch input pin and internal 120KΩ pull down
IN_{tp120k}	Latch input pin and internal 120KΩ pull up
OUT	Output
I/O	Bi-directional Pin
I/OD	Bi-directional Pin, Open Drain
OD	Open Drain
#	Active Low
*	Internal 120kΩ pull-up
&	Internal 120kΩ pull-down

5.1 Crystal I/O

PIN	PIN NAME	TYPE	DESCRIPTION
4	XIN	IN	Crystal input with internal loading capacitors (18pF) and feedback resistors.
5	XOUT	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors (18pF).

5.2 CPU, PCIEX, AGP, and PCI Clock Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
54,53 51,50	CPUCLK8T [0:1] CPUCLK8C [0:1]	OUT	Push-pull differential clock outputs for host frequencies of CPU
46,45,43,42 41,40,37,36 35,34,33,32	PCIEXT [0:5] PCIEXC [0:5]	OUT	Current mode differential clock outputs for PCI-Express
26	AGPCLK2	OUT	3.3V AGP clock output.
27	AGPCLK1	OUT	3.3V AGP clock output.
	&FS4	IN_{td120k}	Latched input for FS4 at initial power up for H/W selecting the output frequency. Latched voltage level refers to Vil_FS and Vih_FS voltage level. This is internal 120K pull down.
28	AGPCLK0	OUT	3.3V AGP clock output.

CPU, PCIEX, AGP, and PCI Clock Outputs, continued

PIN	PIN NAME	TYPE	DESCRIPTION
8	PCICLK0	OUT	3.3V PCI clock output.
	&FS2	IN_{td120k}	Latched input for FS2 at initial power up for H/W selecting the output frequency. Latched voltage level refers to Vil_FS and Vih_FS voltage level. This is internal 120K pull down.
9	PCICLK1	OUT	3.3V PCI clock output.
	&FS3	IN_{td120k}	Latched input for FS3 at initial power up for H/W selecting the output frequency. Latched voltage level refers to Vil_FS and Vih_FS voltage level. This is internal 120K pull down.
10,11,14.15.16	PCICLK [2:6]	OUT	3.3V PCI clock outputs

5.3 Fixed Frequency Outputs

PIN	PIN NAME	TYPE	DESCRIPTION
2	REF0	OUT	3.3V REF 14.318Mhz clock output.
	&FS0	IN_{td120k}	Latched input for FS0 at initial power up for H/W selecting the output frequency, Latched voltage level refers to Vil_FS and Vih_FS voltage level. This is internal 120K pull down.
3	REF1	OUT	3.3V REF 14.318Mhz clock output.
22	24_48MHz	OUT	24MHz (default) or 48MHz clock output, In power on reset period, it is a hardware-latched pin, and it can be R/W by I2C control after power on reset period. Select by register 5 bit 7.
	*SEL24_48#	IN_{tp120k}	Latched input for 24MHz or 48MHz select pin. This is internal 120K pull up default 24MHz. In power on reset period, it is a hardware-latched pin, and it can be R/W by I2C control after power on reset period. Select by register 5 bit 7.
21	48MHz	OUT	48MHz clock output for USB.
	*FS1	IN_{tp120k}	Latched input for FS1 at initial power up for H/W selecting the output frequency. Latched voltage level refers to Vil_FS and Vih_FS voltage level. This is internal 120K pull up.

5.4 I²C Control Interface

PIN	PIN NAME	TYPE	DESCRIPTION
19	*TURBO#	IN_{tp120k}	Real time input pin to change frequency to a pre-programmed, Active low, Over clock entry by I²C register 17 &18. This is internal 120K pull up.
56	SDATA	I/O	Serial data of I²C 2-wire control interface with internal pull-up resistor.
30	SCLK	IN	Serial clock of I²C 2-wire control interface with internal pull-up resistor.

5.5 Power Management Pins

PIN	PIN NAME	TYPE	DESCRIPTION
49	IREF	OUT	Deciding the reference current for the differential pairs. The pin was connected to the precision resistor tied to ground to decide the appropriate current; 475 ohm is the standard value.
24	RESET#	OUT tp120k	System reset signal when the watchdog is time out. This pin will generate 250ms low phase when the watchdog timer is timeout. This is internal 120K pull up.
7	VTT_PWRGD	IN	Power good is a HIGH active input signal used to determine when FS [4:0] are valid to be sample.
	PD#	IN_{tp120k}	Power Down Function. This is power down pin, LOW active (PD). This is internal 120K pull up.

5.6 Power Pins

PIN	PIN NAME	TYPE	DESCRIPTION
47	VDDA	PWR	3.3V power supply for PLL core.
13,18	VDDPCI	PWR	3.3V power supply for PCI.
38,44	VDDPCIEX	PWR	3.3V power supply for PCI express pair.
25	VDDAGP	PWR	3.3V power supply for AGP.
20	VDD48	PWR	3.3V power supply for 48MHz.
55	VDDCPU	PWR	3.3V power supply for CPU.
1	VDDREF	PWR	3.3V power supply for REF.
6,12,17,23, 29,31,39,48,52	GND	PWR	Ground pin

6. FREQUENCY SELECTION BY HARDWARE OR SOFTWARE

This frequency table is used at power on latched FS [4:0] value or software programming at SSEL [4:0] (Register 0 bit 7 ~ 3).

FS4	FS3	FS2	FS1	FS0	CPU (MHZ)	PCIE (MHZ)	AGP (MHZ)	PCI (MHZ)
0	0	0	0	0	266.66	100.00	66.67	33.33
0	0	0	0	1	133.34	100.00	66.67	33.33
0	0	0	1	0	200.01	100.00	66.67	33.33
0	0	0	1	1	166.75	100.05	71.46	35.73
0	0	1	0	0	333.35	111.12	66.67	33.33
0	0	1	0	1	100.00	100.00	66.67	33.33
0	0	1	1	0	400.01	100.00	66.67	33.33
0	0	1	1	1	200.01	100.00	66.67	33.33
0	1	0	0	0	269.36	101.01	67.34	33.67
0	1	0	0	1	134.68	101.01	67.34	33.67
0	1	0	1	0	202.02	101.01	67.34	33.67
0	1	0	1	1	168.24	100.94	72.10	36.05
0	1	1	0	0	336.48	112.16	67.30	33.65
0	1	1	0	1	101.01	101.01	67.34	33.67
0	1	1	1	0	404.04	101.01	67.34	33.67
0	1	1	1	1	202.02	101.01	67.34	33.67
1	0	0	0	0	274.73	103.02	68.68	34.34
1	0	0	0	1	137.37	103.02	68.68	34.34
1	0	0	1	0	206.05	103.02	68.68	34.34
1	0	0	1	1	171.52	102.91	73.51	36.75
1	0	1	0	0	280.00	105.00	70.00	35.00
1	0	1	0	1	140.00	105.00	70.00	35.00
1	0	1	1	0	210.00	105.00	70.00	35.00
1	0	1	1	1	174.92	104.95	74.97	37.48
1	1	0	0	0	285.41	107.03	71.35	35.68
1	1	0	0	1	142.70	107.03	71.35	35.68
1	1	0	1	0	214.06	107.03	71.35	35.68
1	1	0	1	1	178.45	107.07	76.48	38.24
1	1	1	0	0	293.26	109.97	73.31	36.66
1	1	1	0	1	146.63	109.97	73.31	36.66
1	1	1	1	0	219.94	109.97	73.31	36.66
1	1	1	1	1	183.41	110.05	78.60	39.30

7. I²C CONTROL AND STATUS REGISTERS

7.1 Register 0: Frequency Select Register (Default = 10h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	SSEL [4]	0	Frequency selection by software via I²C	R/W
6	SSEL [3]	0		
5	SSEL [2]	0		
4	SSEL [1]	1		
3	SSEL [0]	0		
2	EN_SSEL	0	Enable software frequency table selection SSEL [4:0]. 0 = Select frequency by hardware. 1= Select frequency by software I²C - Bit 7~ 3.	R/W
1	SPSPEN	0	Enable Spread Spectrum in the frequency table. 0 = Normal 1 = Spread Spectrum enabled	R/W
0	EN_SAFE_FREQ	0	Enable reload safe frequency when the watchdog is timeout. 0 = reload the FS [4:0] latched pins when watchdog time out. 1 = reload the safe frequency bit defined at Register 5 bit 4~0.	R/W

7.2 Register 1: CPU Clock Control (1 = Enable, 0 = Stopped) (Default: E2h)

BIT	PIN NO	PWD	DESCRIPTION	TYPE
7	Reserved	1	Reserved	R/W
6	51,50	1	CPUCLK8T1 / C1 output control	R/W
5	54,53	1	CPUCLK8T0 / C0 output control	R/W
4	-	X	Power on latched value of FS4 pin, Default: 0.	R
3	-	X	Power on latched value of FS3 pin, Default: 0.	R
2	-	X	Power on latched value of FS2 pin, Default: 0.	R
1	-	X	Power on latched value of FS1 pin, Default: 1.	R
0	-	X	Power on latched value of FS0 pin, Default: 0.	R

7.3 Register 2: PCI Clock Control (1 = Enable, 0 = Stopped) (Default: FFh)

BIT	PIN NO	PWD	DESCRIPTION	TYPE
7	Reserved	1	Reserved	R/W
6	Reserved	1	Reserved	R/W
5	Reserved	1	Reserved	R/W
4	Reserved	1	Reserved	R/W
3	16	1	PCI6 output control	R/W
2	15	1	PCI5 output control	R/W
1	14	1	PCI4 output control	R/W
0	11	1	PCI3 output control	R/W

7.4 Register 3: AGP/PCI Clock Control (1 = Enable, 0 = Stopped) (Default: F3h)

BIT	PIN NO	PWD	DESCRIPTION	TYPE
7	10	1	PCI2 output control	R/W
6	9	1	PCI1 output control	R/W
5	8	1	PCI0 output control	R/W
4	26	1	AGP2 output control	R/W
3	Reserved	0	Reserved	R/W
2	Reserved	0	Reserved	R/W
1	27	1	AGP1 output control	R/W
0	28	1	AGP0 output control	R/W

7.5 Register 4: 24_48MHz, 48MHz, REF Control (1 = Enable, 0 = Stopped) (Default: FFh)

BIT	PIN NO	PWD	DESCRIPTION	TYPE
7	22	1	24_48MHz output control	R/W
6	Reserved	1	Reserved	R/W
5	21	1	48MHz output control	R/W
4	Reserved	1	Reserved	R/W
3	3	1	REF1 output control	R/W
2	2	1	REF0 output control	R/W
1	Reserved	1	Reserved	R/W
0	Reserved	1	Reserved	R/W

7.6 Register 5: Watchdog Control (Default: 82h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	SEL24_48	1	24_48 MHz output selection, 1: 24 MHz (Default), 0: 48 MHz. Default value follow hardware trapping data on SEL24_48# pin.	R/W
6	EN_WD	0	Program this bit => 1: Enable Watchdog Timer feature. 0: Disable Watchdog Timer feature. Read-back this bit => During timer count down the bit read back to 1. If count to zero, this bit read back to 0.	R/W
5	WD_TIMEOUT	0	Read Back only. Timeout Flag. This bit is Read Only. 1: Watchdog has ever started and counts to zero. 0: Watchdog is restarted and counting.	R
4	SAF_FREQ [4]	0	These bits will be reloaded in Reg-0 to select frequency table. As the watchdog is timeout and EN_SAFE_FREQ=1.	R/W
3	SAF_FREQ [3]	0		
2	SAF_FREQ [2]	0		
1	SAF_FREQ [1]	1		
0	SAF_FREQ [0]	0		

7.7 Register 6: PCIEX Control (1 = Enable, 0 = Stopped) (Default: FEh)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	Reserved	1	Reserved	R/W
6	33,32	1	PCIEXT5/C5 output control	R/W
5	35,34	1	PCIEXT4/C4 output control	R/W
4	37,36	1	PCIEXT3/C3 output control	R/W
3	41,40	1	PCIEXT2/C2 output control	R/W
2	43,42	1	PCIEXT1/C1 output control	R/W
1	46,45	1	PCIEXT0/C0 output control	R/W
0	Reserved	0	Reserved	R/W

7.8 Register 7: Winbond Chip ID (Default: 40h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	CHPI_ID [7]	0	Winbond Chip ID. W83195BR-202	R
6	CHPI_ID [6]	1	Winbond Chip ID.	R
5	CHPI_ID [5]	0	Winbond Chip ID.	R
4	CHPI_ID [4]	0	Winbond Chip ID.	R
3	CHPI_ID [3]	0	Winbond Chip ID.	R
2	CHPI_ID [2]	0	Winbond Chip ID.	R
1	CHPI_ID [1]	0	Winbond Chip ID.	R
0	CHPI_ID [0]	0	Winbond Chip ID.	R

7.9 Register 8: M/N Program (Default: D0h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	N_DIV [8]	1	Programmable N divisor value. Bit7~0 are defined in the Register 9	R/W
6	N_DIV [9]	1	Programmable N divisor value. Bit7~0 are defined in the Register 9	R/W
5	M_DIV [5]	0	Programmable M divisor value.	R/W
4	M_DIV [4]	1		R/W
3	M_DIV [3]	0		R/W
2	M_DIV [2]	0		R/W
1	M_DIV [1]	0		R/W
0	M_DIV [0]	0		R/W

7.10 Register 9: M/N Program Register (Default: 7Ah)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	N_DIV [7]	0	Programmable N divisor value bit 7 ~0. The bit 8 is defined in Register 8.	R/W
6	N_DIV [6]	1		R/W
5	N_DIV [5]	1		R/W
4	N_DIV [4]	1		R/W
3	N_DIV [3]	1		R/W
2	N_DIV [2]	0		R/W
1	N_DIV [1]	1		R/W
0	N_DIV [0]	0		R/W

7.11 Register 10: Reserved (Default: 03h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	SRC_SPSPEN	0	Enable PCIEX spread spectrum feature,1: Enable, 0: Disable	R/W
6	N3VAL<6>	0	Programmable N3 divisor 6~0 for programmable PCIEX clock. The N3VAL<8>, N3VAL<7> default value is 1. **VCO =14.318MHz*(N+4)/ 56**.	R/W
5	N3VAL<5>	0		R/W
4	N3VAL<4>	0		R/W
3	N3VAL<3>	0		R/W
2	N3VAL<2>	0		R/W
1	N3VAL<1>	1		R/W
0	N3VAL<0>	1		R/W

7.12 Register 11: Spread Spectrum Programming (Default: 0Bh)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	SP_UP [3]	0	Spread Spectrum Up Counter bit 3 ~ bit 0.	R/W
6	SP_UP [2]	0		R/W
5	SP_UP [1]	0		R/W
4	SP_UP [0]	0		R/W
3	SP_DOWN [3]	1	Spread Spectrum Down Counter bit 3 ~ bit 0 2's complement representation. Ex: 1 -> 1111; 2 -> 1110; 7 -> 1001; 8 -> 1000	R/W
2	SP_DOWN [2]	0		R/W
1	SP_DOWN [1]	1		R/W
0	SP_DOWN [0]	1		R/W

7.13 Register 12: Divisor Control (Default: 72h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	Reserved	0	Reserved	R/W
6	Reserved	X	Reserved	R/W
5	Reserved	X		R/W
4	Reserved	X	Reserved Reserved	R/W
3	Reserved	X		R/W
2	KVAL2	X	Define the CPU divider ratio Refer to Table-2	R/W
1	KVAL1	X		R/W

0	KVAL0	X		R/W

Table-2 CPU divider ratio selection Table

LSB / MSB		CPU			
		Bit1, 0			
		00	01	10	11
Bit2	0	Div2	Div3	Div4	Div6
	1	Div8	Div8	Div8	Div8

7.14 Register 13: Step-less Enable Control (Default: 3Fh)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	EN_MN_PROG	0	0: Output frequency depend on frequency table 1: Program all clock frequency by changing M/N value The equation is **VCO =14.318MHz*(N+4)/ M**. Once the watchdog timer timeout, the bit will be clear. Then the frequency will be decided by hardware default FS<4:0> or desired frequency select SAF_FREQ [4:0] depend on EN_SAFE_FREQ (Reg0 - bit 0).	R/W
6	N<10>	0	Programmable N divisor bit 10.	R/W
5	Reserved	1	Reserved	R/W
4	Reserved	1	Reserved	R/W
3	IVAL<3>	1	Charge pump current	R/W
2	IVAL<2>	1		R/W
1	IVAL<1>	1		R/W
0	IVAL<0>	1		R/W

7.15 Register 14: Control (Default: 10h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	DRI_CONT	0	CPUT / PCIE_T output state in during POWER DOWN assertion. 1: Driven (2*Iref), 0: Tristate (Floating) CPUT / PCIE_T output state in during STOP Mode assertion. 1: Driven (6*Iref), 0: Tristate (Floating) Complementary parts always tri-state (floating) in power down or stop mode.	R/W
6	Reserved	0	Reserved	R/W

Register 14: Control (Default: 10h), continued

BIT	NAME	PWD	DESCRIPTION	TYPE
5	SPCNT [5]	0	Spread Spectrum Programmable time, the resolution is 280ns. Default period is 11.8us	R/W
4	SPCNT [4]	1		R/W
3	SPCNT [3]	0		R/W
2	SPCNT [2]	0		R/W
1	SPCNT [1]	0		R/W
0	SPCNT [0]	0		R/W

7.16 Register 15: SST Control (Default: E9h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	INV_CPU	1	Invert the CPU phase, 0: Default, 1: Inverse	R/W
6	INV_AGP	1	Invert the CPU phase, 0: Default, 1: Inverse	R/W
5	Reserved	1	Reserved	R/W
4	SPSP1	0	Spread Spectrum type select. 00: Down 1% 01: Down 0.5% 10: Center +/- 0.5% 11: Center +/- 0.25%	R/W
3	SPSP0	1		R/W
2	ASKEW [2]	0	CPU1 to AGP skew control, Skew resolution is 300ps The decision of skew direction is same as ASKEW<2:0> setting	R/W
1	ASKEW [1]	0		R/W
0	ASKEW [0]	1		R/W

7.17 Register 16: Skew Control (Default: E0h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	INV_PCIEX	1	Invert the PCIEX phase, 0: Default, 1: Inverse	R/W
6	Reserved	1	Reserved	R/W
5	CSKEW [2]	1	CPUT1 to CPUT0 skew control, Skew resolution is 300ps The decision of skew direction is same as CSKEW<2:0> setting	R/W
4	CSKEW [1]	0		R/W
3	CSKEW [0]	0		R/W
2	PSKEW [2]	1	CPU1 to PCI skew control, Skew resolution is 300ps The decision of skew direction is same as PSKEW [2:0] setting	R/W
1	PSKEW [1]	0		R/W
0	PSKEW [0]	0		R/W

7.18 Register 17: Slew rate Control (Default: 03h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	Reserved	X	Reserved	R/W
6	INV_USB48	0	Invert the USB48 phase, 0: Default, 1: Inverse	R/W
5	Reserved	0	Reserved	R/W
4	TURBO_EN	0	Real mode overclocking feature 1: Enable 0: Disable This bit should be enable before using real mode overclocking feature.	R/W
3	Reserved	0	Reserved	R/W
2	Reserved	X	Reserved	R/W
1	NtVAL<9>	1	Dynamic programmable N divisor bit 9,8.	R/W
0	NtVAL<8>	1		R/W

7.19 Register 18: Reserved (Default: 7Ah)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	NtVAL<7>	0	Programmable Nt divisor value bit 7 ~0. The bit 8,9 is defined in Register 17.	R/W
6	NtVAL<6>	1		R/W
5	NtVAL<5>	1		R/W
4	NtVAL<4>	1		R/W
3	NtVAL<3>	0		R/W
2	NtVAL<2>	0		R/W
1	NtVAL<1>	1		R/W
0	NtVAL<0>	1		R/W

7.20 Register 19: Control (Default: 22h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	Reserved	0	Reserved	R/W
6	Reserved	0	Reserved	R/W
5	PEXSKEW [2]	1	CPU1 to PCIEX skew control, Skew resolution is 300ps The decision of skew direction is same as PEXSKEW<2:0> setting	R/W
4	PEXSKEW [1]	0		R/W
3	PEXSKEW [0]	0		R/W
2	Reserved	0	Reserved	R/W
1	Reserved	1	Reserved	R/W
0	Reserved	0	Reserved	R/W

7.21 Register 20: Watch dog timer (Default: 88h)

BIT	NAME	PWD	DESCRIPTION	TYPE
7	Reserved	1	Reserved	R/W
6	WD_TIME [6]	0	Setting the down count depth (Failure decision). One bit resolution represents 250ms. Default time depth is 8*250ms = 2.0 second. If the watchdog timer is counting, this register will return present down count value.	R/W
5	WD_TIME [5]	0		R/W
4	WD_TIME [4]	0		R/W
3	WD_TIME [3]	1		R/W
2	WD_TIME [2]	0		R/W
1	WD_TIME [1]	0		R/W
0	WD_TIME [0]	0		R/W

7.22 Register21: Control (Default: 2Bh)

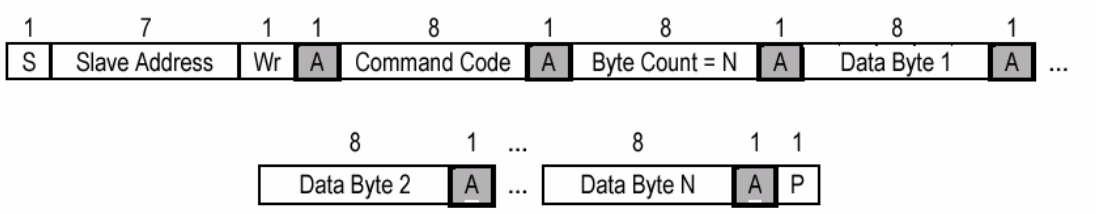
BIT	NAME	PWD	DESCRIPTION	TYPE
7	Tri-state	0	Tri-state all output if set 1	R/W
6	Reserved	0	Reserved	R/W
5	Reserved	1	Reserved	R/W
4	Reserved	0	Reserved	R/W
3	Reserved	1	Reserved	R/W
2	**SRC_BASE3**	**0**	**0 => PCIE is sync with CPU, 1 =>PCIE is async with CPU**	R/W
1	FIX_ADDR<1>	1	Asynchronous AGP / PCI frequency table selection FIX_ADDR<1:0> => 00: 72 / 36MHz 01 : 64 / 32MHz 10: Reserved 11 : Output from PLL1	R/W
0	FIX_ADDR<0>	1		R/W

8. ACCESS INTERFACE

The W83195BR-202 provides I^2C Serial Bus for microprocessor to read/write internal registers. In the W83195BR-202 is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I^2C address is defined at 0xD2.

Block Read and Block Write Protocol

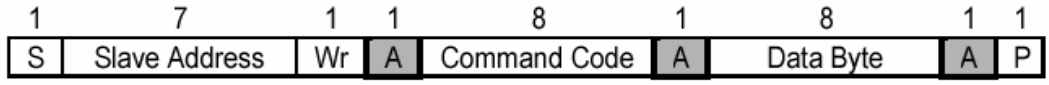
8.1 Block Write protocol



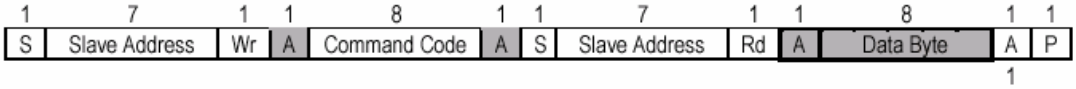
8.2 Block Read protocol

In block mode, the command code must filled 8'h00

8.3 Byte Write protocol



8.4 Byte Read protocol



9. SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD).

PARAMETER	RATING
Absolute 3.3V Core Supply Voltage	-0.5V to +4.6V
Absolute 3.3V I/O Supple Voltage	- 0.5 V to + 4.6 V
Operating 3.3V Core Supply Voltage	3.135V to 3.465V
Operating 3.3V I/O Supple Voltage	3.135V to 3.465V
Storage Temperature	- 65°C to + 150°C
Ambient Temperature	- 55°C to + 125°C
Operating Temperature	0°C to + 70°C
Input ESD protection (Human body model)	2000V

9.2 General Operating Characteristics

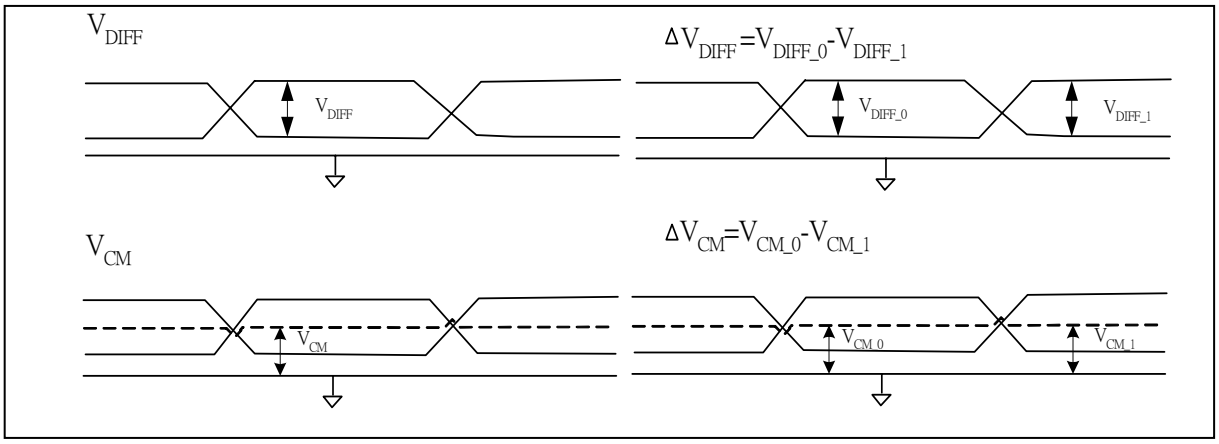
VDDREF =VDDA=VDDCPU=VDDPCI=VDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, CI=10pF					
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Input Low Voltage	V_{IL}		0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0		V_{dc}	
Output Low Voltage	V_{OL}		0.4	V_{dc}	All outputs using 3.3V power
Output High Voltage	V_{OH}	2.4		V_{dc}	All outputs using 3.3V power
Operating Supply Current	I_{dd}		300	mA	CPU = 100 to 400 MHz PCI = 33.3 Mhz with load
Input pin capacitance	Cin		5	pF	
Output pin capacitance	Cout		6	pF	
Input pin inductance	Lin		7	nH	

9.3 Skew Group timing clock

VDDREF =VDDA=VDDCPU=VDDPCI=VDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, CI=10pF					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**	**TEST CONDITIONS**
CPU to CPU Skew			250	ps	Crossing point for CPUT rising edge
CPU to PCI Skew			500	ps	Crossing point for CPUT rising edge and 1.5V for PCI clocks
CPU to AGP Skew			500	Ps	Crossing point for CPUT rising edge and 1.5V for AGP clocks
PCI to PCI Skew			500	ps	Measured between rising at 1.5V
PCI to AGP Skew			500	ps	Measured between rising at 1.5V
AGP to AGP Skew			500	ps	Measured between rising at 1.5V
48MHz to 48MHz Skew			1000	ps	Measured between rising at 1.5V
REF to REF Skew			500	ps	Measured between rising at 1.5V

9.4 CPU Electrical Characteristics

VDDA=VDDCPU= 3.3V ± 5 %, TA = 0℃ to +70℃, CI=10pF,					
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Edge Rate	2		10	V/ns	Measured at CPU test load. 0V±400mV (differential measurement)
Fall Edge Rate	2		10	V/ns	Measured at CPU test load. 0V±400mV (differential measurement)
V_{DIFF}: Differential Voltage (Single ended)	0.4	1.25	2.3	V	Measured at CPU test load. (Single ended measurement)
ΔV_{DIFF}: Change in V_{DIFF_DC} Magnitude	-150		+150	mV	Measured at CPU test load. (Single ended measurement)
V_{CM}: Common Mode Voltage	1.05	1.25	1.45	V	Measured at CPU test load. (Single ended measurement)
ΔV_{CM}: Change Common Voltage	-200		+200	mV	Measured at CPU test load. (Single ended measurement)
Duty Cycle	45	50	53	%	Measure at the differential crossing point
Cycle to Cycle Jitter		100	200	ps	Measured at the differential crossing point. Maximum difference of cycle time between two adjacent cycles.
Frequency Stabilization from Power-up (cold start)	0		3	ms	Measured from full supply voltage



9.5 AGP Electrical Characteristics

VDDPCI= 3.3V ± 5 %, TA = 0°C to +70°C, Test load, CI=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Edge Rate	1	4	V/ns	Measured from 20% to 60%
Fall Edge Rate	1	4	V/ns	Measured from 20% to 60%
Cycle to Cycle jitter		250	ps	Measured on rising edge at 1.5V, Maximum difference of cycle time between two adjacent cycles.
Jitter Accumulated	-1000	1000	ps	Measured using the JIT2 software package
Duty Cycle	45	55	%	Measured on rising and falling edge at 1.5V
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.6 PCI Electrical Characteristics

VDDPCI= 3.3V ± 5 %, TA = 0°C to +70°C, Test load, CI=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Edge Rate	1	4	V/ns	Measured from 20% to 60%
Fall Edge Rate	1	4	V/ns	Measured from 20% to 60%
Cycle to Cycle jitter		250	ps	Measured on rising edge at 1.5V, Maximum difference of cycle time between two adjacent cycles.

PCI Electrical Characteristics, continued

PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
Jitter Accumulated	-1000	1000	ps	Measured using the JIT2 software package
Duty Cycle	45	55	%	Measured on rising and falling edge at 1.5V
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.7 24M, 48M Electrical Characteristics

VDD48= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Edge Rate	0.5	2	V/ns	Measured from 20% to 80%
Fall Edge Rate	0.5	2	V/ns	Measured from 20% to 80%
Cycle to Cycle jitter		500	ps	Measured on rising edge at 1.5V, Maximum difference of cycle time between two adjacent cycles.
Jitter Accumulated	-1000	1000	ps	Measured using the JIT2 software package
Duty Cycle	45	55	%	Measured on rising and falling edge at 1.5V
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

9.8 REF Electrical Characteristics

VDDREF= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Edge Rate	0.5	2	V/ns	Measured from 20% to 80%
Fall Edge Rate	0.5	2	V/ns	Measured from 20% to 80%
Cycle to Cycle jitter		1000	ps	Measured on rising edge at 1.5V, Maximum difference of cycle time between two adjacent cycles.

REF Electrical Characteristics, continued

VDDREF= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load, Cl=10pF,				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Jitter Accumulated	-1000	1000	ps	Measured using the JIT2 software package
Duty Cycle	45	55	%	Measured on rising and falling edge at 1.5V
Pull-Up Current Min	-33		mA	Vout=1.0V
Pull-Up Current Max		-33	mA	Vout=3.135V
Pull-Down Current Min	30		mA	Vout=1.95V
Pull-Down Current Max		38	mA	Vout=0.4V

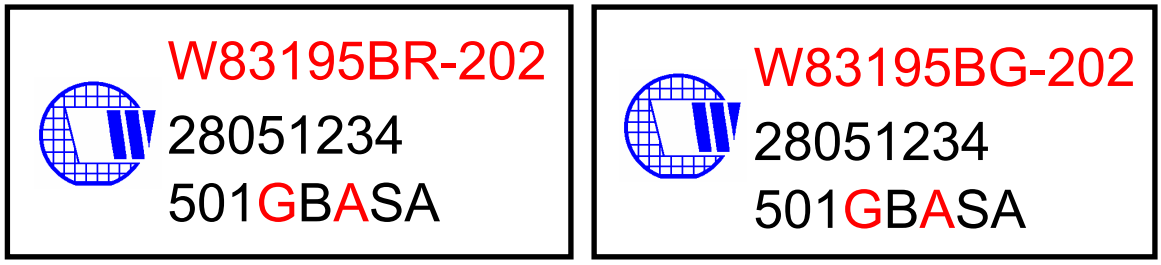
9.9 PCIEX 0.7V Electrical Characteristics

*VDDPE= 3.3V ± 5 %, TA = 0℃ to +70℃, Test load Rs=33, Rp=49.9 Cl=2pF, Vol=0.175V, Voh=0.525V, Vr=475, IREF=2.32mA, Ioh=6*IREF*				
PARAMETER	**MIN**	**MAX**	**UNITS**	**TEST CONDITIONS**
Rise Time	175	700	ps	Measure Single Ended waveform
Fall Time	175	700	ps	Measure Single Ended waveform
Absolute crossing point Voltages	250	550	mV	Measure Single Ended waveform
Voltage High	660	850	mV	Measure Single Ended waveform
Voltage Low	-150		mV	Measure Single Ended waveform
Cycle to Cycle jitter		85	ps	Measure Differential waveform
Duty Cycle	45	55	%	Measure Differential waveform

10. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83195BR-202	56 PIN SSOP	Commercial, 0°C to +70°C
W83195BG-202	56 PIN SSOP (Pb-free package)	Commercial, 0°C to +70°C

11. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83195BR-202

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 501 G A A SA

501: packages made in '2005, week 01

G: assembly house ID; O means OSE, G means GR

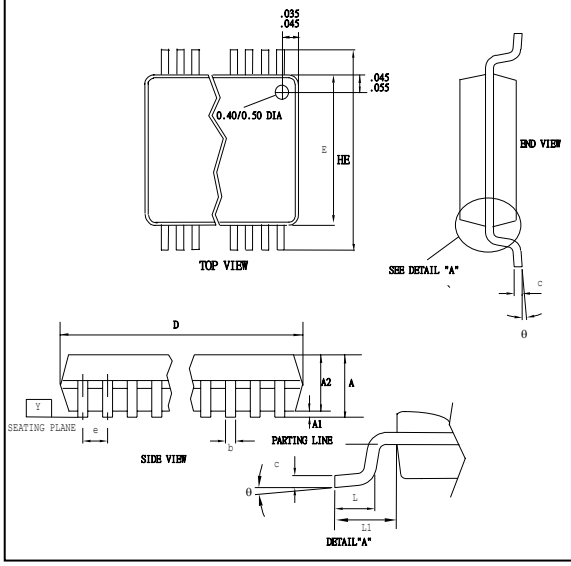
B: Internal use code

A: IC revision

SA: mask version

12. PACKAGE DRAWING AND DIMENSIONS

56 PIN SSOP-300mil



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	2.41	2.57	2.79	0.095	0.101	0.110
A1	0.20	0.30	0.41	0.008	0.012	0.016
A2	2.24	2.29	2.34	0.088	0.090	0.092
b	0.20	0.25	0.34	0.008	0.010	0.0135
c	0.13	—	0.25	0.005	—	0.010
D	18.2	18.42	18.54	0.720	0.725	0.730
H_E	10.16	10.31	10.41	0.400	0.406	0.410
E	7.42	7.52	7.59	0.292	0.296	0.299
e	0.51	0.64	0.76	0.020	0.025	0.030
L	0.61	0.81	1.02	0.024	0.032	0.040
L1	—	1.40	—	—	0.055	—
Y	—	—	0.08	—	—	0.003
θ	0	—	8	0	—	8

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