



W83194BR-619

W83194BG-619

**Winbond Clock Generator For INTEL
P4 Springdale Series Chipset**

Date: Mar/28/2006 Revision: 0.7

W83194BR-619/W83194BG-619



W83194BR-619/W83194BG-619 Data Sheet Revision History

| | PAGES | DATES | VERSION | WEB VERSION | MAIN CONTENTS |
|----|----------------|------------|---------|-------------|---|
| 1 | n.a. | | | | All of the versions before 0.5 are for internal use. |
| 2 | n.a. | 08/01/2003 | 0.5 | | First published preliminary version. |
| 3 | 7~15, 18~20 | 10/27/2004 | 0.6 | | Current register 12 bit 0,1 description and add register default value and add some description |
| 4 | | 03/28/2006 | 0.7 | 0.7 | Add lead-free part number W83194BG-619 |
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1. GENERAL DESCRIPTION

The W83194BR-619 is a Clock Synthesizer for Intel P4 Springdale series chipset. W83194BR-619 provides all clocks required for high-speed microprocessor and provides step-less frequency programming and 32 different frequencies of CPU, SRC, PCI, and 3V66 clocks setting. All clocks are externally selectable with smooth transitions.

The W83194BR-619 provides I²C serial bus interface to program the registers to enable or disable each clock outputs and provides +/-0.25%, +/-0.5% center type and -0.5%, -1.0% down type spread spectrum or programmable S.S.T. scale to reduce EMI.

The W83194BR-619 also has watchdog timer and reset output pin to support auto-reset when systems hanging caused by improper frequency setting.

The W83194BR-619 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply.

2. PRODUCT FEATURES

- 2 pairs current mode differential clock for CPU and Chipset
- 1 pairs current mode differential clock for SRC
- 3 3V66 clock outputs
- 1 3V66/VCH clock output default 66MHz
- 11 PCI synchronous clocks, 3 free running
- 1 48MHz clock outputs for USB and DOT
- 1 24_48MHz for I/O chip, default 48MHz
- 2 REF 14.318MHz clock outputs
- SRC/AGP/PCI clock out supports synchronous and asynchronous mode
- 3V66 leads PCICLK from 1.5ns to 3.5ns
- I²C 2-Wire serial interface supports block and byte mode read/write
- Step-less frequency programming
- Smooth frequency switch with selections from 100 to 400MHz
- Programmable clock outputs Slew rate control and Skew control
- +/- 0.25% center type spread spectrum in table mode
- Programmable S.S.T. scale to reduce EMI
- Programmable registers to enable/stop each output and select modes
- Watch Dog Timer and RESET# output pins
- 48-pin SSOP package

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3. PIN CONFIGURATION

| | | | |
|---------------------|----|----|----------------|
| FS1*/REF0 | 1 | 48 | VDDA |
| FS0*/REF1 | 2 | 47 | GND |
| VDDREF | 3 | 46 | IREF |
| XIN | 4 | 45 | RESET# |
| XOUT | 5 | 44 | GND |
| GND | 6 | 43 | CPUCLKT1 |
| FS2&/PCICLK_F0 | 7 | 42 | CPUCLKC1 |
| FS4&/PCICLK_F1 | 8 | 41 | VDDCPU |
| PCICLK_F2 | 9 | 40 | CPUCLKT0 |
| VDDPCI | 10 | 39 | CPUCLKC0 |
| GND | 11 | 38 | GND |
| PCICLK0 | 12 | 37 | SRCCCLKT |
| PCICLK1 | 13 | 36 | SRCCCLKC |
| PCICLK2 | 14 | 35 | VDD |
| PCICLK3 | 15 | 34 | VTT_PWRGD/PD#* |
| PCICLK4 | 16 | 33 | SDATA* |
| VDDPCI | 17 | 32 | SCLK* |
| GND | 18 | 31 | 3V66_0 |
| PCICLK5 | 19 | 30 | 3V66_1 |
| PCICLK6 | 20 | 29 | GND |
| PCICLK7 | 21 | 28 | VDD3V66 |
| SEL24_48#&/24_48MHz | 22 | 27 | 3V66_2 |
| FS3&/48MHz | 23 | 26 | 3V66_3/VCH |
| GND | 24 | 25 | VDD48 |

#: Active low

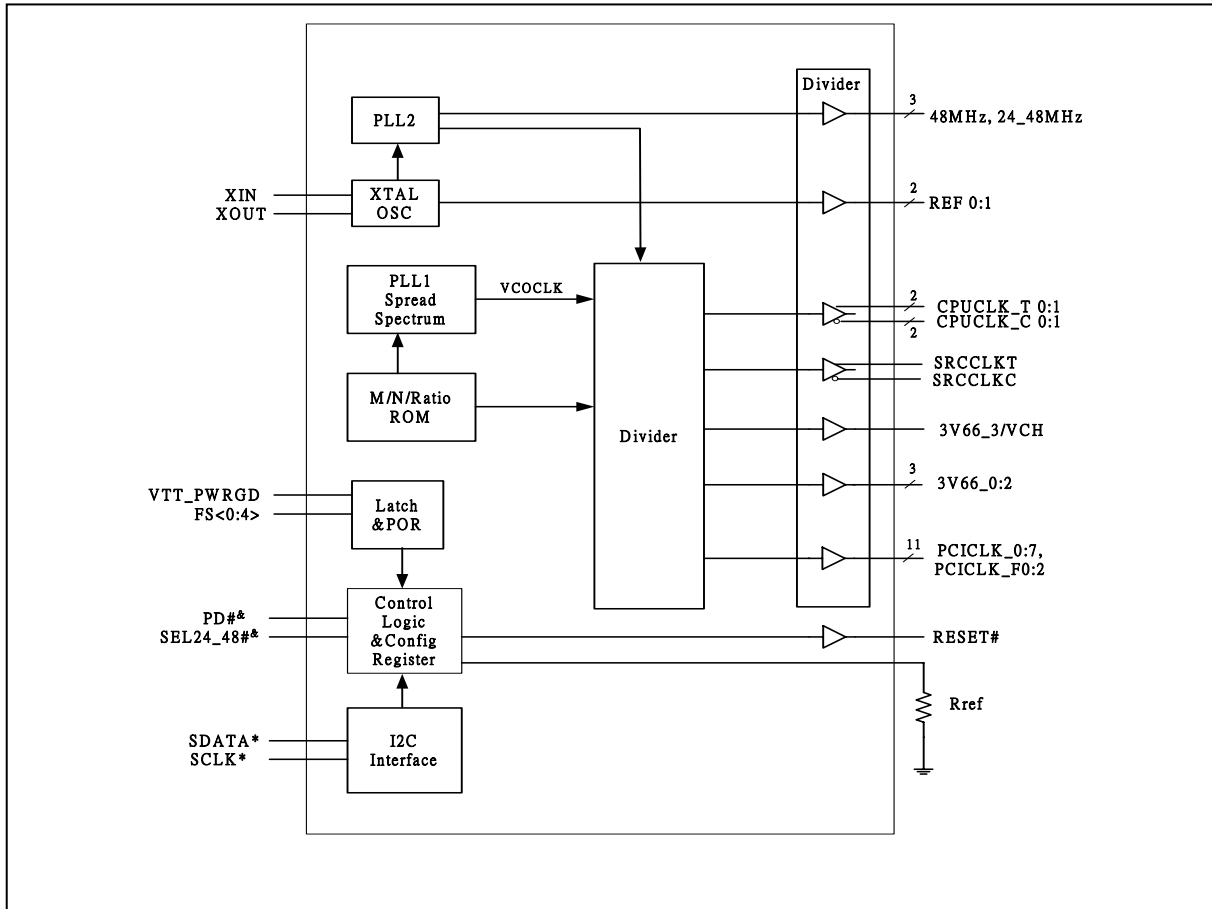
*: Internal pull up resistor 120KΩ to VDD

&: Internal Pull-down resistor 120KΩ to GND

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4. BLOCK DIAGRAM



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5. PIN DESCRIPTION

| BUFFER TYPE SYMBOL | DESCRIPTION |
|----------------------|--|
| IN | Input |
| IN _{td120k} | Latch input pin and internal 120KΩ pull down |
| IN _{tp120k} | Latch input pin and internal 120KΩ pull up |
| OUT | Output |
| OD | Open Drain |
| I/O | Bi-directional Pin |
| I/OD | Bi-directional Pin, Open Drain |
| # | Active Low |
| * | Internal 120kΩ pull-up |
| & | Internal 120kΩ pull-down |

5.1 Crystal I/O

| PIN | PIN NAME | TYPE | DESCRIPTION |
|-----|----------|------|--|
| 4 | XIN | IN | Crystal input with internal loading capacitors (18pF) and feedback resistors. |
| 5 | XOUT | OUT | Crystal output at 14.318MHz nominally with internal loading capacitors (18pF). |

5.2 CPU, SRC, 3V66, PCI Clock Outputs

| PIN | PIN NAME | TYPE | DESCRIPTION |
|----------------|--------------------------------|----------------------|--|
| 40, 43, 39, 42 | CPUCLKT [0:1] CPUCLKC [0:1] | OUT | 0.7V Current mode differential clock outputs for CPU and Chipset. |
| 37,36 | SRCCLKT, SRCCLKC | OUT | 0.7V Current mode differential clock outputs for Chipset, 100MHz (default) or 200MHz outputs selected by I2C register. |
| 26 | 3V66_3 | OUT | 66MHz (default) or 48MHz outputs selected by register byte 3 bit 4 selecting. |
| | VCH | OUT | |
| 31, 30, 27 | 3V66_0, 3V66_1, 3V66_2 | OUT | 3.3V 66MHz output clocks for the chipset and AGP slot. |
| 7 | PCICLK_F0 | OUT | 3.3V 33MHz PCI clock output. |
| | FS2& | IN _{td120k} | Latched input for FS2 at initial power up for H/W selecting the output frequency clocks. This is internal 120KΩ pull down. |
| 8 | PCICLK7_F1 | OUT | 3.3V 33MHz PCI clock output. |
| | FS4& | IN _{td120k} | Latched input for FS4 at initial power up for H/W selecting the output frequency clocks. This is internal 120KΩ pull down. |

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CPU, SRC, 3V66, PCI Clock Outputs, continued

| PIN | PIN NAME | TYPE | DESCRIPTION |
|------------------------------------|--------------|------|-------------------------------|
| 9 | PCICLK_F2 | OUT | 3.3V 33MHz PCI clock outputs. |
| 12,13, 14, 15, 16, 19, 20,21 | PCICLK [0:7] | OUT | 3.3V 33MHz PCI clock outputs. |

5.3 Fixed Frequency Outputs

| PIN | PIN NAME | TYPE | DESCRIPTION |
|-----|----------------------------|----------------------|---|
| 1 | REF0 | OUT | 14.318MHz output. |
| | FS1* | IN _{tp120k} | Latched input for FS1 at initial power up for H/W selecting the output frequency clocks. This is internal 120KΩ pull up. |
| 2 | REF1 | OUT | 14.318MHz output. |
| | FS0* | IN _{tp120k} | Latched input for FS0 at initial power up for H/W selecting the output frequency clocks. This is internal 120KΩ pull up. |
| 22 | 24_48MHz | OUT | 48MHz clock output. |
| | SEL24_48# ^{&} | IN _{td120k} | Latched input at initial power up for 24_48MHz selecting the output frequency clocks. This is internal 120KΩ pull down, 1=24MHz, 0=48MHz (default). |
| 22 | 48MHz | OUT | 48MHz clock output. |
| | FS3 ^{&} | IN _{td120k} | Latched input for FS3 at initial power up for H/W selecting the output frequency clocks. This is internal 120KΩ pull down. |

5.4 I2C Control Interface

| PIN | PIN NAME | TYPE | DESCRIPTION |
|-----|----------|------|---|
| 33 | SDATA* | I/OD | Serial data of I ² C 2-wire control interface with internal pull-up resistor. |
| 32 | SCLK* | IN | Serial clock of I ² C 2-wire control interface with internal pull-up resistor. |

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5.5 Output Control Pins

| PIN | PIN NAME | TYPE | DESCRIPTION | | | | | | | | |
|---------|----------------------|------------|--|--------------------|-------------------|----------------|---------|---------|----------------------|------------|-----------|
| 46 | IREF | OUT | Deciding the reference current for the CPUCLK pairs. The pin was connected to the precision resistor tied to ground to decide the appropriate current. The table is show as follows. | | | | | | | | |
| | | | <table border="1"> <thead> <tr> <th>Board Target Trace</th> <th>Reference R, Iref</th> <th>Output Current</th> <th>Ioh @ Z</th> </tr> </thead> <tbody> <tr> <td>50 Ohms</td> <td>R=475 Iref=2.32mA</td> <td>Ioh=6*Iref</td> <td>0.7V @ 50</td> </tr> </tbody> </table> | Board Target Trace | Reference R, Iref | Output Current | Ioh @ Z | 50 Ohms | R=475 Iref=2.32mA | Ioh=6*Iref | 0.7V @ 50 |
| | | | Board Target Trace | Reference R, Iref | Output Current | Ioh @ Z | | | | | |
| 50 Ohms | R=475 Iref=2.32mA | Ioh=6*Iref | 0.7V @ 50 | | | | | | | | |
| | | | | | | | | | | | |
| 45 | RESET# | OD | System reset signal when the watchdog is time out. This pin will generate 250mS when the watchdog timer is timeout. | | | | | | | | |
| 34 | VTT_PWRGD | IN | Power good input signal comes from ACPI with high active. This 3.3V input is level sensitive strobe used to determine FS [4:0] input are valid and is ready to sample. This pin is high active. | | | | | | | | |
| | PD#* | IN | Power Down Function. This is internal 120KΩ pull up. This is multi-function pin. When the VTT_PWRGD signal is asserted (this is, turns from a logical Low to high), the pin will be switched into the function of power down (PD#). | | | | | | | | |

5.6 Power an GND Pins

| PIN | PIN NAME | TYPE | DESCRIPTION |
|------------------------|----------|------|--------------------------------|
| 3 | VDDREF | PWR | 3.3V power supply for REF. |
| 10,17 | VDDPCI | PWR | 3.3V power supply for PCI. |
| 25 | VDD48 | PWR | 3.3V power supply for 48MHz. |
| 28 | VDD3V66 | PWR | 3.3V power supply for 3V66. |
| 35 | VDD | PWR | 3.3V power supply. |
| 41 | VDDCPU | PWR | 3.3V power supply for CPU. |
| 48 | VDDA | PWR | 3.3V power supply analog core. |
| 6,11,18,24,29,38,44,47 | GND | PWR | Ground pin |

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6. FREQUENCY SELECTION BY HARDWARE OR SOFTWARE

This frequency table is used at power on latched FS [4:0] value or software programming at SSEL [4:0] (Register 0 bit 7 ~ 3).

| FS4 | FS3 | FS2 | FS1 | FS0 | CPU (MHZ) | SRC (MHZ) | 3V66(MHZ) | PCI (MHZ) |
|-----|-----|-----|-----|-----|-----------|-----------|-----------|-----------|
| 0 | 0 | 0 | 0 | 0 | 100.0 | 100/200 | 66.6 | 33.3 |
| 0 | 0 | 0 | 0 | 1 | 200.0 | 100/200 | 66.6 | 33.3 |
| 0 | 0 | 0 | 1 | 0 | 133.3 | 100/200 | 66.6 | 33.3 |
| 0 | 0 | 0 | 1 | 1 | 166.6 | 100/200 | 66.6 | 33.3 |
| 0 | 0 | 1 | 0 | 0 | 200.0 | 100/200 | 66.6 | 33.3 |
| 0 | 0 | 1 | 0 | 1 | 400.0 | 100/200 | 66.6 | 33.3 |
| 0 | 0 | 1 | 1 | 0 | 266.6 | 100/200 | 66.6 | 33.3 |
| 0 | 0 | 1 | 1 | 1 | 333.3 | 100/200 | 66.6 | 33.3 |
| 0 | 1 | 0 | 0 | 0 | 100.9 | 100/200 | 66.6 | 33.3 |
| 0 | 1 | 0 | 0 | 1 | 202 | 100/200 | 66.6 | 33.3 |
| 0 | 1 | 0 | 1 | 0 | 134.6 | 100/200 | 66.6 | 33.3 |
| 0 | 1 | 0 | 1 | 1 | 168.3 | 100/200 | 66.6 | 33.3 |
| 0 | 1 | 1 | 0 | 0 | 115 | 100/200 | 66.6 | 33.3 |
| 0 | 1 | 1 | 0 | 1 | 230 | 100/200 | 66.6 | 33.3 |
| 0 | 1 | 1 | 1 | 0 | 153.3 | 100/200 | 66.6 | 33.3 |
| 0 | 1 | 1 | 1 | 1 | 191.6 | 100/200 | 66.6 | 33.3 |
| 1 | 0 | 0 | 0 | 0 | 100 | 100/200 | 66.6 | 33.3 |
| 1 | 0 | 0 | 0 | 1 | 200 | 100/200 | 66.6 | 33.3 |
| 1 | 0 | 0 | 1 | 0 | 133.3 | 100/200 | 66.6 | 33.3 |
| 1 | 0 | 0 | 1 | 1 | 166.6 | 100/200 | 66.6 | 33.3 |
| 1 | 0 | 1 | 0 | 0 | 200 | 100/200 | 66.6 | 33.3 |
| 1 | 0 | 1 | 0 | 1 | 400 | 100/200 | 66.6 | 33.3 |
| 1 | 0 | 1 | 1 | 0 | 266.6 | 100/200 | 66.6 | 33.3 |
| 1 | 0 | 1 | 1 | 1 | 333.3 | 100/200 | 66.6 | 33.3 |
| 1 | 1 | 0 | 0 | 0 | 105 | 100/200 | 66.6 | 33.3 |
| 1 | 1 | 0 | 0 | 1 | 210 | 100/200 | 66.6 | 33.3 |
| 1 | 1 | 0 | 1 | 0 | 140 | 100/200 | 66.6 | 33.3 |
| 1 | 1 | 0 | 1 | 1 | 175 | 100/200 | 66.6 | 33.3 |
| 1 | 1 | 1 | 0 | 0 | 110 | 100/200 | 66.6 | 33.3 |
| 1 | 1 | 1 | 0 | 1 | 220 | 100/200 | 66.6 | 33.3 |
| 1 | 1 | 1 | 1 | 0 | 146.6 | 100/200 | 66.6 | 33.3 |
| 1 | 1 | 1 | 1 | 1 | 183.3 | 100/200 | 66.6 | 33.3 |

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7. I²C CONTROL AND STATUS REGISTERS

(The register No. Is increased by 1 if use byte data read/write protocol)

7.1 Register 0: Frequency Select Register (Default =18H)

| BIT | NAME | PWD | DESCRIPTION |
|-----|--------------|-----|--|
| 7 | SSEL [4] | 0 | Software frequency table selection through I ² C |
| 6 | SSEL [3] | 0 | |
| 5 | SSEL [2] | 0 | |
| 4 | SSEL [1] | 1 | |
| 3 | SSEL [0] | 1 | |
| 2 | EN_SSEL | 0 | Enable software table selection FS [4:0]. 0 = Hardware table setting (Jump mode). 1 = Software table setting through Bit7~3. (Jump less mode) |
| 1 | SPSPEN | 0 | Enable spread spectrum mode under clock output. 0 = Spread Spectrum mode disable 1 = Spread Spectrum mode enable |
| 0 | EN_SAFE_FREQ | 0 | After watchdog timeout 0 = Reload the hardware FS [4:0] latched pins setting. 1 = Reload the desirable frequency table selection defined at Reg-5 Bit 4~0. |

7.2 Register 1: SRC/CPU Clock Register (1 = Enable, 0 = Disable) (Default =E3H)

| BIT | NAME | PWD | DESCRIPTION |
|-----|---------------------|-----|---|
| 7 | SRCLKT SRCCLKC | 1 | Pin 37,36 SRCCLK T/C output control |
| 6 | CPULKT1 CPUCLKC1 | 1 | Pin 43,42 CPULKT1/C1 output control |
| 5 | CPULKT0 CPUCLKC0 | 1 | Pin 40,39 CPULKT0/C0 output control |
| 4 | FS4 | X | Power on latched value of FS4 (9) pin. |
| 3 | FS3 | X | Power on latched value of FS3 (22) pin. |
| 2 | FS2 | X | Power on latched value of FS2 (8) pin. |
| 1 | FS1 | X | Power on latched value of FS1 (1) pin. |
| 0 | FS0 | X | Power on latched value of FS0 (2) pin. |

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7.3 Register 2: PCI Clock Register (1 = Enable, 0 = Disable) (Default =FFH)

| BIT | NAME | PWD | DESCRIPTION |
|-----|--------|-----|-------------------------------|
| 7 | PCI_F2 | 1 | Pin 10 PCI_F2 output control |
| 6 | PCI_F1 | 1 | Pin 9 PCI_F1 output control |
| 5 | PCI_F0 | 1 | Pin 8 PCI_F0 output control |
| 4 | PCI_7 | 1 | Pin 21 PCICLK7 output control |
| 3 | PCI_6 | 1 | Pin 20 PCICLK6 output control |
| 2 | PCI_5 | 1 | Pin 19 PCICLK5 output control |
| 1 | PCI_4 | 1 | Pin 16 PCICLK4 output control |
| 0 | PCI_3 | 1 | Pin 15 PCICLK3 output control |

7.4 Register 3: PCI, 3V66 Clock Register (1 = Enable, 0 = Disable) (Default =EFH)

| BIT | NAME | PWD | DESCRIPTION |
|-----|--------|-----|--|
| 7 | PCI_2 | 1 | Pin 14 PCICLK2 output control |
| 6 | PCI_1 | 1 | Pin 13 PCICLK1 output control |
| 5 | PCI_0 | 1 | Pin 12 PCICLK0 output control |
| 4 | VCH_EN | X | Pin 26 3V66_3 / VCH output select 1: VCH output, 0: 3V66 output (Default) |
| 3 | 3V66_3 | 1 | Pin 26 3V66_3 / VCH output control |
| 2 | 3V66_2 | 1 | Pin 27 3V66_2 output control |
| 1 | 3V66_1 | 1 | Pin 30 3V66_1 output control |
| 0 | 3V66_0 | 1 | Pin 31 3V66_0 output control |

7.5 Register 4: 24_48MHz, REF Control Register (1 = Enable, 0 = Disable) (Default =FCH)

| BIT | NAME | PWD | DESCRIPTION |
|-----|----------|-----|--------------------------------|
| 7 | 24_48MHz | 1 | Pin 22 24_48MHz output control |
| 6 | 48MHZ | 1 | Pin 23 48MHz output control |
| 5 | Reserve | 1 | Reserved |
| 4 | Reserve | 1 | Reserved |
| 3 | REF1 | 1 | Pin 2 REF1 output control |
| 2 | REF0 | 1 | Pin 1 REF0 output control |
| 1 | MODE1 | 0 | Clock output mode selection |
| 0 | MODE0 | 0 | Refer to Table-1 |

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7.6 Table-1: Clock output mode selection

| MODE | NORMAL MODE | CPU OVER CLOCK MODE | CPU/SRC OVER CLOCK MODE |
|--------------------|--------------------------|-------------------------------|-------------------------------|
| MODE1/0 | 00 | 01 | 10 |
| CPU over clock | Byte 8 & 9 | Byte 8 & 9 | Byte 8 & 9 |
| SRC over clock | Byte 8 & 9 | Byte 4 & 10 (asynchronous) | Byte 8 & 9 |
| AGP/PCI over clock | Byte 8 & 9 | Byte 4 & 10 (asynchronous) | Byte 4 & 10 (asynchronous) |
| Spreading | All clocks are Effective | CPU is effective Only. | CPU and SRC are Effective. |

7.7 Register 5: Watchdog Control Register (Default =C0H)

| BIT | NAME | PWD | DESCRIPTION |
|-----|--------------|-----|---|
| 7 | SEL24 | X | Pin 22 24 / 48 MHz output selection 1: 24 MHz, 0: 48 MHz. (Default) Default value follow hardware trapping data on SEL24_48# pin. |
| 6 | EN_WD | 1 | Program this bit => 1: Enable Watchdog Timer feature. 0: Disable Watchdog Timer feature. Read-back this bit => During timer count down the bit read back to 1. If count to zero, this bit read back to 0 |
| 5 | WD_TIMEOUT | 0 | Read Back only. Timeout Flag. 1: Watchdog has ever started and counts to zero. 0: Watchdog is restarted and counting. |
| 4 | SAF_FREQ [4] | 0 | These bits will be reloaded in Reg-0 to select frequency table. As the watchdog is timeout and EN_SAFE_FREQ=1. |
| 3 | SAF_FREQ [3] | 0 | |
| 2 | SAF_FREQ [2] | 0 | |
| 1 | SAF_FREQ [1] | 0 | |
| 0 | SAF_FREQ [0] | 0 | |

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7.8 Register 6: Watchdog Timer Register (Default =08H)

| BIT | NAME | PWD | DESCRIPTION |
|-----|-------------|-----|---|
| 7 | WD_TIME [7] | 0 | Setting the down count depth. One bit resolution represents 250ms. Default time depth is 8*250ms = 2.0 second. If the watchdog timer is counting, this register will return present down count value. |
| 6 | WD_TIME [6] | 0 | |
| 5 | WD_TIME [5] | 0 | |
| 4 | WD_TIME [4] | 0 | |
| 3 | WD_TIME [3] | 1 | |
| 2 | WD_TIME [2] | 0 | |
| 1 | WD_TIME [1] | 0 | |
| 0 | WD_TIME [0] | 0 | |

7.9 Register 7: M/N Program Register (Default =40H)

| BIT | NAME | PWD | DESCRIPTION |
|-----|-----------|-----|--|
| 7 | Tri-state | 0 | Tri-state all output if set 1 |
| 6 | Reserve | 1 | Reserved |
| 5 | Reserve | 0 | Reserved |
| 4 | FIX_AGP | 0 | AGP output frequency select mode 0: Output frequency according to frequency selection table 1: Output frequency according to FIX frequency table |
| 3 | Reserve | 0 | Reserved |
| 2 | Reserve | 0 | Reserved |
| 1 | ASEL<1> | 0 | Asynchronous AGP/PCI frequency table selection |
| 0 | ASEL<0> | 0 | ASEL<1:0> 00: 66.6MHz 01:72.1MHz 10: 79.9MHz 11:68.7MHz |

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7.10 Register 8: M/N Program Register (Default =8AH)

| BIT | NAME | PWD | DESCRIPTION |
|-----|-----------|-----|---|
| 7 | N_DIV [8] | 1 | Programmable N divisor value. Bit 7 ~0 are defined in the Register 8. |
| 6 | M_DIV [6] | 0 | |
| 5 | M_DIV [5] | 0 | |
| 4 | M_DIV [4] | 0 | |
| 3 | M_DIV [3] | 1 | |
| 2 | M_DIV [2] | 0 | |
| 1 | M_DIV [1] | 1 | |
| 0 | M_DIV [0] | 0 | |

7.11 Register 9: M/N Program Register (Default =CEH)

| BIT | NAME | PWD | DESCRIPTION |
|-----|-----------|-----|--|
| 7 | N_DIV [7] | 1 | Programmable N divisor value bit 7 ~0. The bit 8 is defined in Register 7. |
| 6 | N_DIV [6] | 1 | |
| 5 | N_DIV [5] | 0 | |
| 4 | N_DIV [4] | 0 | |
| 3 | N_DIV [3] | 1 | |
| 2 | N_DIV [2] | 1 | |
| 1 | N_DIV [1] | 1 | |
| 0 | N_DIV [0] | 0 | |

7.12 Register 10: M/N Program Register (Default =13H)

| BIT | NAME | PWD | DESCRIPTION |
|-----|---------|-----|---|
| 7 | Reserve | 0 | Reserved |
| 6 | N3<6> | 0 | Programmable N3 divisor bit 6 ~0 for synchronism SRC/AGP/PCI clock. |
| 5 | N3<5> | 0 | |
| 4 | N3<4> | 1 | |
| 3 | N3<3> | 0 | |
| 2 | N3<2> | 0 | |
| 1 | N3<1> | 1 | |
| 0 | N3<0> | 1 | |

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7.13 Register 11: Spread Spectrum Programming Register (Default =1FH)

| BIT | NAME | PWD | DESCRIPTION |
|-----|-------------|-----|--|
| 7 | SP_UP [3] | 0 | Spread Spectrum Up Counter bit 3 ~ bit 0. |
| 6 | SP_UP [2] | 0 | |
| 5 | SP_UP [1] | 0 | |
| 4 | SP_UP [0] | 1 | |
| 3 | SP_DOWN [3] | 1 | Spread Spectrum Down Counter bit 3 ~ bit 0 2's complement representation. Ex: 1 -> 1111; 2 -> 1110; 7 -> 1001; 8 -> 1000 |
| 2 | SP_DOWN [2] | 1 | |
| 1 | SP_DOWN [1] | 1 | |
| 0 | SP_DOWN [0] | 1 | |

7.14 Register 12: Divider Ratio Register (Default =C6H)

| BIT | NAME | PWD | DESCRIPTION |
|-----|-------|-----|--|
| 7 | SRC_H | 1 | SRC frequency select, 1: 100MHz, 0: 200MHz |
| 6 | DS9 | 1 | Define the AGP divider ratio, Table-2 integrate the all divider configuration |
| 5 | DS5 | 0 | Define the AGP divider ratio |
| 4 | DS4 | 0 | Table-2 integrate the all divider configuration |
| 3 | DS3 | 0 | Define the SRC divider ratio |
| 2 | DS2 | 1 | Refer to Table-2 |
| 1 | DS1 | 1 | Define the CPU divider ratio |
| 0 | DS0 | 0 | Refer to Table-2 |

7.15 Table-2 CPU, SRC, AGP divider ratio selection Table

| MSB \ LSB | | CPU | | SRC | | AGP | | | |
|------------------------|---|------|------|------|------|---------|-------|-------|-------|
| | | Bit0 | | Bit2 | | Bit5, 4 | | | |
| | | 0 | 1 | 0 | 1 | 00 | 01 | 10 | 11 |
| Bit1/ Bit3/ Bit6 | 0 | Div2 | Div3 | Div2 | Div3 | Div5 | Div6 | Div7 | Div8 |
| | 1 | Div4 | Div5 | Div4 | Div5 | Div10 | Div12 | Div12 | Div12 |

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7.16 Register 13: Control Register (Default =0FH)

| BIT | NAME | PWD | DESCRIPTION |
|-----|------------|-----|--|
| 7 | EN_MN_PROG | 0 | 0: Output frequency depend on frequency table 1: Program all clock frequency by changing M/N value The equation is $VCO = 14.318MHz * (N+4) / M$. Once the watchdog timer timeout, the bit will be clear. Then the frequency will be decided by hardware default FS<4:0> or desired frequency select SAF_FREQ [4:0] depend on EN_SAFE_FREQ (Reg9 - bit 7). |
| 6 | Reserve | 0 | Reserved |
| 5 | Reserve | 0 | Reserved |
| 4 | Reserve | 0 | |
| 3 | IVAL<3> | 1 | |
| 2 | IVAL<2> | 1 | Charge pump current selection |
| 1 | IVAL<1> | 1 | |
| 0 | IVAL<0> | 1 | |

7.17 Register 14: Control Register (Default =32H)

| BIT | NAME | PWD | DESCRIPTION |
|-----|-----------|-----|---|
| 7 | CPUT_DRI | 0 | CPUT output state in during POWER DOWN or Stop mode assertion. 1: Driven (2*Iref), 0: Tristate (Floating) CPUC always tri-state (floating) in power down Assertion. |
| 6 | SRCT_DRI | 0 | SRC_T output state in during POWER DOWN or Stop mode assertion. 1: Driven (6*Iref), 0: Tristate (Floating) SRC_C always tri-state (floating) in power down Assertion. |
| 5 | SPCNT [5] | 1 | Spread Spectrum Programmable time, the resolution is 280ns. Default period is 11.8us |
| 4 | SPCNT [4] | 1 | |
| 3 | SPCNT [3] | 0 | |
| 2 | SPCNT [2] | 0 | |
| 1 | SPCNT [1] | 1 | |
| 0 | SPCNT [0] | 0 | |

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7.18 Register 15: Control Register (Default =3AH)

| BIT | NAME | PWD | DESCRIPTION |
|-----|-----------|-----|--|
| 7 | INV_CPU | 0 | Invert the CPU phase 0: Default, 1: Inverse |
| 6 | Reserve | 0 | Reserved |
| 5 | Reserve | 1 | Reserved |
| 4 | SPSP1 | 1 | Spread Spectrum type select. |
| 3 | SPSP0 | 1 | 00: Down 1% 01: Down 0.5% 10: Center \pm 0.5% 11: Center \pm 0.25% |
| 2 | ASKEW [2] | 1 | CPU to AGP skew control. Skew resolution is 300ps The decision of skew direction is same as ASKEW [2:0] setting |
| 1 | ASKEW [1] | 0 | |
| 0 | ASKEW [0] | 0 | |

7.19 Register 16: Control Register (Default =24H)

| BIT | NAME | PWD | DESCRIPTION |
|-----|-----------|-----|--|
| 7 | INV_AGP | 0 | Invert the AGP phase 0: Default, 1: Inverse |
| 6 | INV_PCI | 0 | Invert the PCI phase 0: Default, 1: Inverse |
| 5 | SSKEW [2] | 1 | CPU to SRC skew control, Skew resolution is 300ps The decision of skew direction is same as SSKEW [2:0] setting |
| 4 | SSKEW [1] | 0 | |
| 3 | SSKEW [0] | 0 | |
| 2 | PSKEW [2] | 1 | CPU to PCI skew control, Skew resolution is 300ps The decision of skew direction is same as PSKEW [2:0] setting |
| 1 | PSKEW [1] | 0 | |
| 0 | PSKEW [0] | 0 | |

7.20 Register 17: Slew Rate Control Register (Default =55H)

| BIT | NAME | PWD | DESCRIPTION |
|-----|-----------|-----|-------------------------------------|
| 7 | PCI_F2_S2 | 0 | PCI_F2 slew rate control |
| 6 | PCI_F2_S1 | 1 | 11: Strong, 00: Weak, 10/01: Normal |
| 5 | PCI_F0_S2 | 0 | PCI_F1 / PCI_F0 slew rate control |
| 4 | PCI_F0_S1 | 1 | 11: Strong, 00: Weak, 10/01: Normal |
| 3 | AGP_32_S2 | 0 | 3V66_3 / 3V66_2 slew rate control |
| 2 | AGP_32_S1 | 1 | 11: Strong, 00: Weak, 10/01: Normal |
| 1 | AGP_10_S2 | 0 | 3V66_1 / 3V66_0 slew rate control |
| 0 | AGP_10_S1 | 1 | 11: Strong, 00: Weak, 10/01: Normal |

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7.21 Register 18: Slew Rate Control (Default =55H)

| BIT | NAME | PWD | DESCRIPTION |
|-----|-----------|-----|-------------------------------------|
| 7 | PCI_75_S2 | 0 | PCI7, 6,5 slew rate control |
| 6 | PCI_75_S1 | 1 | 11: Strong, 00: Weak, 10/01: Normal |
| 5 | PCI_42_S2 | 0 | PCI4, 3,2 slew rate control |
| 4 | PCI_42_S1 | 1 | 11: Strong, 00: Weak, 10/01: Normal |
| 3 | PCI_10_S2 | 0 | PCI1, 0 slew rate control |
| 2 | PCI_10_S1 | 1 | 11: Strong, 00: Weak, 10/01: Normal |
| 1 | REF_S2 | 0 | REF slew rate control |
| 0 | REF_S1 | 1 | 11: Strong, 00: Weak, 10/01: Normal |

7.22 Register 19: Control Register (Default =FFH)

| BIT | NAME | PWD | DESCRIPTION |
|-----|------------|-----|---|
| 7 | CPUSTOP_EN | 1 | Stop all CPU clocks. 1: Enable stop feature, 0: Disable |
| 6 | PCISTOP_EN | 1 | Stop SRC clock and all PCI clocks except free running parts. 1: Enable stop feature, 0: Disable |
| 5 | SRCS_EN | 1 | Allow PCISTOP pin to affect SRC output state 1: Allow, 0: Ignore the PCISTOP pin effect (Free running) |
| 4 | INV_DOT48 | 1 | Invert the DOT48 phase 0: In phase with USB48, 1: 180 degrees out of phase |
| 3 | INV_USB48 | 1 | Invert the USB48 phase 0: In phase with DOT48, 1: 180 degrees out of phase |
| 2 | USB48_S2 | 1 | USB48/DOT48/USB24_48 slew rate control |
| 1 | USB48_S1 | 1 | 11: Strong, 00: Weak, 10/01: Normal |
| 0 | INV_SRC | 1 | Invert the SRC phase, 0: Default, 1: Inverse |

7.23 Register 20: Winbond Chip ID – Project Code Register (Ready Only) (Default =47H)

| BIT | NAME | PWD | DESCRIPTION |
|-----|-------------|-----|---|
| 7 | CHPI_ID [7] | 0 | Winbond Chip ID. W83194BR-619 (SA5847). |
| 6 | CHPI_ID [6] | 1 | Winbond Chip ID. |
| 5 | CHPI_ID [5] | 0 | Winbond Chip ID. |
| 4 | CHPI_ID [4] | 0 | Winbond Chip ID. |
| 3 | CHPI_ID [3] | 0 | Winbond Chip ID. |
| 2 | CHPI_ID [2] | 1 | Winbond Chip ID. |
| 1 | CHPI_ID [1] | 1 | Winbond Chip ID. |
| 0 | CHPI_ID [0] | 1 | Winbond Chip ID. |

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7.24 Register 21: Winbond Chip ID – Version Code Register (Ready Only) (Default =50H)

| BIT | NAME | PWD | DESCRIPTION |
|-----|----------------|-----|--|
| 7 | MAS_ID [1] | 0 | MASK definition for master body |
| 6 | MAS_ID [0] | 1 | *A****: 01, *B****: 10, *C****: 11, *D****:00 |
| 5 | SUB_ID [1] | 0 | MASK definition for code body |
| 4 | SUB_ID [0] | 1 | *A****001: 01, *A****002: 10, *A****003: 11, *A****004:00 |
| 3 | MAS_VER_ID [1] | 0 | MASK version definition for master body |
| 2 | MAS_VER_ID [0] | 0 | *A****001AA: 00, *A****001AB: 01, *A****001AC: 10, *A****001AD: 11. |
| 1 | SUB_VER_ID [1] | 0 | MASK version definition for code body *A****001A: 00, *A****001B: 01 *A****001C: 10, *A****001D: 11 |

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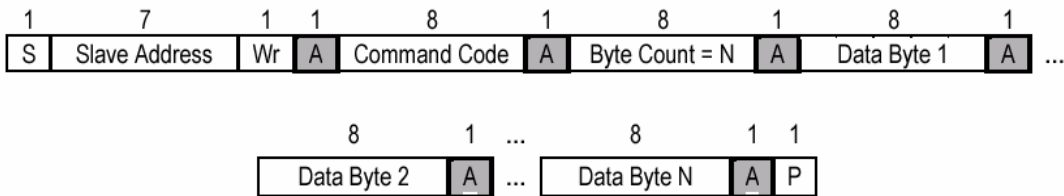


8. ACCESS INTERFACE

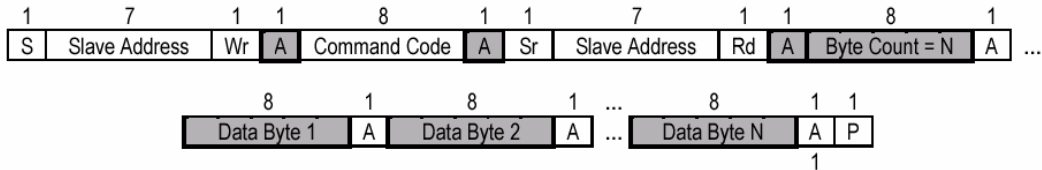
The W83194BR-619 provides I²C Serial Bus for microprocessor to read/write internal registers. In the W83194BR-619 is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I²C address is defined at 0xD2.

Block Read and Block Write Protocol

8.1 Block Write protocol

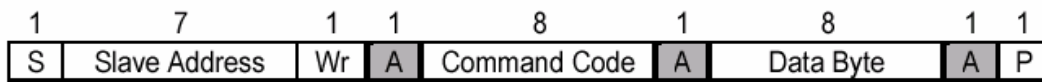


8.2 Block Read protocol

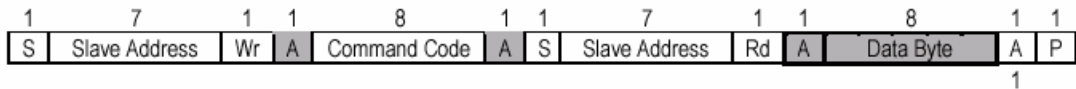


In block mode, the command code must filled 00H

8.3 Byte Write protocol



8.4 Byte Read protocol



W83194BR-619/W83194BG-619



9. SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD).

| PARAMETER | RATING |
|---|--------------------|
| Absolute 3.3V Core Supply Voltage | -0.5V to +4.6V |
| Absolute 3.3V I/O Supply Voltage | - 0.5 V to + 4.6 V |
| Operating 3.3V Core Supply Voltage | 3.135V to 3.465V |
| Operating 3.3V I/O Supply Voltage | 3.135V to 3.465V |
| Storage Temperature | - 65°C to + 150°C |
| Ambient Temperature | - 55°C to + 125°C |
| Operating Temperature | 0°C to + 70°C |
| Input ESD protection (Human body model) | 2000V |

9.2 General Operating Characteristics

| <i>VDDREF=VDDA=VDDCPU=VDD3V66=VDDPCI=VDD48= 3.3V ± 5 %, TA = 0°C to +70°C, CI=10pF</i> | | | | | |
|--|------------------|-----|-----|-----------------|--|
| PARAMETER | SYMBOL | MIN | MAX | UNITS | TEST CONDITIONS |
| Input Low Voltage | V _{IL} | | 0.8 | V _{dc} | |
| Input High Voltage | V _{IH} | 2.0 | | V _{dc} | |
| Output Low Voltage | V _{OL} | | 0.4 | V _{dc} | All outputs using 3.3V power |
| Output High Voltage | V _{OH} | 2.4 | | V _{dc} | All outputs using 3.3V power |
| Operating Supply Current | I _{dd} | | 350 | mA | CPU = 100 to 400 MHz PCI = 33.3 Mhz with load |
| Input pin capacitance | C _{in} | | 5 | pF | |
| Output pin capacitance | C _{out} | | 6 | pF | |
| Input pin inductance | L _{in} | | 7 | nH | |

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CLOCK GEN. FOR INTEL P4 SPRINGDALE/PRESCOTT SERIES CHIPSET

9.3 Skew Group timing clock

VDDREF =VDDA=VDDCPU=VDD3V66=VDDPCI=VDD48= 3.3V ± 5 %, TA = 0°C to +70°C, CI=10pF

| PARAMETER | MIN | TYP | MAX | UNITS | TEST CONDITIONS |
|---------------------|-----|-----|------|-------|------------------|
| 3V66 to PCI Skew | 1.5 | 2.6 | 3.5 | ns | Measured at 1.5V |
| CPU to CPU Skew | | | 100 | ps | Crossing point |
| 3V66 to 3V66 Skew | | | 250 | ps | Measured at 1.5V |
| PCI to PCI Skew | | | 500 | ps | Measured at 1.5V |
| 48MHz to 48MHz Skew | | | 1000 | ps | Measured at 1.5V |
| REF to REF Skew | | | 500 | ps | Measured at 1.5V |

9.4 CPU 0.7V Electrical Characteristics

VDDA=VDDCPU= 3.3V ± 5 %, TA = 0°C to +70°C, Test load Rs=33, Rp=49.9 CI=2pF, Vol=0.175V, Voh=0.525V, Vr=475, IREF=2.32mA, loh=6*IREF

| PARAMETER | MIN | MAX | UNITS | TEST CONDITIONS |
|----------------------------------|-----|-----|-------|-------------------------------|
| Rise Time | 175 | 700 | ps | Measure Single Ended waveform |
| Fall Time | 175 | 700 | ps | Measure Single Ended waveform |
| Absolute crossing point Voltages | 250 | 550 | mV | Measure Single Ended waveform |
| Cycle to Cycle jitter | | 125 | ps | Measure Differential waveform |
| Duty Cycle | 45 | 55 | % | Measure Differential waveform |

9.5 SRC 0.7V Electrical Characteristics

VDD= 3.3V ± 5 %, TA = 0°C to +70°C, Test load Rs=33, Rp=49.9 CI=2pF, Vol=0.175, Voh=0.525V, Vr=475, IREF=2.32mA, loh=6*IREF

| PARAMETER | MIN | MAX | UNITS | TEST CONDITIONS |
|----------------------------------|-----|-----|-------|-------------------------------|
| Rise Time | 175 | 700 | ps | Measure Single Ended waveform |
| Fall Time | 175 | 700 | ps | Measure Single Ended waveform |
| Absolute crossing point Voltages | 250 | 550 | mV | Measure Single Ended waveform |
| Cycle to Cycle jitter | | 125 | ps | Measure Differential waveform |
| Duty Cycle | 45 | 55 | % | Measure Differential waveform |

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9.6 3V66 Electrical Characteristics

| VDD3V66= 3.3V ± 5 %, TA = 0°C to +70°C, Test load, Cl=10pF, | | | | |
|--|-----|------|-------|--------------------|
| PARAMETER | MIN | MAX | UNITS | TEST CONDITIONS |
| Rise Time | 500 | 2000 | ps | Vol=0.4V, Voh=2.4V |
| Fall Time | 500 | 2000 | ps | Voh=2.4V, Vol=0.4V |
| Cycle to Cycle jitter | | 250 | ps | Measured at 1.5V |
| Duty Cycle | 45 | 55 | % | Measured at 1.5V |
| Pull-Up Current Min | -33 | | mA | Vout=1.0V |
| Pull-Up Current Max | | -33 | mA | Vout=3.135V |
| Pull-Down Current Min | 30 | | mA | Vout=1.95V |
| Pull-Down Current Max | | 38 | mA | Vout=0.4V |

9.7 PCI Electrical Characteristics

| VDDPCI= 3.3V ± 5 %, TA = 0°C to +70°C, Test load, Cl=10pF, | | | | |
|---|-----|------|-------|--------------------|
| PARAMETER | MIN | MAX | UNITS | TEST CONDITIONS |
| Rise Time | 500 | 2000 | ps | Vol=0.4V, Voh=2.4V |
| Fall Time | 500 | 2000 | ps | Voh=2.4V, Vol=0.4V |
| Cycle to Cycle jitter | | 250 | ps | Measured at 1.5V |
| Duty Cycle | 45 | 55 | % | Measured at 1.5V |
| Pull-Up Current Min | -33 | | mA | Vout=1.0V |
| Pull-Up Current Max | | -33 | mA | Vout=3.135V |
| Pull-Down Current Min | 30 | | mA | Vout=1.95V |
| Pull-Down Current Max | | 38 | mA | Vout=0.4V |

9.8 24M, 48M Electrical Characteristics

| VDD48= 3.3V ± 5 %, TA = 0°C to +70°C, Test load, Cl=10pF, | | | | |
|--|-----|------|-------|--------------------|
| PARAMETER | MIN | MAX | UNITS | TEST CONDITIONS |
| Rise Time | 500 | 2000 | ps | Vol=0.4V, Voh=2.4V |
| Fall Time | 500 | 2000 | ps | Voh=2.4V, Vol=0.4V |
| Long term jitter | | 500 | ps | Measured at 1.5V |
| Duty Cycle | 45 | 55 | % | Measured at 1.5V |
| Pull-Up Current Min | -33 | | mA | Vout=1.0V |
| Pull-Up Current Max | | -33 | mA | Vout=3.135V |
| Pull-Down Current Min | 30 | | mA | Vout=1.95V |
| Pull-Down Current Max | | 38 | mA | Vout=0.4V |

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9.9 REF Electrical Characteristics

| VDDREF= 3.3V ± 5 %, TA = 0°C to +70°C, Test load, CI=10pF, | | | | |
|---|------------|------------|--------------|--|
| PARAMETER | MIN | MAX | UNITS | TEST CONDITIONS |
| Rise Time | 1000 | 4000 | ps | V _{ol} =0.4V, V _{oh} =2.4V |
| Fall Time | 1000 | 4000 | ps | V _{oh} =2.4V, V _{ol} =0.4V |
| Cycle to Cycle jitter | | 1000 | ps | Measured at 1.5V |
| Duty Cycle | 45 | 55 | % | Measured at 1.5V |
| Pull-Up Current Min | -33 | | mA | V _{out} =1.0V |
| Pull-Up Current Max | | -33 | mA | V _{out} =3.135V |
| Pull-Down Current Min | 30 | | mA | V _{out} =1.95V |
| Pull-Down Current Max | | 38 | mA | V _{out} =0.4V |

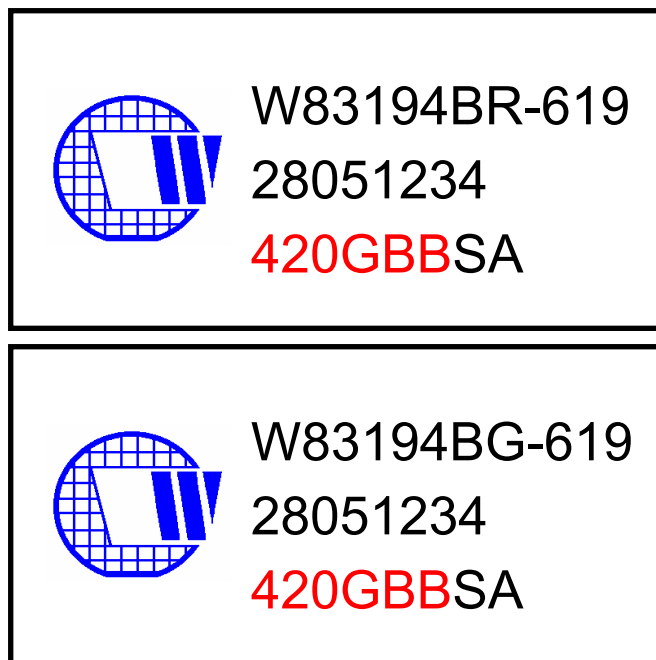
9.10 ORDERING INFORMATION

| PART NUMBER | PACKAGE TYPE | PRODUCTION FLOW |
|--------------------|-------------------------------|--------------------------|
| W83194BR-619 | 48 PIN SSOP | Commercial, 0°C to +70°C |
| W83194BG-619 | 48 PIN SSOP (Pb-free package) | Commercial, 0°C to +70°C |

W83194BR-619/W83194BG-619



9.11 How to read the top marking



1st line: Winbond logo and the type number: W83194BR-619/W83194BG-619

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 420 G B B SA

420: packages made in '2004, week 20

G: assembly house ID; O means OSE, G means GR

B: Internal use code

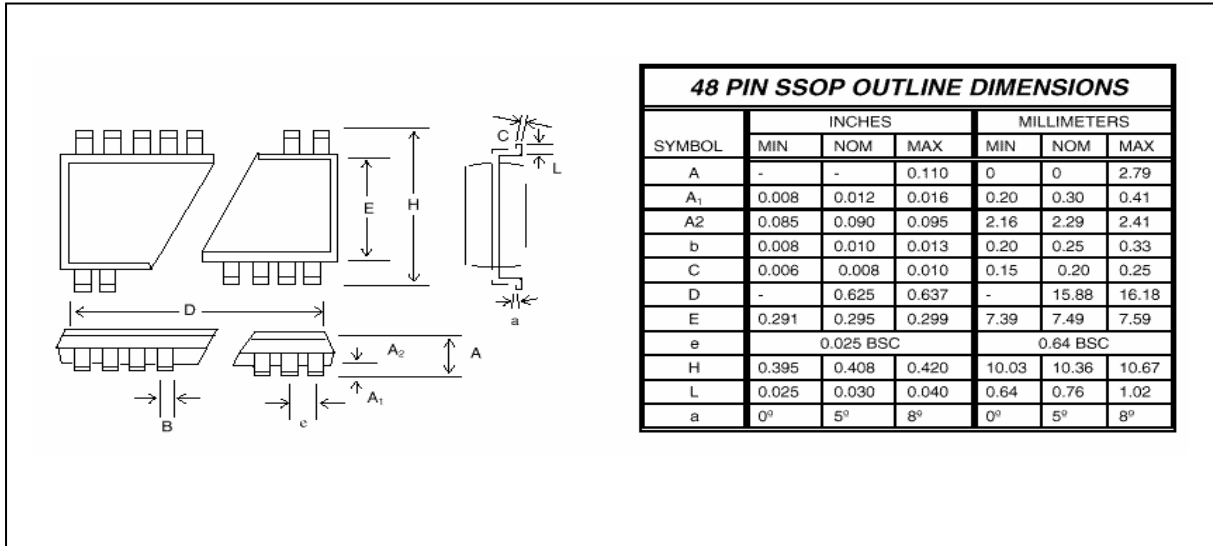
B: IC revision

SA: mask version

W83194BR-619/W83194BG-619



10. PACKAGE DRAWING AND DIMENSIONS



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