PCA2125

SPI Real time clock / calendar

Rev. 00.11 — 30 January 2007 Preliminary data sheet

1. Product profile

1.1 General description

The PCA2125 is a CMOS real time clock/calendar optimized for low power consumption and 125 °C operation. Data is transferred serially via an SPI bus with a maximum data rate of 8.0 Mbits/s. An alarm and timer function are also available with possibility to generate a wake-up signal on an interrupt pin.

1.2 Features

- Provides year, month, day, weekday, hours, minutes and seconds based on 32.768 kHz quartz crystal
- Resolution: seconds - years
- Clock operating voltage: 1.2 to 5.5 V
- Low backup current; typical 0.55 µA at V_{DD} = 3.0 V and T_{amb} = 25 °C
- 3 line SPI with separate combinable data input and output
- Serial interface (at V_{DD} = 1.8 to 5.5 V)
- 1 second or 1 minute interrupt output
- Freely programmable timer with interrupt capability
- Freely programmable alarm function with interrupt capability
- Integrated oscillator capacitor
- Internal power-on reset
- Open-drain interrupt pin

1.3 Applications

- Automotive time keeping application
- Metering

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage	SPI bus inactive; T_{amb} = 25 °C	1.2	-	5.5	V
		SPI bus active; T_{amb} = –40 to +125 °C	1.6	-	5.5	V

Table 1. Quick reference data *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	supply current	f_{SCL} = 7.0 MHz	-	-	800	µA
		f_{SCL} = 1.0 MHz	-	-	200	µA
		SPI bus inactive and CLKOUT disabled; f_{SCL} = 0 kHz; T_{amb} = 25 °C				
		V_{DD} = 5 V	-	550	725	nA
		V_{DD} = 2 V	-	550	725	nA
T_{amb}	ambient temperature	operating	–40	-	+125	°C
T_{stg}	storage temperature		–65	-	+150	°C

2. Pinning information

2.1 Pinning

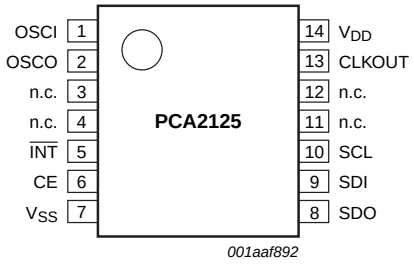


Fig 1. Pin configuration TSSOP14

2.2 Pin description

Table 2. Pin description PCA2125

Symbol	Pin	Description
OSCI	1	oscillator input
OSCO	2	oscillator output
nc	3	Do not connect and do not use as feed through. Connect to V_{DD} if floating pins not allowed.
nc	4	Do not connect and do not use as feed through. Connect to V_{DD} if floating pins not allowed.
$\overline{INT}$	5	interrupt output (open-drain; active LOW). When not used, must be connected to V_{SS} or pulled high via a resistor.
CE	6	chip enable input (active HIGH) with 200 kΩ pull down.
V_{SS}	7	ground
SDO	8	serial data output, push-pull
SDI	9	serial data input. May float when CE inactive.
SCL	10	serial clock input. May float when CE inactive.
nc	11	Do not connect and do not use as feed through. Connect to V_{DD} if floating pins not allowed.

Table 2. Pin description PCA2125

Symbol	Pin	Description
nc	12	Do not connect and do not use as feed through. Connect to V_{DD} if floating pins not allowed.
CLKOUT	13	clock output (open drain)
V_{DD}	14	positive supply voltage

3. Ordering information

Table 3. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA2125TS	PCA2125	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4mm	SOT402-1

4. Block diagram

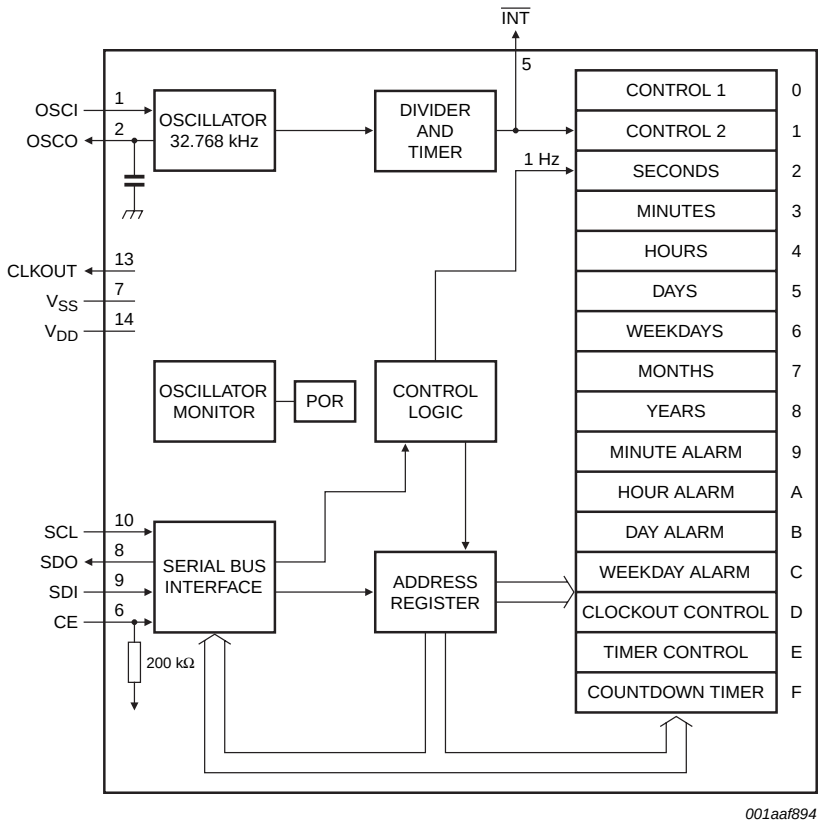


Fig 2. Block diagram of PCA2125

5. Device protection diagram

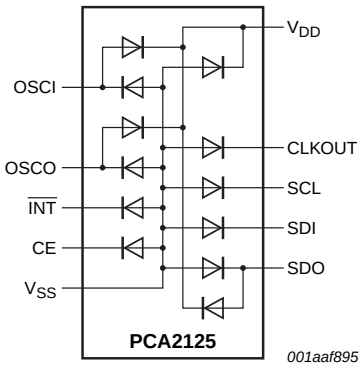


Fig 3. Device diode protection diagram PCA2125

6. Functional description

The PCA2125 contains sixteen 8-bit registers with an auto-incrementing address register, and on-chip 32.768 kHz oscillator with one integrated capacitor, a frequency divider which provides the source clock for the Real Time Clock (RTC), a programmable clock output, and an 8 MHz SPI.

All sixteen registers are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00H and 01H) are used as control registers. The memory addresses 02H through 08H are used as counters for the clock function (seconds up to years). Addresses 09H through 0CH define the alarm condition, whilst address 0DH defines the clock out mode.

The seconds, minutes, hours, days, weekdays, months and years registers are all coded in BCD format. When one of the RTC registers is read the contents of all counters are frozen. Therefore, faulty reading of the clock/calendar during a carry condition is prevented.

Address registers 0EH and 0FH are used for the countdown timer function. The countdown timer has four selectable source clocks allowing for countdown periods in the range from less than 1ms to more than 4hours. There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute, but these are defined at address 01H.

Table 4: Countdown timer durations

Timer source clock	minimum timer duration	maximum timer duration
4096 Hz	244 µs	62.256 ms
64 Hz	15.625 ms	3.984 s
1 Hz	1 s	255 s
1⁄60 Hz	60 s	4 hrs 15 minutes

6.1 Register overview

16 registers are available. The time registers are encoded in the binary coded decimal format (BCD) to simplify application use. Other registers are either bit-wise or standard binary.

Table 5: Registers overview

Bit positions labelled as x are not implemented and will return a 0 when read. Bit positions labelled with 0 should always be written with logic 0.

Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00_{HEX}	control 1	ext test	0	stop	0	POR ovrd	12/24	0	0
01_{HEX}	control 2	MI	SI	MSF	TI/TP	AF	TF	AIE	TIE
02_{HEX}	seconds	RF	10 seconds			seconds			
03_{HEX}	minutes	x	10 minutes			minutes			
04_{HEX}	hours	x	x	AMPM / 10 hours		hours			
05_{HEX}	days	x	x	10 days		days			
06_{HEX}	weekdays	x	x	x	x	x	weekdays		
07_{HEX}	months	x	x	x	10months	months			
08_{HEX}	years	10 years				years			
09_{HEX}	minute alarm	AEn	10 minute alarm			minute alarm			
$0A_{HEX}$	hour alarm	AEn	x	AMPM / 10 hour alarm		hour alarm			
$0B_{HEX}$	day alarm	AEn	x	10 day alarm		day alarm			
$0C_{HEX}$	weekday alarm	AEn	x	x	x	x	weekday alarm		
$0D_{HEX}$	CLKOUT control	x	x	x	x	x	COF2	COF1	COF0
$0E_{HEX}$	timer control	TE	x	x	x	x	x	CTD1	CTD0
$0F_{HEX}$	countdown timer	countdown timer value, n							

6.2 Reset

The PCA2125 includes an internal reset circuit (see Figure 4) which is active whenever the oscillator is stopped. The oscillator may be stopped, for example, by grounding one of the oscillator pins, OSCI or OSCO. The oscillator is also considered to be stopped during the time between power-up and stable crystal resonance. This time may be in the range of 200ms to 2s depending on crystal type, temperature and supply voltage. Whenever an internal reset occurs, the RF flag is set.

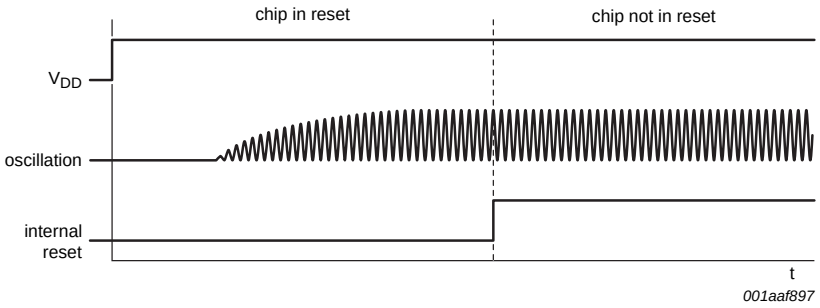


Fig 4. Power on reset

The SPI interface is initialized whenever the chip enable line CE is inactive.

Table 6: Register reset value

Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00_{HEX}	control 1	0	0	0	-	1	0	0	0
01_{HEX}	control 2	0	0	0	0	0	0	0	0
02_{HEX}	seconds	1	x	x	x	x	x	x	x
03_{HEX}	minutes	-	x	x	x	x	x	x	x
04_{HEX}	hours	-	-	x	x	x	x	x	x
05_{HEX}	days	-	-	x	x	x	x	x	x
06_{HEX}	weekdays	-	-	-	-	-	x	x	x
07_{HEX}	months	-	-	-	x	x	x	x	x
08_{HEX}	years	x	x	x	x	x	x	x	x
09_{HEX}	minute alarm	1	x	x	x	x	x	x	x
$0A_{HEX}$	hour alarm	1	-	x	x	x	x	x	x
$0B_{HEX}$	day alarm	1	-	x	x	x	x	x	x
$0C_{HEX}$	weekday alarm	1	-	-	-	-	x	x	x
$0D_{HEX}$	CLKOUT control	-	-	-	-	-	0	0	0
$0E_{HEX}$	timer control	0	-	-	-	-	-	1	1
$0F_{HEX}$	countdown timer	x	x	x	x	x	x	x	x

[1] registers marked ‘x’ are undefined at power up and unchanged by subsequent resets.

[2] registers marked ‘-’ are not implemented.

After reset, the following mode is entered:

32768Hz CLKOUT active

Power on reset override available to be set

24 hour mode is selected

6.2.1 Power-On Reset (POR) override

The power on reset duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up on-board test of the device (see Figure 5).

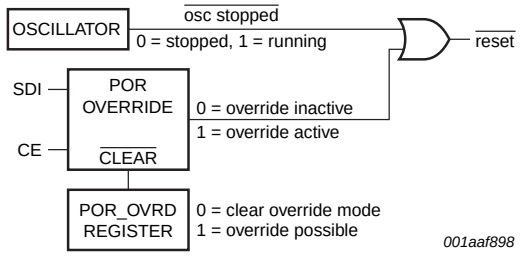


Fig 5. Reset system.

The setting of this mode requires that the 'POR ovrd' register be set to '1' and that the SPI bus pins, SDI and CE, be toggled in a specific order as shown in Figure 6. All timings are required minimums.

Once the override mode has been entered, the device immediately stops being reset and set-up operation may commence i.e. entry into the external clock test mode via the SPI bus access. The override mode may be cleared by writing a logic 0 to 'POR ovrd'. 'POR ovrd' must be set to logic 1 before re-entry into the override mode is possible. Setting 'POR ovrd' to logic 0 during normal operation has no effect except to prevent accidental entry into the POR override mode. This is the recommended setting.

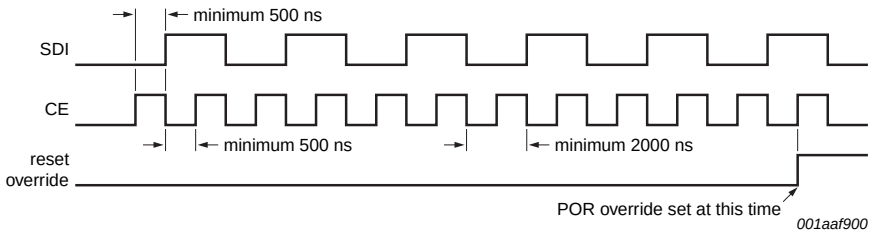


Fig 6. POR override sequence.

6.3 Control registers

6.3.1 Control 1 register

Table 7. Control 1 (address 00_{HEX}) bits description

Bit	Symbol	Value	Description	Section
7	ext test	0	normal mode	Section 6.9
		1	external clock test mode	
6		0	Reserved for future use.	
5	stop	0	RTC source clock runs	Section 6.10
		1	RTC divider chain flip-flops are asynchronously set to logic 0; the RTC clock is stopped (CLKOUT at 32.768, 16.384 or 8.192 kHz is still available)	
4		0	Reserved for future use.	
3	POR ovrd	0	Power-on reset override facility is disabled; set to logic 0 for normal operation	Section 6.2.1
		1	Power-on reset override may be enabled	
2	12/24	0	24 hour mode is selected	Table 15
		1	12 hour mode is selected	
1 to 0		0 0	Reserved for future use.	

6.3.2 Control 2 register

Table 8. Control 2 (address 01_{HEX}) bits description

Bit	Symbol	Value	Description	Section
7	MI	0	Minute interrupt is disabled	Section 6.6.1
		1	Minute interrupt is enabled	
6	SI	0	Second interrupt is disabled	
		1	Second interrupt is enabled	
5	MSF	0	No minute or second interrupt generated	Section 6.6
		1	Flag set when minute or second interrupt generated. Flag must be cleared to clear interrupt.	
2	TF	0	No countdown timer interrupt generated	
		1	Flag set when countdown timer interrupt generated. Flag must be cleared to clear interrupt.	
4	TI/TP	0	Interrupt pin follows timer flags	Section 6.7.2
		1	Interrupt pin generates a pulse	
3	AF	0	No alarm interrupt generated	Section 6.5.1
		1	Flag set when alarm triggered. Flag must be cleared to clear interrupt.	
1	AIE	0	No interrupt generated from the alarm flag	Section 6.7.3
		1	Interrupt generated when alarm flag set	
0	TIE	0	No interrupt generated from the countdown timer flag	Section 6.7
		1	Interrupt generated when countdown timer flag set	

6.4 Time and date function

The majority of these registers are coded in the Binary Coded Decimal format. BCD is used to simplify application use.

An example is shown for the minutes register:

Table 9: BCD example

Minutes value in decimal	Bit 7 2^3	Bit 6 2^2	Bit 5 2^1	Bit 4 2^0	Bit 3 2^3	Bit 2 2^2	Bit 1 2^1	Bit 0 2^0
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	1
02	0	0	0	0	0	0	1	0
:								
09	0	0	0	0	1	0	0	1
10	0	0	0	1	0	0	0	0
:								
58	0	1	0	1	1	0	0	0
59	0	1	0	1	1	0	0	1

Table 10. Seconds / RF (address 02_{HEX}) bits description

Bit	Symbol	Value	Description
7	RF	0	clock integrity is guaranteed
		1	clock integrity is not guaranteed. Chip reset has occurred since flag was last cleared
6 to 0	seconds	00 to 59	this register holds the current seconds coded in BCD format;

Table 11. Minutes (address 03_{HEX}) bits description

Bit	Symbol	Value	Description
6 to 0	minutes	00 to 59	this register holds the current minutes coded in BCD format

Table 12. Hours (address 04_{HEX}) bits description

Bit	Symbol	Value	Description
12 hour mode		[1]	
5	AMPM	0	Indicates AM
		1	Indicates PM
4 to 0	hours	00 to012	this register holds the current hours coded in BCD format for 12 hour mode
24 hour mode		[1]	
5 to 0	hours	00 to 23	this register holds the current hours coded in BCD format for 24 hour mode

[1] Hour mode is set by the 12 / 24 bit in control register 2.

Table 13. Days (address 05_{HEX}) bits description

Bit	Symbol	Value		Description
5 to 0	days	01 to 31	[1]	this register holds the current day coded in BCD format

[1] The RTC compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

Table 14. Weekdays (address 06_{HEX}) bits description

Bit	Symbol	Value		Description
2 to 0	weekdays	0 to 6	[1]	this register holds the current weekday, see Table 15

[1] These bits may be re-assigned by the user.

Although the association of the weekdays counter to the actual weekday is arbitrary, the PCA2125 will assume ‘Sunday’ is 000 and ‘Monday’ is 001 for the purposes of determining the increment for calendar weeks.

Table 15: Weekday assignments

Day	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sunday	x	x	x	x	x	0	0	0
Monday	x	x	x	x	x	0	0	1
Tuesday	x	x	x	x	x	0	1	0
Wednesday	x	x	x	x	x	0	1	1
Thursday	x	x	x	x	x	1	0	0
Friday	x	x	x	x	x	1	0	1
Saturday	x	x	x	x	x	1	1	0

Table 16. Months (address 07_{HEX}) bits description

Bit	Symbol	Value	Description
4 to 0	month	01 to 12	this register holds the current month coded in BCD format, see Table 17

Table 17: Month assignments

Month	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	x	x	x	0	0	0	0	1
February	x	x	x	0	0	0	1	0
March	x	x	x	0	0	0	1	1
April	x	x	x	0	0	1	0	0
May	x	x	x	0	0	1	0	1
June	x	x	x	0	0	1	1	0
July	x	x	x	0	0	1	1	1
August	x	x	x	0	1	0	0	0
September	x	x	x	0	1	0	0	1
October	x	x	x	1	0	0	0	0
November	x	x	x	1	0	0	0	1
December	x	x	x	1	0	0	1	0

Table 18. Years (address 08_{HEX}) bits description

Bit	Symbol	Value	Description
7 to 0	years	00 to 99	this register holds the current year coded in BCD format

6.4.1 Data flow

Figure 7 shows the data flow and data dependencies starting from the 1 Hz clock tick.

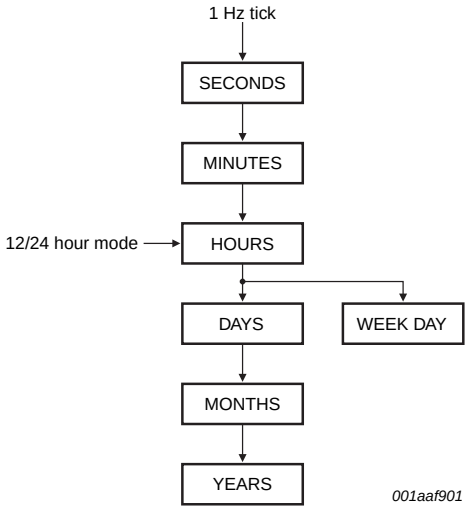


Fig 7. Data flow for the time function

6.5 Alarm function

When one or more of these registers are loaded with a valid minute, hour, day or weekday and its corresponding bit Alarm Enable not (AEn) is logic 0, then that information will be compared with the current minute, hour, day and weekday.

Table 19. Minute alarm (address 09_{HEX}) bits description

Bit	Symbol	Value	Description
7	AEn	0	minute alarm is enabled
		1	minute alarm is disabled
6 to 0	minute alarm	00 to 59	this register holds the minute alarm information coded in BCD format

Table 20. Hour alarm (address $0A_{HEX}$) bits description

Bit	Symbol	Value	Description
7	AEn	0	hour alarm is enabled
		1	hour alarm is disabled
24 hour mode			

Table 20. Hour alarm (address $0A_{HEX}$) bits description

Bit	Symbol	Value	Description
5 to 0	hour alarm	00 to 23	this register holds the hour alarm information coded in BCD format when in 24 hour mode.
12 hour mode			
5	am/pm alarm	0 to 1	this register holds the hour alarm information coded in BCD format when in 12 hour mode
4 to 0	hour alarm	00 to 11	

Table 21. Day alarm (address $0B_{HEX}$) bits description

Bit	Symbol	Value	Description
7	AEn	0	day alarm is enabled
		1	day alarm is disabled
5 to 0	day alarm	01 to 31	this register holds the day alarm information coded in BCD format

Table 22. Weekday alarm (address $0C_{HEX}$) bits description

Bit	Symbol	Value	Description
7	AEn	0	weekday alarm is enabled
		1	weekday alarm is disabled
2 to 0	weekday alarm	0 to 6	this register holds the weekday alarm information

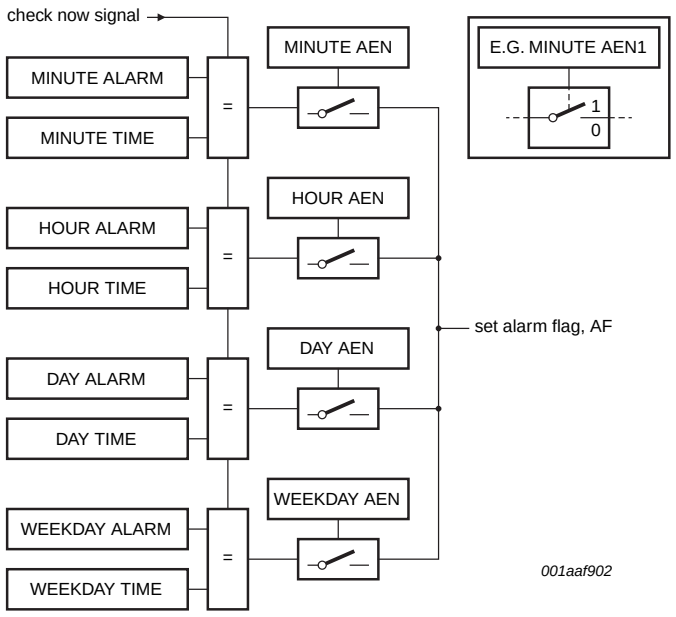


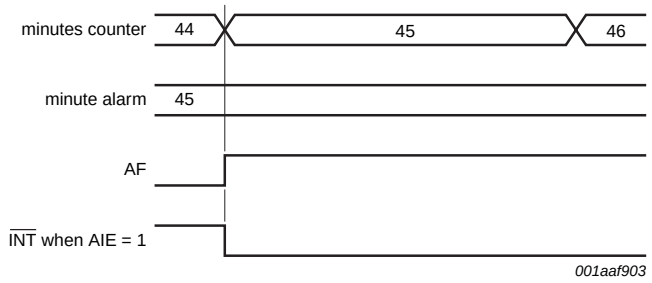
Fig 8. Alarm function block diagram

Generation of interrupts from the alarm function is described under the interrupt section, Section 6.7.3.

6.5.1 Alarm flag

When all enabled comparisons first match, the Alarm Flag (AF) is set. AF will remain set until cleared by software. Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their bit AEn at logic 1 are ignored.

Figure 9 shows an example for clearing AF but leaving MSF and TF unaffected. Clearing the flags is made by a write command, therefore bits 7,6,4,1 and 0 must be written with their previous values. Repeatedly re-writing these bits has no influence on the functional behavior.



Example where only the minute alarm is used and no other interrupts are enabled.

Fig 9. AF timing

To prevent the timer flags being overwritten while clearing AF, a logic AND is performed during a write access. Writing a '1' will cause the flag to maintain it's value, whilst writing a '0' will cause the flag to be reset.

Table 23: Flag location in control 2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control 2	-	-	MSF	-	AF	TF	-	-

The following tables show what instruction must be sent to clear the AF. In this example, MSF and TF are unaffected.

Table 24: Example to clear only TF (bit 2)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control 2	-	-	1	-	0	1	-	-

6.6 Timer functions

The countdown timer has four selectable source clocks allowing for countdown periods in the range from less than 1ms to more than 4hours. There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute.

Address registers 01_{HEX}, $0E_{HEX}$ and $0F_{HEX}$ are used to control the timer function and output.

Table 25. Control 2 (address 01_{HEX}) bits description

Bit	Symbol	Value	Description
7	MI	0	Minute interrupt is disabled
		1	Minute interrupt is enabled
6	SI	0	Second interrupt is disabled
		1	Second interrupt is enabled
5	MSF	0	No minute or second interrupt generated
		1	Flag set when minute or second interrupt generated. Flag must be cleared to release $\overline{INT}$.
4	TI/TP	0	Interrupt pin follows timer flags
		1	Interrupt pin generates a pulse
2	TF	0	No countdown timer interrupt generated
		1	Flag set when countdown timer interrupt generated. Flag must be cleared to release $\overline{INT}$.
0	TIE	0	No interrupt generated from the countdown timer flag
		1	Interrupt generated when countdown timer flag set
3	AF		See Table 8.
1	AIE		See Table 8.

Table 26. Timer control (address $0E_{HEX}$) bits description

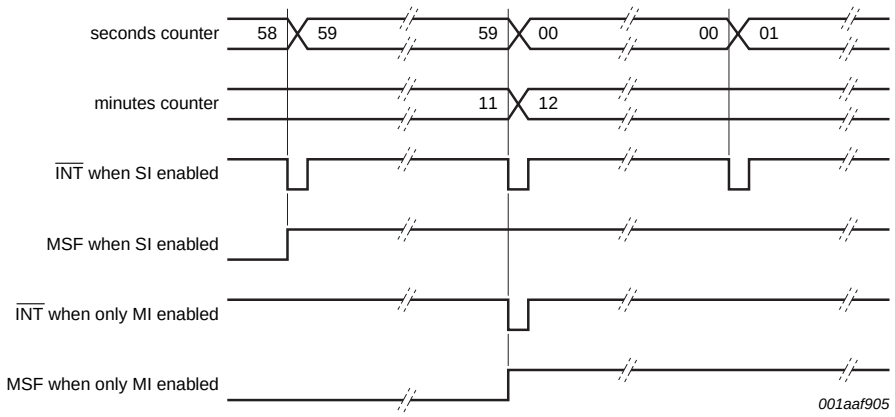
Bit	Symbol	Value	Description	Section
6:2	0		Reserved for future use.	
7	TE	0	Countdown timer is disabled	Section 6.6.2
		1	Countdown timer is enabled	
1 to 0	CDT	0 0	4096 Hz countdown timer source clock	
		0 1	64 Hz countdown timer source clock	
		1 0	1 Hz countdown timer source clock	
		1 1	1⁄60 Hz countdown timer source clock	

Table 27. Countdown timer (address $0A_{HEX}$) bits description

Bit	Symbol	Value	Description	Section
7 to 0	n	00 to FF	countdown value = n; $CountdownPeriod = \frac{n}{SourceClockFrequency}$	Section 6.6.2

6.6.1 Second and minute interrupt; SI, MI

The minute and second interrupt are pre-defined timers for generating periodic interrupts. The timers can be enabled independently from one another, however a minute interrupt enabled on top of a second interrupt will not be distinguishable since it will occur at the same time; see Figure 10.



In this example, TI/TP is set to 1 resulting in $^{1}/_{64}$ Hz wide interrupt pulse and the MSF flag is not cleared after an interrupt.

Fig 10. INT example for SI and MI

Table 28. Effect of MI and SI on INT generation

Minute interrupt, MI	Second interrupt, SI	Result
disabled	disabled	No interrupt generated
enabled	disabled	An interrupt once per minute
disabled	enabled	An interrupt once per second
enabled	enabled	An interrupt once per second

The minute/second flag, MSF, is set to '1' when either the seconds or the minutes counter increments according to the currently enabled interrupt. The flag can be read and cleared by the interface. The status of the MSF does not affect INT pulse generation. If the MSF flag is not cleared prior to the next coming interrupt period, an INT pulse will still be generated.

The purpose of the flag is to allow the controlling system to interrogate the PCA2125 and identify the source of the interrupt i.e. minute/second or countdown timer.

Table 29: Effect of MI and SI on MSF

Minute interrupt, MI	Second interrupt, SI	Result
disabled	disabled	MSF never set.
enabled	disabled	MSF set when minutes counter increments
disabled	enabled	MSF set when seconds counter increments
enabled	enabled	MSF set when seconds counter increments

6.6.2 Countdown timer function

The 8-bit countdown timer at address $0F_{HEX}$ is controlled by the timer control register at address $0E_{HEX}$. The timer control register determines one of 4 source clock frequencies for the timer (4096 Hz, 64 Hz, 1 Hz, or $1/60$ Hz), and enables or disables the timer.

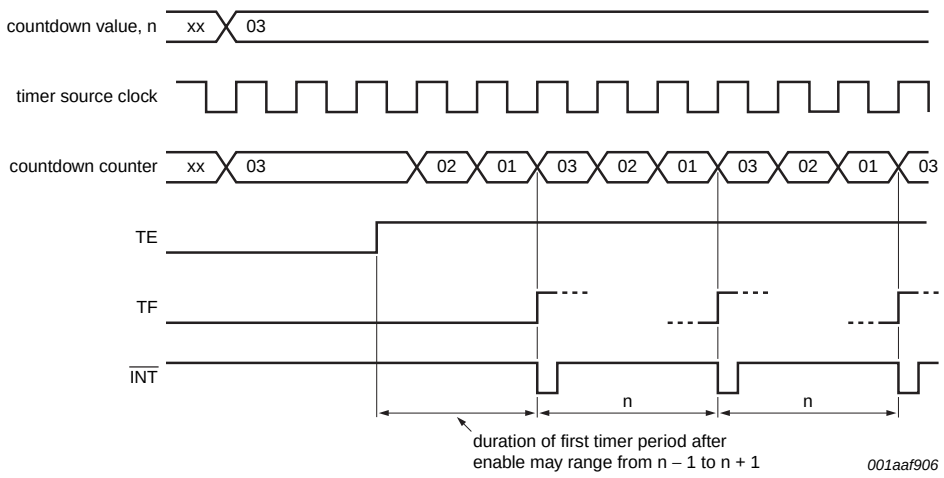
Table 30. CDT1 and CDTD: Timer frequency selection

CDT1	CDT0	TIMER Source clock frequency [1]	delay for n = 1	delay for n = 255
0	0	4096 Hz	244 µs	62.256 ms
0	1	64 Hz	15.625 ms	3.984 s
1	0	1 Hz	1 s	255 s
1	1	1/60 Hz	60 s	4 hrs 15 min

[1] When not in use, CDT must be set to $1/60$ Hz for power saving.

Remark: Note that all timings which are generated from the 32.768kHz oscillator are based on the assumption that there is 0 ppm deviation. Deviation in oscillator frequency will result in deviation in timings. This is not applicable to interface timing.

The timer counts down from a software-loaded 8-bit binary value, n. Loading the counter with 0 effectively stops the timer. Values from 1 to 255 are valid. When the counter reaches 1, the countdown Timer Flag (TF) will be set and the counter automatically re-loads and starts the next timer period. Reading the timer will return the current value of the countdown counter (see Figure 11)..



In the example it is assumed that the timer flag is cleared before the next countdown period expires and that the $\overline{INT}$ is set to pulsed mode.

Fig 11. General countdown timer behavior

If a new value of n is written before the end of the current timer period, then this value will take immediate effect. NXP does not recommend to changing n without first disabling the counter (by setting TE = 0). The update of n is asynchronous to the timer clock, therefore changing it without setting TE = 0 will result in a corrupted value loaded into the

countdown counter which results an undetermined countdown period for the first period. The countdown value n will however be correctly stored and correctly loaded on subsequent timer periods.

When the countdown timer flag is set, an interrupt signal on $\overline{INT}$ will be generated provided that this mode is enabled. See Section 6.7.2 for details on how the interrupt can be controlled.

When starting the timer for the first time, the first period will have an uncertainty which is a result of the enable instruction being generated from the interface clock which is asynchronous from the timer source clock. Subsequent timer periods will have no such delay. The amount of delay for the first timer period will depend on the chosen source clock, see Table 31.

Table 31: First period delay for timer counter value, n.

Timer source clock	minimum timer period	maximum timer period
4096 Hz	n	n + 1
64 Hz	n	n + 1
1 Hz	(n-1) + 1/64Hz	n + 1/64Hz
1/60 Hz	(n-1) + 1/64Hz	n + 1/64Hz

At the end of every countdown, the timer sets the countdown Timer Flag (TF). The TF may only be cleared by software. The asserted TF can be used to generate an interrupt ($\overline{INT}$). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of TF. Bit TI/TP is used to control this mode selection and the interrupt output may be disabled with the TIE bit, see Table 25.

When reading the timer, the current countdown value is returned and not the initial value, n. For accurate read back of the countdown value, the SPI bus clock (SCL) must be operating at a frequency of at least twice the selected timer clock. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

6.6.3 Timer flags

When a minute or second interrupt occurs, MSF is set to 1. Similarly, at the end of a timer countdown, TF is set to 1. These bits maintain their value until overwritten by software. If both countdown timer and minute/second interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another a logic AND is performed during a write access. Writing a ‘1’ will cause the flag to maintain it’s value, whilst writing a ‘0’ will cause the flag to be reset.

Three examples are given for clearing the flags. Clearing the flags is made by a write command, therefore bits 7,6,4,1 and 0 must be written with their previous values. Repeatedly re-writing these bits has no influence on the functional behavior.

Table 32: Flag location in control 2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control 2	-	-	MSF	-	AF	TF	-	-

The following tables show what instruction must be sent to clear the appropriate flag.

Table 33: Example to clear only TF (bit 2)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control 2	-	-	1	-	1	0	-	-

Table 34: Example to clear only MSF (bit 5)

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control 2	-	-	0	-	1	1	-	-

Table 35: Example to clear both TF and MSF

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control 2	-	-	0	-	1	0	-	-

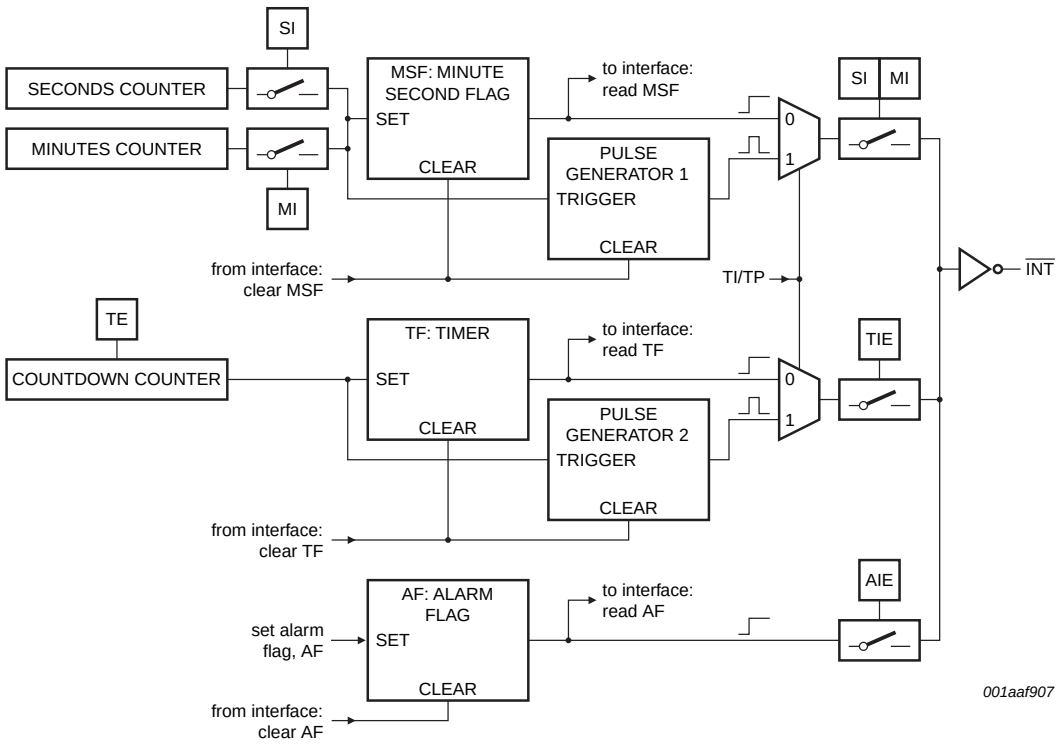
Clearing the alarm flag (AF) operates in exactly the same way, but is described in Section 6.5.1.

6.7 Interrupt output, $\overline{INT}$

An active low interrupt signal is available at pin $\overline{INT}$. Operation is controlled via the bits of control register 2. Interrupts may be sourced from three places; Second/minute timer, countdown timer or alarm function.

With the TI/TP bit, the timer generated interrupts can be configured to either generate a pulse or to follow the status of the interrupt flags; TF and MSF.

Remark: Note that the interrupts from the three groups are wire-OR'd, meaning they will mask one another (see Figure 12).



When SI, MI, TIE and AIE are all disabled, $\overline{INT}$ will remain high impedance.

Fig 12. Interrupt scheme

6.7.1 Minute/Second interrupts

The pulse generator for the minute/second interrupt operates from an internal 64 Hz clock and consequently generates a pulse of $^1/_{64}$ seconds in duration.

If the MSF flag is clear before the end of the $\overline{INT}$ pulse, then the $\overline{INT}$ pulse is shortened. This allows the source of a system interrupt to be cleared immediately it is serviced i.e. the system does not have to wait for the completion of the pulse before continuing; see Figure 13. Instructions for clearing MSF can be found in Section 6.6.3.

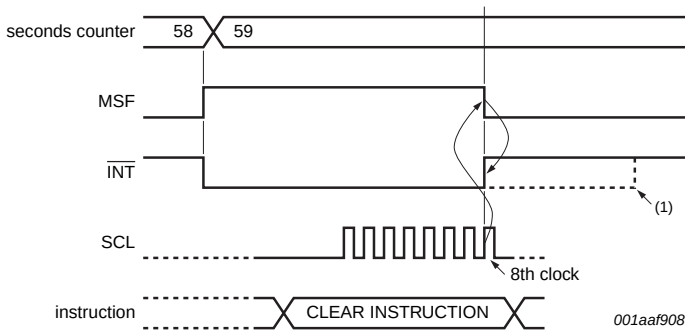


Fig 13. Example of shortening the $\overline{\text{INT}}$ pulse by clearing the MSF flag.

The timing shown for clearing MSF in Figure 13 is also valid for the non-pulsed interrupt mode i.e. when TI/TP = 0, where the pulse may be shortened by setting both MI and SI to '0'.

6.7.2 Countdown timer interrupts

Generation of interrupts from the countdown timer is controlled via the TIE bit (see Table 25).

The pulse generator for the countdown timer interrupt also uses an internal clock, but this time it is dependent on the selected source clock for the countdown timer and on the countdown value, n. As a consequence, the width of the interrupt pulse varies (see Table 36).

Table 36. $\overline{\text{INT}}$ operation (bit TI / TP = 1)

Source clock (Hz)	$\overline{\text{INT}}$ period (s)	
	n = 1 [1]	n > 1
4096	1⁄8192	1⁄4096
64	1⁄128	1⁄64
1	1⁄64	1⁄64
1⁄60	1⁄64	1⁄64

[1] n = loaded countdown value. Timer stopped when n = 0.

If the TF flag is clear before the end of the $\overline{\text{INT}}$ pulse, then the $\overline{\text{INT}}$ pulse is shortened. This allows the source of a system interrupt to be cleared immediately it is serviced i.e. the system does not have to wait for the completion of the pulse before continuing (see Figure 14). Instructions for clearing MSF can be found in Section 6.6.3.

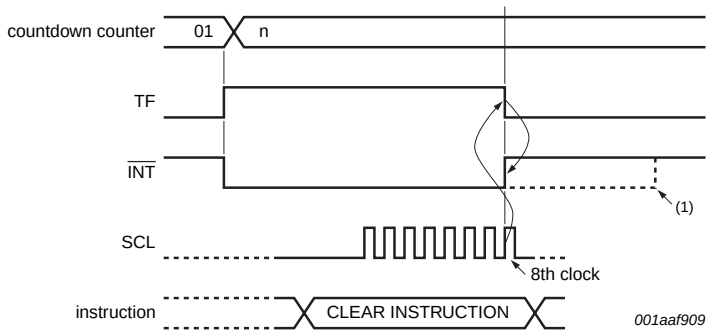
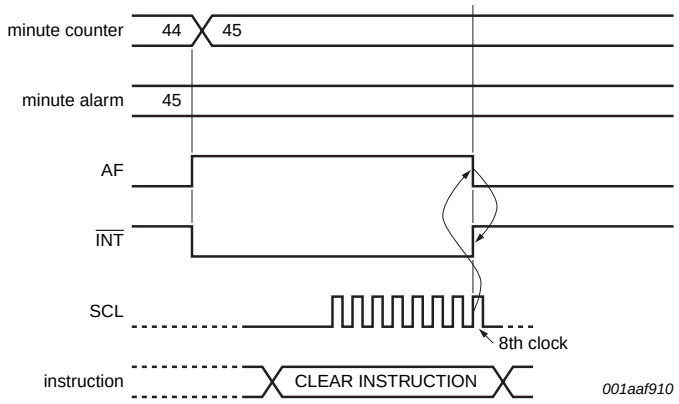


Fig 14. Example of shortening the $\overline{INT}$ pulse by clearing the TF flag.

The timing shown for clearing TF in Figure 14 is also valid for the non-pulsed interrupt mode i.e. when TI/TP = 0, where the pulse may be shortened by setting TIE to '0'.

6.7.3 Alarm interrupts

Generation of interrupts from the alarm function is controlled via the AIE bit (see Table 8). If AIE is enabled, the $\overline{INT}$ pin follows the status of AF. Clearing AF will immediately clear $\overline{INT}$. No pulse generation is possible for alarm interrupts (see Figure 15).



Example where only the minute alarm is used and no other interrupts are enabled.

Fig 15. AF timing

6.8 Clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by the COF control bits in the control register. Frequencies of 32.768 kHz (default) down to 1Hz can be generated for use as a system clock, micro-controller clock, input to a charge pump, or for calibration of the oscillator.

CLKOUT is an open drain output and enabled at power-on. When disabled the output is high impedance (Hi-Z).

The duty cycle of the selected clock is not controlled however, due to the nature of the clock generation, all but the 32.768kHz frequencies will be 50:50.

The ‘stop’ function can also affect the CLKOUT signal, depending on the selected frequency. When ‘stop’ is active, the CLKOUT pin will generate a continuous 0 for those frequencies that can be stopped. For more details see Section 6.10.

Table 37: CLKOUT frequency selection

COF[2:0]			CLKOUT FREQUENCY, Hz	Typical duty cycle High% : Low%	Effect of ‘stop’
0	0	0	32768	60:40 to 40:60	No effect
0	0	1	16384	50:50	No effect
0	1	0	8192	50:50	No effect
0	1	1	4096	50:50	CLKOUT = 0
1	0	0	2048	50:50	CLKOUT = 0
1	0	1	1024	50:50	CLKOUT = 0
1	1	0	1	50:50	CLKOUT = 0
1	1	1	CLKOUT = 0		

6.9 External clock test mode

A test mode is available which allows for on-board testing. In such a mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit ‘ext test’ in control/status1 register. Then pin CLKOUT becomes an input. The test mode replaces the internal signal with the signal applied to pin CLKOUT. Every 64 positive edges applied to pin CLKOUT generates an increment of one second.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a minimum period of 1000 ns. The internal clock, now sourced from CLKOUT, is divided down to 1 Hz by a 26 divide chain called a pre-scaler. The pre-scaler can be set into a known state by using bit ‘stop’. When bit ‘stop’ is set, the pre-scaler is reset to 0 (stop must be cleared before the pre-scaler can operate again).

From a stop condition, the first 1 second increment will take place after 32 positive edges on CLKOUT. Thereafter, every 64 positive edges will cause a 1 second increment.

Remark: Entry into EXT_CLK test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the pre-scaler can be made.

Operation example:

1. Set ‘ext test’ test mode (control/status 1, bit ‘ext test’ = 1)
2. Set stop (control/status 1, bit stop = 1)
3. Clear stop (control/status 1, bit stop = 0)
4. Set time registers to desired value
5. Apply 32 clock pulses to CLKOUT
6. Read time registers to see the first change
7. Apply 64 clock pulses to CLKOUT
8. Read time registers to see the second change.

Repeat 7 and 8 for additional increments.

6.10 'stop' bit function

The function of the stop bit is to allow for accurate starting of the time circuits. The stop function will cause the upper part of the pre-scaler, F2 to F14, to be held in reset and thus no 1Hz ticks will be generated. The time circuits can then be set and will not increment until the stop is released. (see Figure 16).

Stop will not affect the output of 32768 Hz, 16384 Hz or 8192 Hz (see Section 6.8).

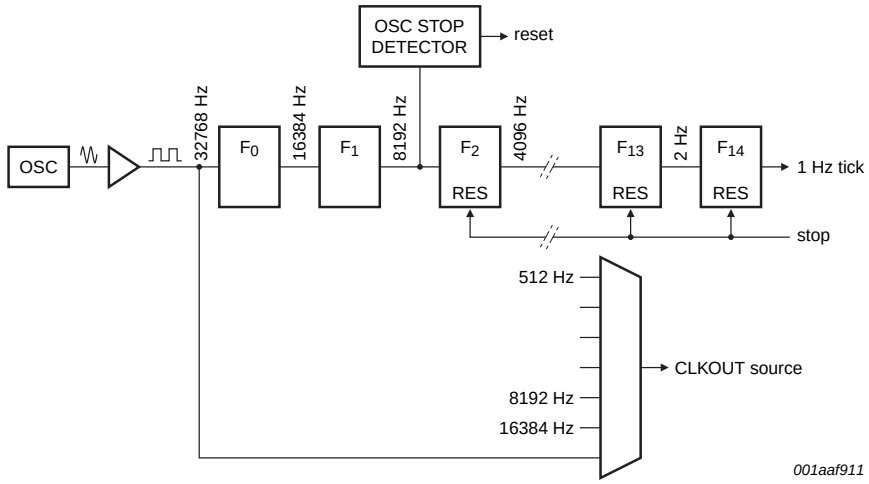


Fig 16. stop bit

The lower two stages of the pre-scaler, F_0 and F_1, are not reset and because the SPI interface is asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits will be between 0 and one 8192Hz cycle (see Figure 17).

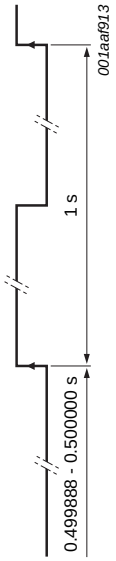
Fig 17. stop bit release timing

The first increment of the time circuits is between 0.499888 s and 0.500000 s after stop is released. The uncertainty is caused by the pre-scaler bits F_0 and F_1 not being reset (see Table 38).

Table 38. First increment of time circuits after stop release

Stop	Pre-scaler F_0F_1, F_2 to F_{14} [1]	1Hz tick	Time HH:MM:SS	Comment
Clock is running normally.				
0	01-0000111010100			Pre-scaler counting normally
Stop is activated by user. F_0F_1 are not reset and values can not be predicted externally.				
1	xx-0000000000000		12:45:12	Pre-scaler is reset. Time circuits are frozen.

Table 38. First increment of time circuits after stop release

Stop	Pre-scaler F_0F_1, F_2 to F_{14} [1]	1Hz tick	Time HH:MM:SS	Comment
New time is set by user.				
1	xx-0000000000000		08:00:00	Pre-scaler is reset. Time circuits are frozen.
Stop is released by user.				
0	xx-0000000000000		08:00:00	Pre-scaler is now running.
0	xx-1000000000000		08:00:00	
0	xx-0100000000000		08:00:00	
0	xx-1100000000000		08:00:00	
:	:		:	
0	11-1111111111110		08:00:00	
0	00-0000000000001		08:00:01	0 to 1 transition of F14 increments the time circuits.
0	10-0000000000001		08:00:01	
:	:		:	
0	11-1111111111111		08:00:01	
0	00-0000000000000		08:00:01	
:	:		:	
0	11-1111111111110		08:00:01	
0	00-0000000000001		08:00:02	0 to 1 transition of F14 increments the time circuits.

[1] F_0 is clocked at 32768 Hz.

6.11 3-line Serial Interface

Data transfer to and from the device is made via a 3 wire SPI interface. The data lines for input and output are split to allow for alternative system wiring. The data input and output line can be connected together to facilitate a bi-directional databus. The chip enable signal is used to identify the transmitted data. Each data transfer is a byte, with the MSB sent first (see Figure 18).

Table 39. Serial interface

Symbol	Function		Description
CE	chip enable input; active high	[1]	When inactive, the interface is reset. Pull-down resistor included. Input may be higher than V_{DD}.
SCL	serial clock input		When CE is inactive, input may float. Input may be higher than V_{DD}.
SDI	serial data input		When CE is inactive, input may float. Input may be higher than V_{DD}. Input data is sampled on the rising edge of SCL.
SDO	serial data output		Push-pull output. Drives from V_{SS} to V_{DD}. Output data is changed on the falling edge of SCL.

[1] Chip enable may not be wired permanently high.

The transmission is controlled by the active high chip enable signal CE. The first byte transmitted is the command byte. Subsequent bytes will be either data to be written or data to be read. Date is captured on the rising edge of the clock and transferred internally on the falling edge.

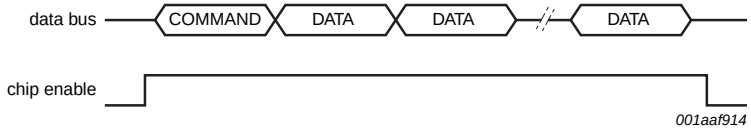


Fig 18. Data transfer overview

The command byte defines the address of the first register to be accessed and the read/write mode. The address counter will auto increment after every access and will reset to zero after the last valid register is accessed. The read/write bit (R/$\overline{W}$) defines if the following bytes will be read or write information.

Table 40: Command byte definition

Bit	Symbol	Value	Description
7	R/$\overline{W}$	0	Data will be write data
		1	Data will be read data
6..4	Sub Address, SA	001	Other codes will cause the device to ignore data transfer.
3..0	Register Address, RA	00_{HEX} to $0F_{HEX}$	Valid address range.

In the following example, the seconds register is set to 45 seconds and the minutes register to 10 minutes (see Figure 19).

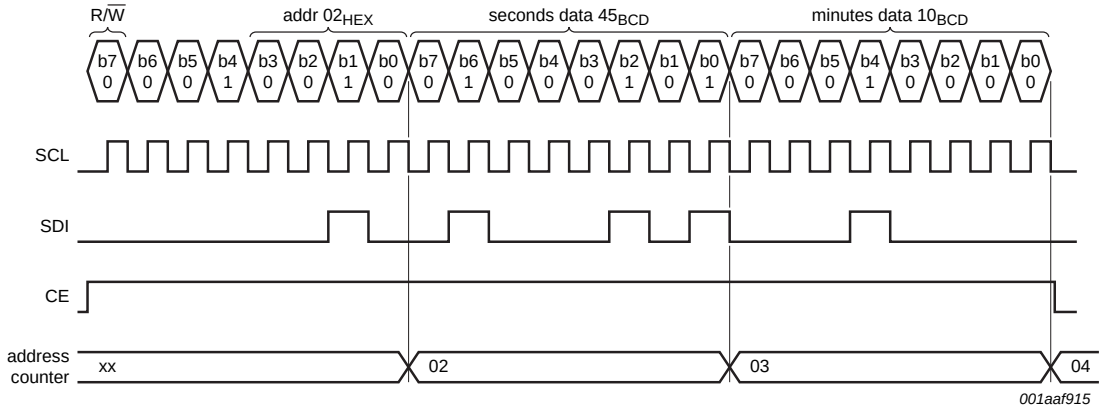


Fig 19. Serial bus write example

In the following example, the months and years registers are read (see Figure 20). In this example, SDI and SDO are not connected together. In this configuration, it is important that SDI is never left floating, it must always be driven either high or low. If SDI is left open, high I_{DD} currents may result.

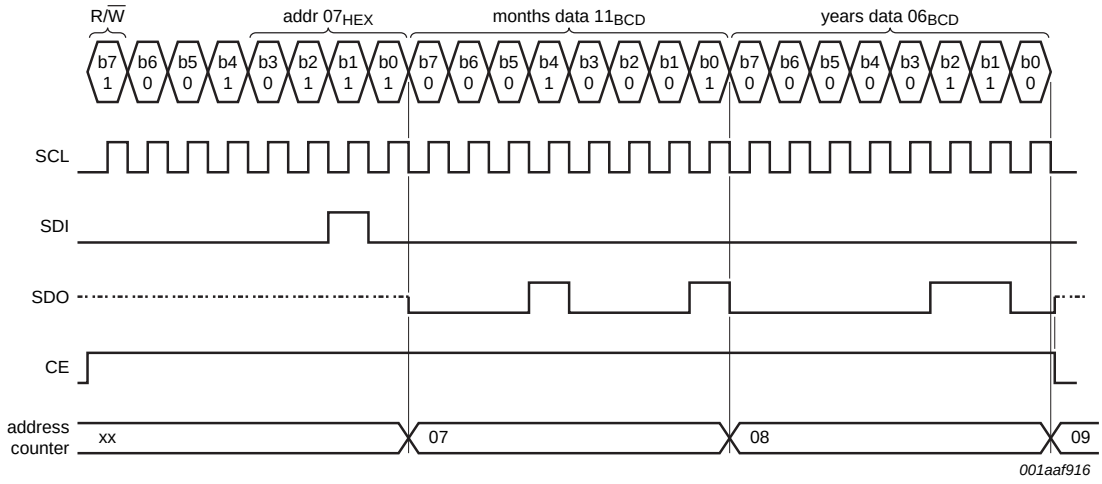


Fig 20. Serial bus read example

7. Limiting values

Table 41: Limiting values *In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Min	Max	Unit
V_{DD}	supply voltage	–0.5	+6.5	V
I_{DD}	supply current	–50	+50	mA
V_I	input voltage	–0.5	+6.5	V
V_O	output voltage	–0.5	+6.5	V
I_I	input current	–10	+10	mA
I_O	output current	–10	+10	mA
P_{tot}	total power dissipation	-	300	mW
T_{amb}	ambient temperature	–40	+125	°C
T_{stg}	storage temperature	–65	+150	°C

7.1 ESD values

- Electrostatic Discharge (ESD) protection exceeds 2000 V Human Body model (HBM) per JESD22-A114, 200 V Machine Model (MM) per JESD22-A115 and 2000 V CHarged Device Model (CDM) per JESD22-C101.
- Latch-up testing is done to JEDEC standard JESD78 which exceeds 100 mA.

8. Static characteristics

Table 42. Static characteristics

V_{DD} = 1.2 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +125 °C; f_{osc} = 32.768 kHz; quartz R_s = 60 kΩ; C_L = 12 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage	SPI bus inactive; T_{amb} = 25 °C	[1]	1.2	-	5.5	V
		SPI bus active; T_{amb} = –40 to 125 °C	[1]	1.6	-	5.5	V
$V_{DDminclock}$	minimum supply voltage for clock data integrity	T_{amb} = 25 °C		-	1.1	-	V
I_{DD1}	supply current 1	SPI bus active					
		f_{SCL} = 7.0 MHz		-	-	800	µA
		f_{SCL} = 1.0 MHz		-	-	200	µA

Table 42. Static characteristics

V_{DD} = 1.2 to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 to +125 °C; f_{osc} = 32.768 kHz; quartz R_s = 60 kΩ; C_L = 12 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DD2}	supply current 2	SPI bus inactive; CLKOUT disabled; (f_{SCL} = 0 Hz); T_{amb} = 25 °C	[2]				
		V_{DD} = 5.0 V		-	550	725	nA
		V_{DD} = 3.0 V		-	550	725	nA
		V_{DD} = 2.0 V		-	550	725	nA
		SPI bus inactive (f_{SCL} = 0 Hz); CLKOUT disabled; T_{amb} = −40 to +125 °C	[2]				
		V_{DD} = 5.0 V		-	-	-	nA
		V_{DD} = 3.0 V		-	680	1000	nA
		V_{DD} = 2.0 V		-	-	-	nA
I_{DD3}	supply current 3	SPI bus inactive (f_{SCL} = 0 Hz); CLKOUT enabled at 32 kHz; T_{amb} = 25 °C					
		V_{DD} = 5.0 V		-	-	-	nA
		V_{DD} = 3.0 V		-	-	-	nA
		V_{DD} = 2.0 V		-	-	-	nA
		SPI bus inactive (f_{SCL} = 0 Hz); CLKOUT enabled at 32 kHz; T_{amb} = −40 to +125 °C					
		V_{DD} = 5.0 V		-	-	-	nA
		V_{DD} = 3.0 V		-	-	-	nA
		V_{DD} = 2.0 V		-	-	-	nA
Inputs							
V_{IL}	LOW-level input voltage			V_{SS}	-	$0.3V_{DD}$	V
V_I	Input voltage	for OSCI pin		-0.5	-	V_{DD}+0.5	V
V_I	Input voltage	for pins CE, SDI, SCL		-0.5	-	5.5	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	V_{DD}	V
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}		−1	0	+1	µA
C_i	input capacitance		[3]	-	-	7	pF
Outputs							
V_O	Output voltage	for pins OSCO and SDO		$0.7V_{DD}$	-	V_{DD}+0.5	V
V_O	Output voltage	for CLKOUT and $\overline{INT}$ (refers to external pull-up voltage)		$0.7V_{DD}$	-	5.5	V
I_{OH}	HIGH-level output current	V_{OH} = 4.6 V; V_{DD} = 5 V		-	-	1.5	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 5 V ($\overline{INT}$ and CLKOUT)		−1.5	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 5 V		−1	-	-	mA
I_{LO}	output leakage current	V_O = V_{DD} or V_{SS}		−1	0	+1	µA
C_{OSCO}	Capacitance on OSCO			-	25	-	pF

[1] For reliable oscillator start at power-up: V_{DD} = $V_{DD(min)}$ + 0.3 V.

[2] Timer source clock = $^1/_{60}$ Hz, level of pins SCE, SDI and SCL is V_{DD} or V_{SS}.

[3] Tested on sample basis.

9. Dynamic characteristics

Table 43. Dynamic characteristics

V_{DD1} = 1.6 to 5.5V; V_{SS} = 0 V; T_{amb} = –40 to +125 °C, f_{CLKOUT} = 32.768 kHz unless otherwise specified. All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

Symbol	Parameter	Conditions	V_{DD} = 1.6V		V_{DD} = 2.7V		V_{DD} = 4.5V		V_{DD} = 5.5V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Serial interface timing characteristics (SPI and serial interface, see Figure 21)											
f_{SCLK}	SCL clock frequency		-	1.89	-	4.76	-	6.25	-	8.0	MHz
t_{SCLK}	SCLK time		530	-	210	-	160	-	125	-	ns
$t_{w(SCLKH)}$	SCLK HIGH pulse width		200	-	100	-	100	-	62.5	-	ns
$t_{w(SCLKL)}$	SCLK LOW pulse width		200	-	100	-	100	-	62.5	-	ns
t_{RF}	SCLK rise and fall time		-	100	-	100	-	100	-	100	ns
t_{CES}	CE setup time		30	-	30	-	30	-	30	-	ns
t_{CEH}	CE hold time		100	-	60	-	40	-	30	-	ns
t_{CER}	CE recovery time		100	-	100	-	100	-	100	-	ns
t_{WCE}	Pulse width CE		-	0.99	-	0.99	-	0.99	-	0.99	s
t_{DS}	SDI setup time		20	-	10	-	10	-	5	-	ns
t_{DH}	SDI hold time		100	-	60	-	40	-	30	-	ns
t_{RD}	SDO read delay time		-	216	-	100	-	75	-	60	ns
t_{RZ}	SDO disable time	No load value. Bus will be help up by bus capacitance. Use RC time constant with application values.	-	50	-	30	-	30	-	25	ns
t_{ZZ}	Bus conflict avoidance time		0	-	0	-	0	-	0	-	ns

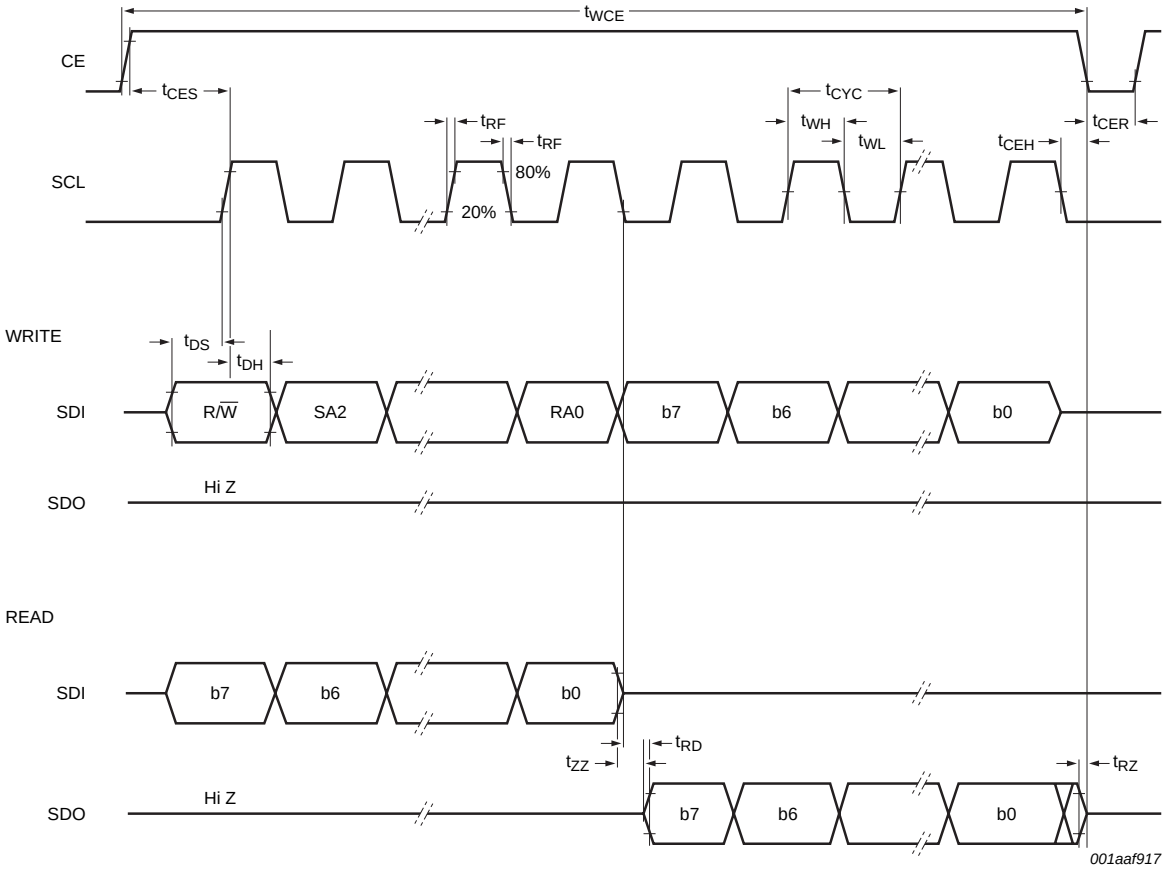
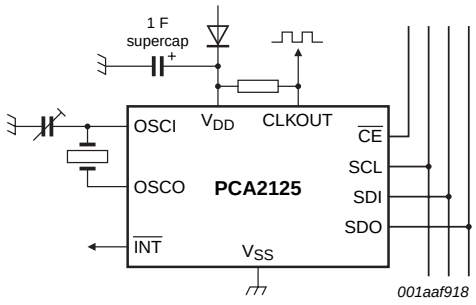


Fig 21. SPI interface timing

10. Application information



The 1 Farad capacitor is used as a standby/back-up supply. With the RTC in its minimum power configuration i.e. timer off and CLKOUT off, the RTC may operate for weeks.

Fig 22. Application diagram.

10.1 Quartz frequency adjustment

10.1.1 Method 1: fixed OSCI capacitor

By evaluating the average capacitance necessary for the application layout, a fixed capacitor can be used (see Figure 22). The frequency is best measured via the 32.768 kHz signal available after power-on at pin CLKOUT. The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$). Average deviations of ±5 minutes per year can be easily achieved.

10.1.2 Method 2: OSCI trimmer

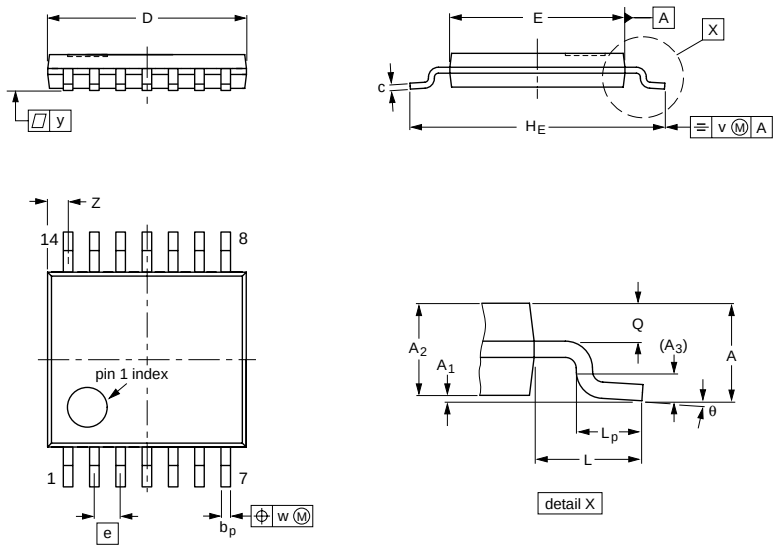
Using the 32.768 kHz signal available after power-on at pin CLKOUT, fast setting of a trimmer is possible.

10.1.3 Method 3: OSCO output

Direct measurement of OSCO out (accounting for test probe capacitance).

11. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 23. Package outline SOT402-1

12. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling MOS devices; see *JESD625-A and/or IEC61340-5*.

13. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 24) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 44 and 45

Table 44. SnPb eutectic process (from J-STD-020C)

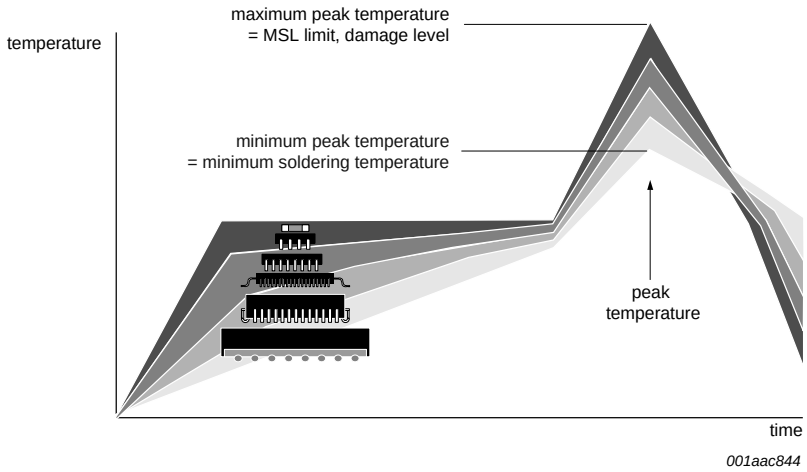
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 45. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 24.



MSL: Moisture Sensitivity Level

Fig 24. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Revision history

Table 46. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA2125_1	tbd	Product data sheet	-	PCA2125_00.11
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Figure 11 and Figure 13: update SPI diagrams for readout data, last bit during read. • Figure 4: POR ovrd diagram corrected. • Section 6.6: update SPI timing.			
PC212x_08	20061218	Objective data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

15.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For additional information, please visit: **http://www.nxp.com**

For sales office addresses, send an email to: **salesaddresses@nxp.com**

17. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 30 January 2007
Document identifier: PCA2125_00