NB6L295M

2.5V / 3.3V Dual Channel Programmable Clock/Data Delay with Differential CML Outputs

Multi−Level Inputs w/ Internal Termination

The NB6L295M is a Dual Channel Programmable Delay Chip designed primarily for Clock or Data de−skewing and timing adjustment. The NB6L295M is versatile in that two individual variable delay channels, PD0 and PD1, can be configured in one of two operating modes, a Dual Delay or an Extended Delay.

In the Dual Delay Mode, each channel has a programmable delay section which is designed using a matrix of gates and a chain of multiplexers. There is a fixed minimum delay of 3.2 ns per channel.

The Extended Delay Mode amounts to the additive delay of PD0 plus PD1 and is accomplished with the Serial Data Interface MSEL bit set High. This will internally cascade the output of PD0 into the input of PD1. Therefore, the Extended Delay path starts at the IN0/$\overline{IN0}$ inputs, flows through PD0, cascades to the PD1 and outputs through Q1/$\overline{Q1}$. There is a fixed minimum delay of 6.0 ns for the Extended Delay Mode.

The required delay is accomplished by programming each delay channel via a 3−pin Serial Data Interface, described in the application section. The digitally selectable delay has an increment resolution of typically 11 ps with a net programmable delay range of either 0 ns to 6 ns per channel in Dual Delay Mode; or from 0 ns to 11.2 ns for the Extended Delay Mode.

The Multi−Level Inputs can be driven directly by differential LVPECL, LVDS or CML logic levels; or by single ended LVPECL, LVCMOS or LVTTL. A single enable pin is available to control both inputs. The SDI input pins are controlled by LVCMOS or LVTTL level signals. The NB6L295M 16 mA CML output contains temperature compensation circuitry. This device is offered in a 4 mm x 4 mm 24−pin QFN Pb−free package. The NB6L295M is a member of the ECLinPS MAX™ family of high performance products.

- Input Clock Frequency > 1.5 GHz with 210 mV V_{OUTPP}
- Input Data Rate > 2.5 Gb/s
- Programmable Delay Range: 0 ns to 6 ns per Delay Channel
- Programmable Delay Range: 0 ns to 11.2 ns for Extended Delay Mode
- Total Delay Range: 3.2 ns to 9.0 ns per Delay Channel
- Total Delay Range: 6.2 ns to 17.8 ns in Extended Delay Mode
- Monotonic Delay: 11 ps Increments in 511 Steps
- Linearity ±20 ps, Maximum
- 100 ps Typical Rise and Fall Times
- 1 ps Typical Clock Jitter, RMS
- 20 ps Pk−Pk Typical Data Dependent Jitter
- LVPECL, CML or LVDS Differential Input Compatible
- LVPECL, LVCMOS, LVTTL Single Ended Input Compatible
- 3−Wire Serial Interface
- Operating Range: V_{CC} = 2.375 V to 3.6 V
- CML Output Level; 380 mV Peak−to−Peak, Typical
- Internal 50 Ω Input/Output Termination Provided
- −40°C to 85°C Ambient Operating Temperature
- 24−Pin QFN, 4 mm x 4 mm
- These are Pb−Free Devices

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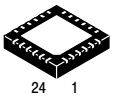
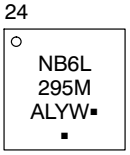


QFN−24
MN SUFFIX
CASE 485L

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

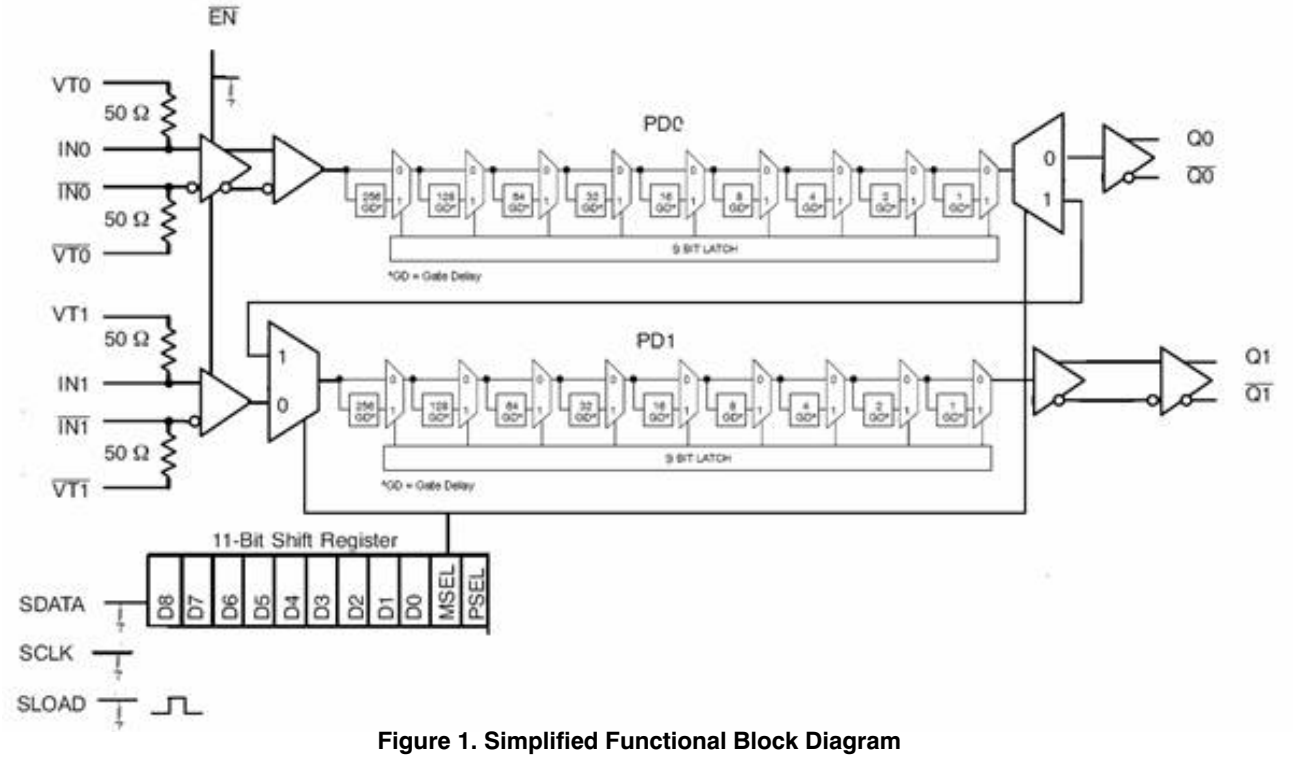


Figure 1. Simplified Functional Block Diagram

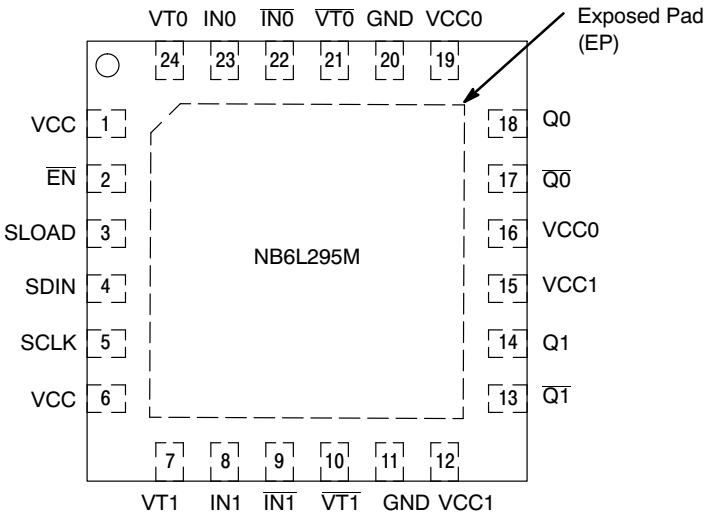


Figure 2. Pinout: QFN−24 (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	VCC	Power Supply	Positive Supply Voltage for the Inputs and Core Logic
2	$\overline{EN}$	LVCMOS/LVTTL Input	Input Enable/ Disable for both PD0 and PD1. LOW for enable, HIGH for disable, Open Pin Default state LOW (37 kΩ Pulldown Resistor).
3	SLOAD	LVCMOS/LVTTL Input	Serial Load; This pin loads the configuration latches with the contents of the shift register. The latches will be transparent when this signal is HIGH; thus, the data must be stable on the HIGH−to−LOW transition of S_LOAD for proper operation. Open Pin Default state LOW (37 kΩ Pulldown Resistor).
4	SDIN	LVCMOS/LVTTL Input	Serial Data In; This pin acts as the data input to the serial configuration shift register. Open Pin Default state LOW (37 kΩ Pulldown Resistor).
5	SCLK	LVCMOS/LVTTL Input	Serial Clock In; This pin serves to clock the serial configuration shift register. Data from SDIN is sampled on the rising edge. Open Pin Default state LOW (37 kΩ Pulldown Resistor).
6	VCC	Power Supply	Positive Supply Voltage for the Inputs and Core Logic
7	VT1		Internal 50 Ω Termination Pin for IN1.
8	IN1	LVPECL, CML, LVDS Input	Noninverted differential input. Note 1. Channel 1.
9	$\overline{IN1}$	LVPECL, CML, LVDS Input	Inverted differential input. Note 1. Channel 1.
10	$\overline{VT1}$		Internal 50 Ω Termination Pin for $\overline{IN1}$
11	GND	Power Supply	Negative Power Supply
12	VCC1	Power Supply	Positive Supply Voltage for the Q1/$\overline{Q1}$ outputs, channel PD1
13	$\overline{Q1}$	CML Output	Inverted Differential Output. Channel 1. Typically terminated with 50 Ω resistor to V_{CC1}
14	Q1	CML Output	Noninverted Differential Output. Channel 1. Typically terminated with 50 Ω resistor to V_{CC1}
15	VCC1	Power Supply	Positive Supply Voltage for the Q1/$\overline{Q1}$ outputs, channel PD1
16	VCC0	Power Supply	Positive Supply Voltage for the Q0/$\overline{Q0}$ outputs, channel PD0
17	$\overline{Q0}$	CML Output	Inverted Differential Output. Channel 0. Typically terminated with 50 Ω resistor to V_{CC0}
18	Q0	CML Output	Noninverted Differential Output. Channel 0. Typically terminated with 50 Ω resistor to V_{CC0}
19	VCC0	Power Supply	Positive Supply Voltage for the Q0/$\overline{Q0}$ outputs, channel PD0
20	GND	Power Supply	Negative Power Supply
21	$\overline{VT0}$		Internal 50 Ω Termination Pin for $\overline{IN0}$
22	$\overline{IN0}$	LVPECL, CML, LVDS Input	Noninverted differential input. Note 1. Channel 0.
23	IN0	LVPECL, CML, LVDS Input	Inverted differential input. Note 1. Channel 0.
24	VT0		Internal 50 Ω Termination Pin for IN0
−	EP	Ground	The Exposed Pad (EP) on the QFN−24 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is electrically connected to GND and must be connected to GND on the PC board.

1. In the differential configuration when the input termination pin (VTx/$\overline{VTx}$) are connected to a common termination voltage or left open, and if no signal is applied on INx/$\overline{INx}$ input then the device will be susceptible to self−oscillation.
2. All VCC, VCC0 and VCC1 Pins must be externally connected to the same power supply for proper operation. Both VCC0s are connected to each other and both VCC1s are connected to each other: VCC0 and VCC1 are separate.

Table 2. ATTRIBUTES

Characteristics		Value
Input Default State Resistors		37 kΩ
ESD Protection	Human Body Model Machine Model	> 2 kV > 100V
Moisture Sensitivity (Note 3)	QFN−24	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		3094
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}, V_{CC0}, V_{CC1}	Positive Power Supply	GND = 0 V		4.0	V
V_{IO}	Positive Input/Output Voltage	GND = 0 V	$-0.5 \le V_{IO} \le V_{CC}+0.5$	4.5	V
V_{INPP}	Differential Input Voltage $\lvert INx - \overline{INx}\rvert$			V_{CC} − GND	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)			±50	mA
I_{OUT}	Output Current Through R_T (50 Ω Resistor)			±50	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 4)	0 lfpm 500 lfpm	QFN−24 QFN−24	37 32	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 4)	QFN−24	11	°C/W
T_{sol}	Wave Solder Pb−Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 4. DC CHARACTERISTICS, MULTI−LEVEL INPUTS V_{CC} = V_{CC0} = V_{CC1} = 2.375 V to 3.6 V, GND = 0 V, T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
POWER SUPPLY CURRENT					
I_{CC}	Power Supply Current (Inputs, V_{TX} and Outputs Open) (Sum of I_{CC}, I_{CC0}, and I_{CC1})		170	215	mA
CML OUTPUTS (Notes 5 and 6, Figure 22)					
V_{OH}	Output HIGH Voltage V_{CC} = V_{CC0} = V_{CC1} = 3.3 V V_{CC} = V_{CC0} = V_{CC1} = 2.5 V	V_{CC} − 40 3260 2460	V_{CC} − 10 3290 2490	V_{CC} 3300 2500	mV
V_{OL}	Output LOW Voltage V_{CC} = V_{CC0} = V_{CC1} = 3.3 V V_{CC} = V_{CC0} = V_{CC1} = 2.5 V	V_{CC} − 500 2800 2000	V_{CC} − 400 2900 2100	V_{CC} − 300 3000 2200	mV
DIFFERENTIAL INPUT DRIVEN SINGLE−ENDED (see Figures 11 and 12) (Note 7)					
V_{th}	Input Threshold Reference Voltage Range	1050		V_{CC} − 150	mV
V_{IH}	Single−Ended Input HIGH Voltage	V_{th} +150		V_{CC}	mV
V_{IL}	Single−Ended Input LOW Voltage	GND		V_{th} − 150	mV
V_{ISE}	Single−Ended Input Voltage Amplitude (V_{IH} − V_{IL})	300		V_{CC} − GND	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (see Figures 13 and 14) (Note 8)					
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	GND		V_{CC} − 150	mV
V_{ID}	Differential Input Voltage Swing (INx, $\overline{INx}$) (V_{IHD} − V_{ILD})	150		V_{CC} − GND	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Note 9)	950		V_{CC} − 75	mV
I_{IH}	Input HIGH Current INx/$\overline{INX}$, (VTn/$\overline{VTn}$ Open)	−150		150	μA
I_{IL}	Input LOW Current IN/$\overline{INX}$, (VTn/$\overline{VTn}$ Open)	−150		150	μA
SINGLE−ENDED LVCMOS/LVTTL CONTROL INPUTS					
V_{IH}	Single−Ended Input HIGH Voltage	2000		V_{CC}	mV
V_{IL}	Single−Ended Input LOW Voltage	GND		800	mV
I_{IH}	Input HIGH Current	−150		150	μA
I_{IL}	Input LOW Current	−150		150	μA
TERMINATION RESISTORS					
R_{TIN}	Internal Input Termination Resistor	40	50	60	Ω
R_{TOUT}	Internal Output Termination Resistor	40	50	60	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. CML outputs loaded with 50 Ω to V_{CC} for proper operation.
6. Input and output parameters vary 1:1 with V_{CC}.
7. V_{th}, V_{IH}, V_{IL}, and V_{ISE} parameters must be complied with simultaneously. V_{th} is applied to the complementary input when operating in single−ended mode.
8. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.
9. V_{CMR}(min) varies 1:1 with voltage on GND pin, V_{CMR}(max) varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.

Table 5. AC CHARACTERISTICS $V_{CC} = V_{CC0} = V_{CC1}$ = 2.375 V to 3.6 V, GND = 0 V, T_A = −40°C to +85°C (Note 10)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{SCLK}	Serial Clock Input Frequency, 50% Duty Cycle			20	MHz
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) $f_{in} \leq 1.5$ GHz (Note 15) (See Figure 23)	210	380		mV
f_{DATA}	Maximum Data Rate (Note 14)	2.5			Gb/s
t_{Range}	Programmable Delay Range (@ 50 MHz) Dual Mode IN0/IN0 to Q0/Q0 or IN1/IN1 to Q1/Q1 Extended Mode IN0/IN0 to Q1/Q1	 0 0	 5.7 11.2	 6.9 13.7	ns
t_{SKEW}	Duty Cycle Skew (Note 11) Within Device Skew − Dual Mode D[8:0] = 0 D[8:0] = 1		4 55 67	 96 170	ps
L_{in}	Linearity (Note 12)		±15	±20	ps
t_s	Setup Time (@ 20 MHz) SDIN to SCLK SLOAD to SCLK $\overline{EN}$ to SDIN	0.5 1.5 0.5	0.3 1.0		ns
t_h	Hold Time SDIN to SCLK SLOAD to SCLK $\overline{EN}$ to SLOAD	1.0 1.0 0.5	0.6		ns
t_{pwmin}	Minimum Pulse Width SLOAD	1			ns
t_{JITTER}	Clock TIE Jitter RMS (Note 13) $f_{in} \leq 1.5$ GHz Data Dependent Jitter P−P (Note 14) $f_{DATA} \leq 2.5$ Gb/s		2.4 2.0	9.0 15	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 15)	150		V_{CC} − GND	mV
t_r, t_f	Output Rise/Fall Times (@ 50 MHz), (20% − 80%) Qx, $\overline{Qx}$	85	100	150	ps

10. Measured by forcing $V_{INPPmin}$ and $V_{INPPmax}$ from a 50% duty cycle clock source, V_{CMR} (min+max). All loading with an external R_L = 50 Ω to V_{CC}. See Figure 20. Input edge rates 40 ps (20% − 80%).
11. Duty cycle skew is measured between differential outputs using the deviations of the sum of Tpw− and Tpw+ @ 0.5 GHz.
12. Deviation from a linear delay (actual Min to Max) in the Dual Mode 511 programmable steps; 3.3 V @ 25°C, 400 mV V_{INPP}.
13. Additive CLOCK jitter with 50% duty cycle input clock signal. 1000 WFMS, JIT3 Software.
14. NRZ data at PRBS23 and K28.5. 10,000 WFMS, TDS8000.
15. 1Input and output voltage swing is a single−ended measurement operating in differential mode.

Table 6. AC CHARACTERISTICS $V_{CC} = V_{CC0} = V_{CC1}$ = 2.375 V to 3.6 V, GND = 0 V, T_A = −40°C to +85°C (Note 10)

Symbol	Characteristic	−40°C			+25°C			+85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delay (@ 50 MHz) Dual Mode INx to Qx / $\overline{INx}$ to $\overline{Qx}$ D[8:0] = 0 D[8:0] = 1 Extended Mode INx to Qx/$\overline{INx}$ to $\overline{Qx}$ D[8:0] = 0 D[8:0] = 1	 2.9 8.1 5.5 16	 3.1 8.7 5.9 17.2	 3.3 9.3 6.7 18.1	 3.0 8.3 5.7 16.5	 3.2 9.0 6.2 17.8	 3.5 9.8 6.7 19.1	 3.1 8.6 5.9 17	 3.4 9.3 6.6 19	 3.8 10.7 7.3 21	ns
Δt	Step Delay (Selected D Bit HIGH All Others LOW) D0 HIGH D1 HIGH D2 HIGH D3 HIGH D4 HIGH D5 HIGH D6 HIGH D7 HIGH D8 HIGH					 8.4 16.4 41.2 85 178 360 722 1448 2903			 12.4 25.1 58.3 108 210 405 796 1579 3143		ns

Serial Data Interface Programming

The NB6L295M is programmed by loading the 11−Bit SHIFT REGISTER using the SCLK, SDATA and SLOAD inputs. The 11 SDATA bits are 1 PSEL bit, 1 MSEL bit and 9 delay value data bitsD[8:0]. A separate 11−bit load cycle is required to program the delay data value of each channel, PD0 and PD1. For example, at powerup two load cycles will be needed to initially set PD0 and PD1; Dual Mode Operation as shown in Figures 3 and 4 and Extended Mode Operation as shown in Figures 5 and 6.

DUAL MODE OPERATIONS

PD0 Programmable Delay									Control Bits		
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	Value
D8	D7	D6	D5	D4	D3	D2	D1	D0	MSEL	PSEL	Bit Name
(MSB)										(LSB)	

Figure 3. PDO Shift Register

PD1 Programmable Delay									Control Bits		
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	1	Value
D8	D7	D6	D5	D4	D3	D2	D1	D0	MSEL	PSEL	Bit Name
(MSB)										(LSB)	

Figure 4. PD1 Shift Register

EXTENDED MODE OPERATIONS

PD0 Programmable Delay									Control Bits		
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	1	0	Value
D8	D7	D6	D5	D4	D3	D2	D1	D0	MSEL	PSEL	Bit Name
(MSB)										(LSB)	

Figure 5. PDO Shift Register

PD1 Programmable Delay									Control Bits		
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	1	1	Value
D8	D7	D6	D5	D4	D3	D2	D1	D0	MSEL	PSEL	Bit Name
(MSB)										(LSB)	

Figure 6. PD1 Shift Register

Refer to Table 7, Channel and Mode Select BIT Functions. In a load cycle, the 11−Bit Shift Register least significant bit (clocked in first) is **PSEL** and will determine which channel delay buffer, either PDO (LOW) or PD1 (HIGH), will latch the delay data value D[8:0]. The **MSEL BIT** determines the Delay Mode. When set LOW, the Dual Delay Mode is selected and the device uses both channels independently. A pulse edge entering IN0/$\overline{\text{IN0}}$ is delayed according to the values in PD0 and exits from Q0/$\overline{\text{Q0}}$. An input signal pulse edge entering IN1/$\overline{\text{IN1}}$ is delayed according to the values in PD1 and exits from Q1/$\overline{\text{Q1}}$. When MSEL is set HIGH, the Extended Delay Mode is selected and an input signal pulse edge enters IN0 and $\overline{\text{IN0}}$ and flows through PD0 and is extended through PD1 to exit at Q1 and $\overline{\text{Q1}}$. The most significant 9−bits, D[8:0] are delay value data for both channels. See Figure 7.

Table 7. CHANNEL AND MODE SELECT BIT FUNCTIONS

BIT Name	Function
PSEL	0 Loads Data to PD0
	1 Loads Data to PD1
MSEL	0 Selects Dual Programmable Delay Paths, 3.1 ns to 8.8 ns Delay Range for Each Path
	1 Selects Extended Delay Path from IN0/$\overline{\text{IN0}}$ to Q1/$\overline{\text{Q1}}$, 6.0 ns to 17.2 ns Delay Range; Disables Q0/$\overline{\text{Q0}}$ Outputs, Q0−LOW, $\overline{\text{Q0}}$−HIGH.
D[8:0]	Select one of 512 Delay Values

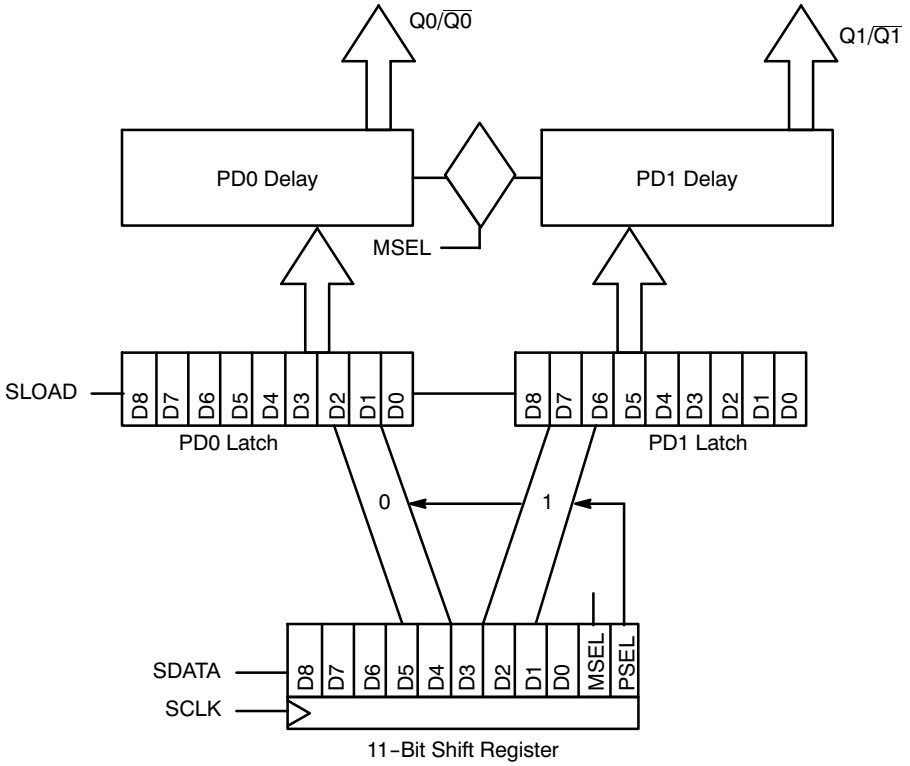


Figure 7. Serial Data Interface, Shift Register, Data Latch, Programmable Delay Channels Load Cycle Required for Each Channel

Serial Data Interface Loading

Loading the device through the 3 input Serial Data Interface (SDI) is accomplished by sending data into the SDIN pin by using the SCLK input pin and latching the data with the SLOAD input pin. The 11−bit SHIFT REGISTER shifts once per rising edge of the **SCLK** input. The serial input **SDIN** must meet setup and hold timing as specified in the AC Characteristics section of this document for each bit and clock pulse. The **SLOAD** line loads the value of the shift register on a LOW−to−HIGH edge transition (transparent state) into a data Latch register and latches the data with a subsequent HIGH−to−LOW edge transition. Further changes in SDIN or SCLK are not recognized by the latched register. The internal multiplexer states are set by the PSEL and MSEL bits in the SHIFT register. Figure 6 shows the timing diagram of a typical load sequence. Input $\overline{EN}$ should be LOW (enabled) prior to SDI programming, then pulled HIGH (disabled) during programming. After programming, the $\overline{EN}$ should be returned LOW (enabled) for functional delay operation.

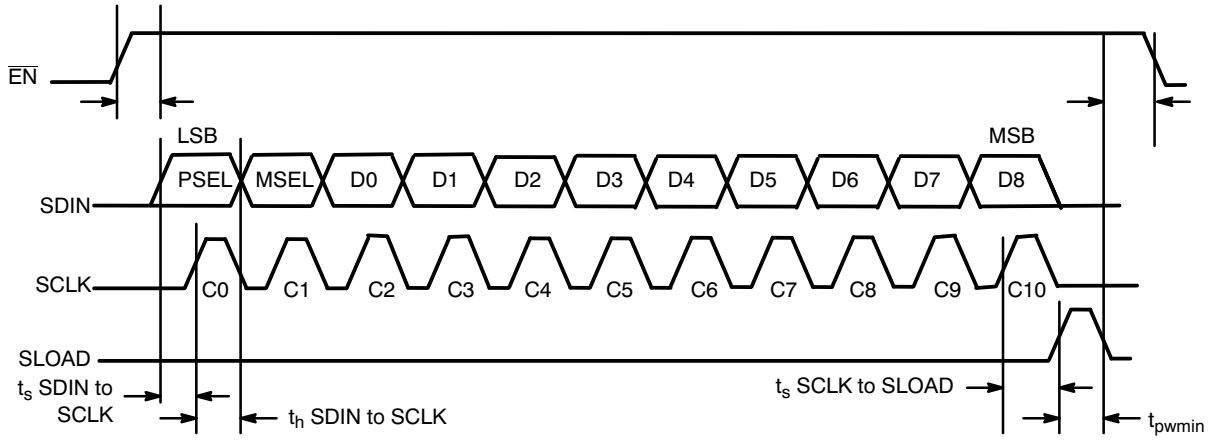


Figure 8. SDI Programming Cycle Timing Diagram (Load Cycle 1 of 2)

Table 8 shows theoretical values of delay capabilities in both the Dual Delay Mode and in the Extended Delay Modes of operation.

Table 8. EXAMPLES OF THEORETICAL DELAY VALUES FOR PD0 AND PD1 IN DUAL MODE
INPUTS: IN0/$\overline{IN0}$, IN1/$\overline{IN1}$, OUTPUTS: Q0/$\overline{Q0}$, Q1, $\overline{Q1}$

Dual Mode						
PD1 D[8:0]	(Decimal)	PD0 D[8:0]	(Decimal)	MSEL	PD0 Delay* (ps)	PD1 Delay* (ps)
000000000	(0)	000000000	(0)	0	0	0
000000000	(0)	000000001	(1)	0	11	0
000000000	(0)	000000010	(2)	0	22	0
000000000	(0)	000000011	(3)	0	33	0
000000000	(0)	000000100	(4)	0	44	0
000000000	(0)	000000101	(5)	0	55	0
000000000	(0)	000000110	(6)	0	66	0
000000000	(0)	000000111	(7)	0	77	0
000000000	(0)	000001000	(8)	0	88	0
		• • •			• • •	• • •
000000000	(0)	000010000	(16)	0	176	0
000000000	(0)	000100000	(32)	0	352	0
000000000	(0)	001000000	(64)	0	704	0
000000000	(0)	111111101	(509)	0	5599	0
000000000	(0)	111111110	(510)	0	5610	0
000000000	(0)	111111111	(511)	0	5621	0

*Fixed minimum delay not included

Table 9. EXAMPLES OF THEORETICAL DELAY VALUES FOR PD0 AND PD1 IN EXTENDED MODE
INPUTS: IN0/$\overline{IN0}$, IN1/$\overline{IN1}$, OUTPUTS: Q0/$\overline{Q0}$, Q1, $\overline{Q1}$

Extended Delay Mode							
PD1 D[8:0]	(Decimal)	PD0 D[8:0]	(Decimal)	MSEL	PD0* (ps)	PD1* (ps)	Total Delay* (ps)
000000000	(0)	000000000	(0)	1	0	0	0
000000000	(0)	000000001	(1)	1	0	11	11
000000000	(0)	000000010	(2)	1	0	22	22
000000000	(0)	000000011	(3)	1	0	33	33
		• • •			• • •	• • •	• • •
000000000	(0)	111111101	(509)	1	0	5599	5599
000000000	(0)	111111110	(510)	1	0	5610	5610
000000000	(0)	111111111	(511)	1	0	5621	5621
000000001	(1)	111111111	(511)	1	11	5621	5632
000000010	(2)	111111111	(511)	1	22	5621	5643
		• • •			• • •	• • •	• • •
111111100	(508)	111111111	(511)	1	5588	5621	11209
111111101	(509)	111111111	(511)	1	5599	5621	11220
111111110	(510)	111111111	(511)	1	5610	5621	11231
111111111	(511)	111111111	(511)	1	5621	5621	11242

*Fixed minimum delay not included

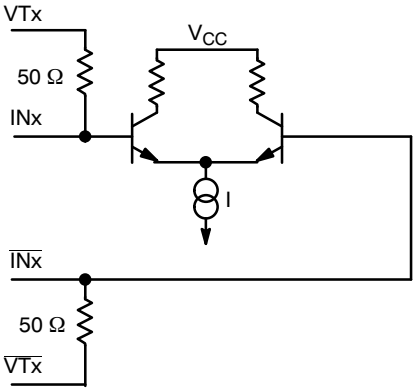


Figure 9. Input Structure

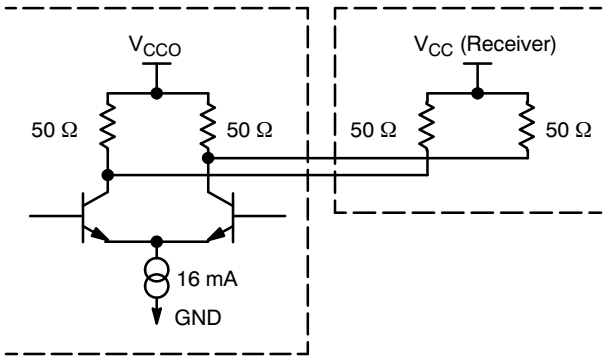


Figure 10. Typical CML Output Structure and Termination

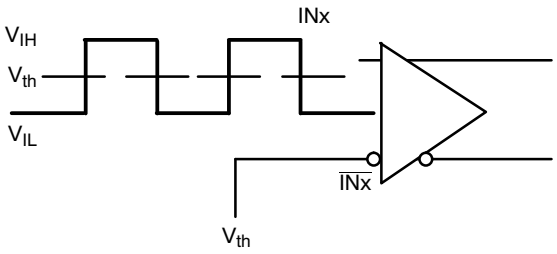


Figure 11. Differential Input Driven Single−Ended

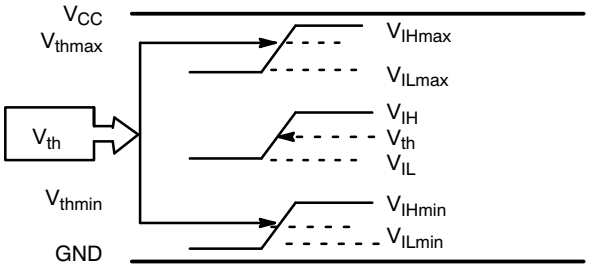


Figure 12. V_{th} Diagram

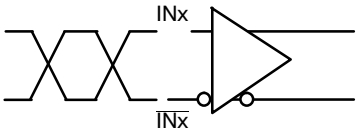


Figure 13. Differential Inputs Driven Differentially

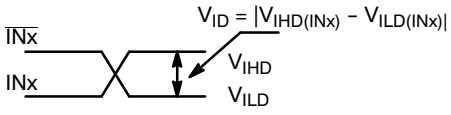


Figure 14. Differential Inputs Driven Differentially

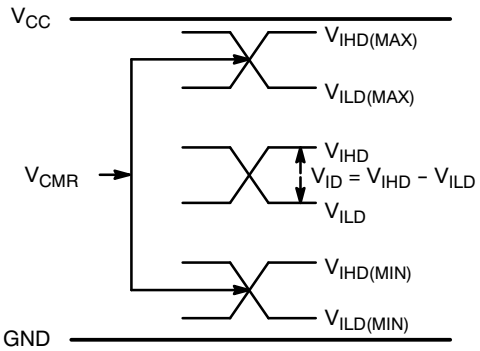


Figure 15. V_{CMR} Diagram

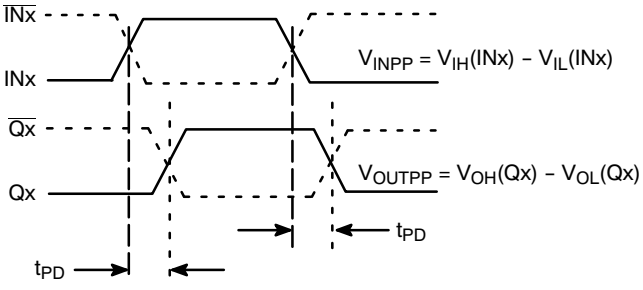


Figure 16. AC Reference Measurement

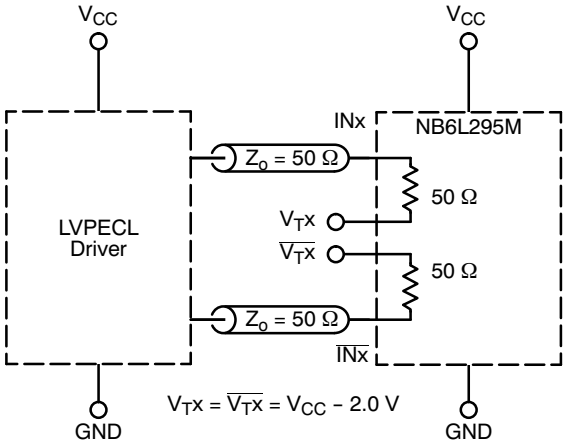


Figure 17. LVPECL Interface

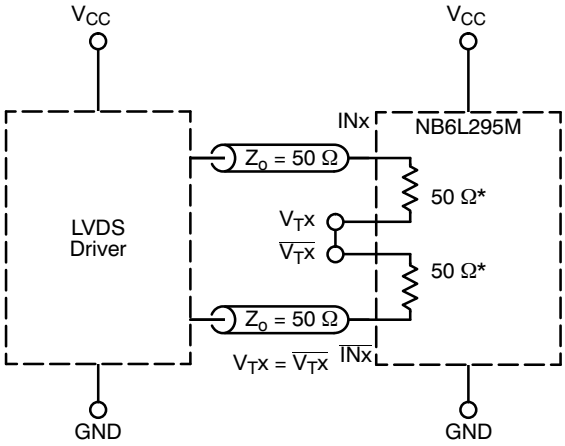


Figure 18. LVDS Interface

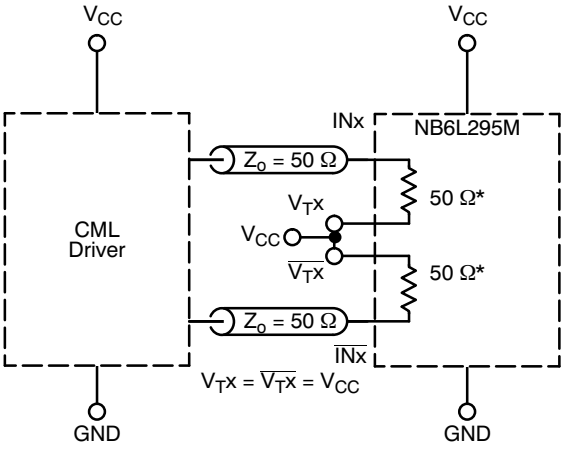


Figure 19. CML Interface, Standard 50 Ω Load

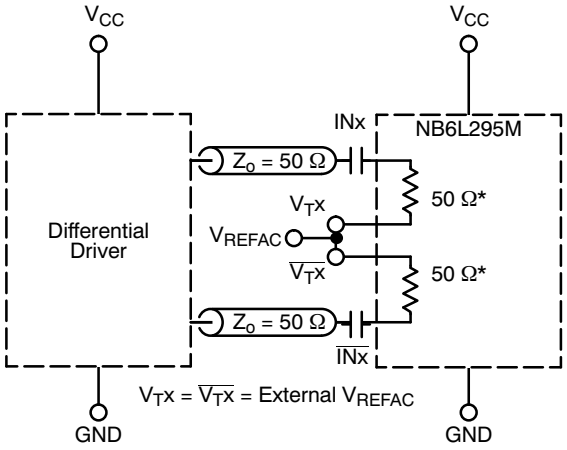


Figure 20. Capacitor−Coupled Differential Interface (V_{Tx}/$\overline{V_{Tx}}$ Connected to V_{REFAC}; V_{REFAC} Bypassed to Ground with 0.1 μF Capacitor)

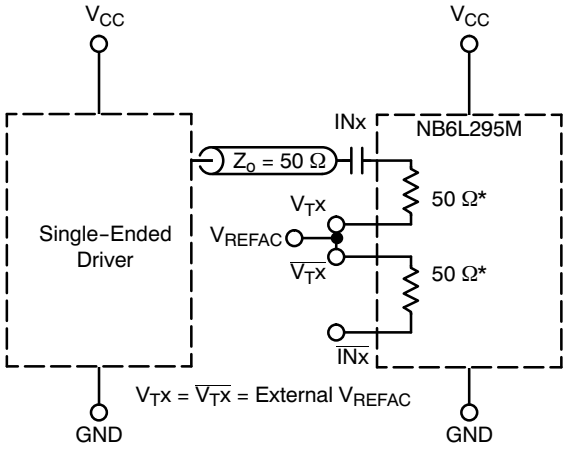


Figure 21. Capacitor−Coupled Single−Ended Interface (V_{Tx}/$\overline{V_{Tx}}$ Connected to External V_{REFAC}; V_{REFAC} Bypassed to Ground with 0.1 μF Capacitor)

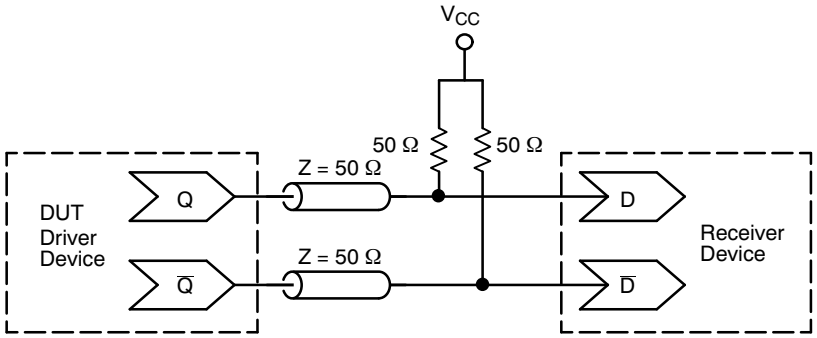


Figure 22. Typical Termination for Output Driver and Device Evaluation

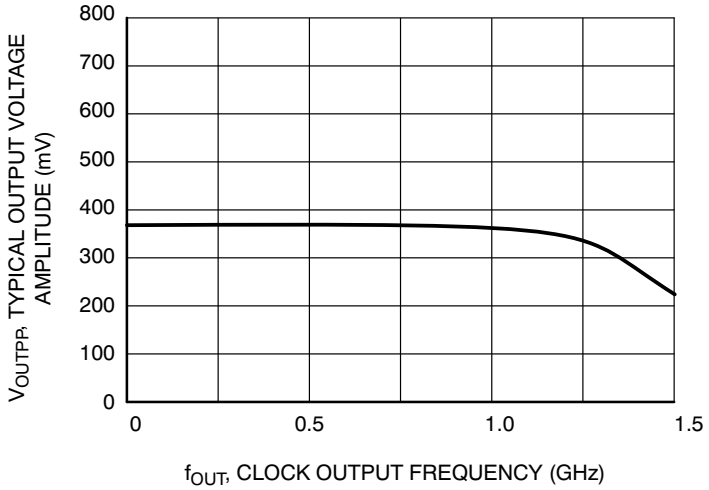


Figure 23. Output Voltage Amplitude (V_{OUTPP}) vs. Output Frequency at Ambient Temperature (Typical)

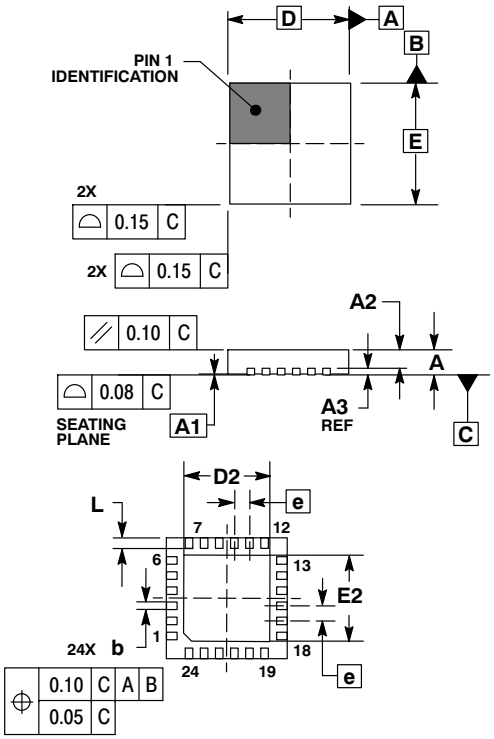
ORDERING INFORMATION

Device	Package	Shipping†
NB6L295MMNG	QFN−24 (Pb−free)	92 Units / Rail
NB6L295MMNTXG	QFN−24 (Pb−free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

QFN 24
MN SUFFIX
24 PIN QFN, 4x4
CASE 485L−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.23	0.28
D	4.00 BSC	
D2	2.70	2.90
E	4.00 BSC	
E2	2.70	2.90
e	0.50 BSC	
L	0.35	0.45

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