MK2722
Sigma Designs Clock Source

Description

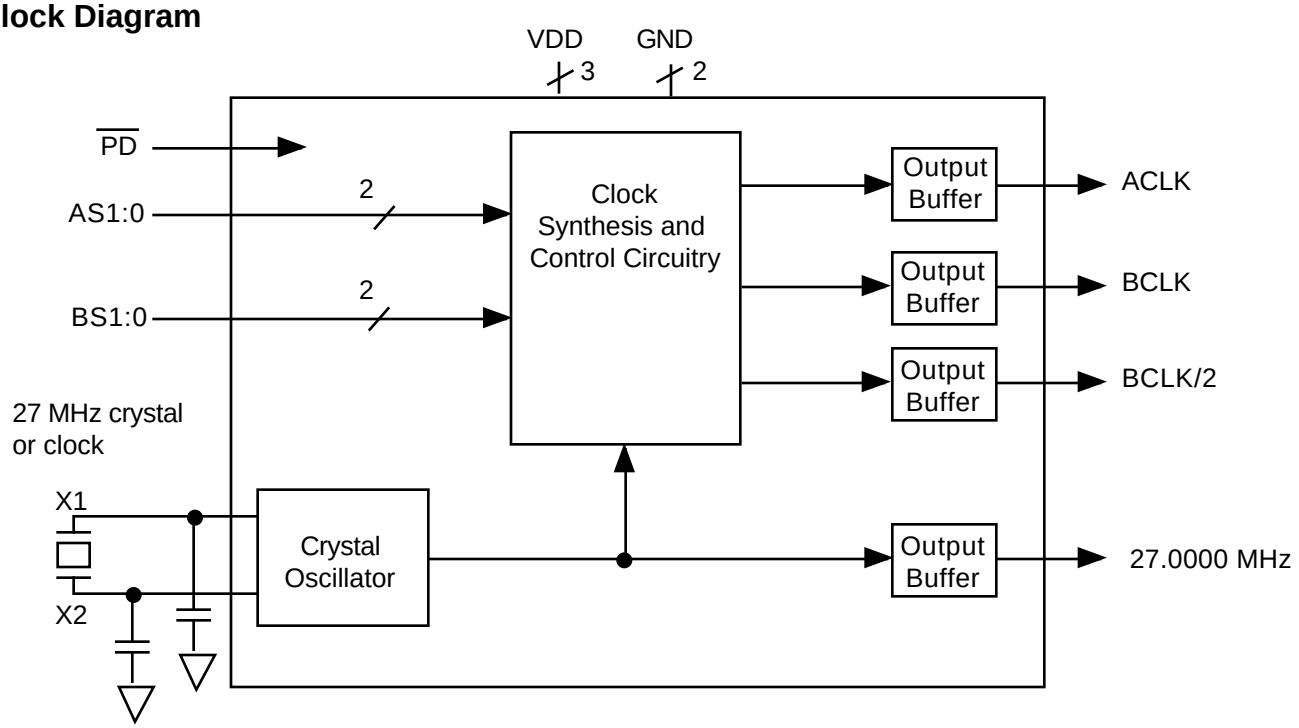
The MK2722 is a low cost, low jitter, high performance clock synthesizer designed for Sigma Designs' MPEG decoder systems. Using analog Phase-Locked Loop (PLL) techniques, the device accepts a 27 MHz crystal or clock input to produce multiple output clocks. The power down pin turns off the device, drawing less than 100 µA.

ICS offers a wide variety of clock synthesizers for desktop and portable computers, and multimedia systems. Consult ICS to eliminate crystals and oscillators from your board.

Features

- Packaged in 16 pin narrow (150 mil) SOIC
- Uses 27 MHz crystal or clock input
- Zero ppm synthesis error in all clocks (audio clocks exactly track 27 MHz video clock)
- Audio clock supports 32, 44.1, and 48kHz sampling rates at 256X and 384X
- Power down turns off chip
- Low jitter
- Total of four output clocks
- 25 mA output drive capability at TTL levels
- 5V±10% supply voltage (contact ICS for 3.3V operation)
- Advanced, low power, sub-micron CMOS process

Block Diagram



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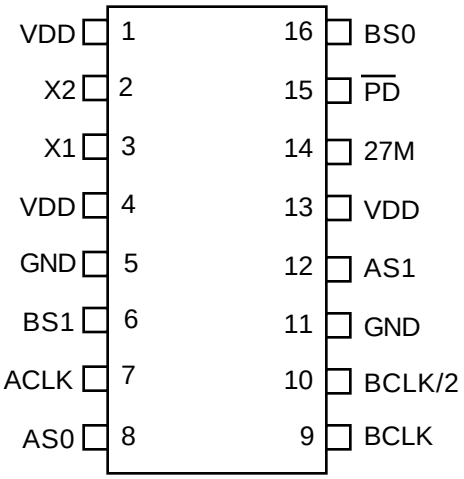
Pin Assignment



16 pin narrow (150 mil) SOIC

ACLK Decoding Table (MHz)

AS1	AS0	ACLK
pin 12	pin 8	pin 7
0	0	12.288
0	M	18.432
0	1	16.9344
1	0	11.2896
1	M	12.288
1	1	8.192

BCLK Decoding Table (MHz)

BS1	BS0	BCLK	BCLK/2
pin 6	pin 16	pin 9	pin 10
0	0	40.5	20.25
0	1	50	25
1	0	28.6364	14.3182
1	1	40	20

Pin Descriptions

Number	Name	Type	Description
1	VDD	I	Connect to +5V.
2	X2	XO	Crystal connection. Connect to 27 MHz crystal. Leave unconnected for clock input.
3	X1	XI	Crystal connection. Connect to 27 MHz crystal or clock.
4	VDD	P	Connect to +5V.
5	GND	P	Connect to ground.
6	BS1	I	Select 1 for BCLK. Determines BCLK outputs per table above. Internal pull-up.
7	ACLK	O	Audio Clock output. Determined by status of AS1, AS0 per table above.
8	AS0	TI	Select 0 for ACLK. Determines ACLK output per table above.
9	BCLK	O	BCLK output. Determined by status of BS1, BS0 per table above.
10	BCLK/2	O	BCLK divided by two output. Determined by status of BS1, BS0 per table above.
11	GND	P	Connect to ground.
12	AS1	I	Select 1 for ACLK. Determines ACLK output per table above. Internal pull-up.
13	VDD	P	Connect to +5V.
14	27M	O	27.0000 MHz buffered crystal clock output.
15	$\overline{PD}$	I	Power Down. Active low. Clocks stop low. Internal pull-up.
16	BS0	I	Select 0 for BCLK. Determines BCLK outputs per table above. Internal pull-up.

Key: I = Input, TI = Tri-level input, O = output, P = power supply connection

Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (Note 1)					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
DC CHARACTERISTICS (VDD = 5V unless noted)					
Operating Voltage, VDD		4.5	5	5.5	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Output High Voltage, VOH	IOH=-4mA	VDD-0.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
Operating Supply Current, IDD, 5.0V	No Load		30		mA
Power Down Supply Current, IDDPD, 5V	No Load, note 2		25		µA
Short Circuit Current	Each output		±50		mA
Input Capacitance			7		pF
On chip pull-up resistor	Pins 6, 8, 12, 15, and 16		250		kΩ
AC CHARACTERISTICS (VDD = 5V unless noted)					
Input Frequency			27.000		MHz
Input Crystal Accuracy				±30	ppm
Frequency Error, all clocks				0	ppm
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	At 1.4V	40	50	60	%
Maximum Absolute Jitter, short term			200		ps

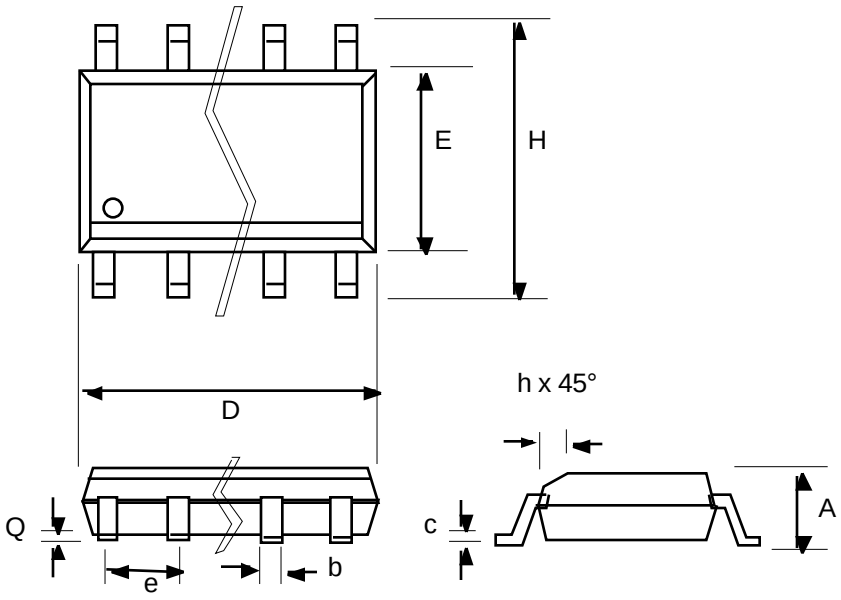
Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. With AS1=AS0=BS1=BS0=VDD

External Components

The MK2722 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.1µF should be connected between VDD and GND (pins 4 and 5, 13 and 11), as close to the MK2722 as possible. A series termination resistor of 33Ω may be used for each clock output. If a clock input is not used, a 27 MHz fundamental mode crystal must be connected as close to the chip as possible. Crystal capacitors should be connected from pins X1 to ground and X2 to ground. The value (in pF) of these crystal capacitors should be = (C_L-12)*2, where C_L is the crystal load capacitance in pF. So for a crystal with 16pF load capacitance, the crystal capacitors should be 8pF each.

Package Outline and Package Dimensions

16 pin SOIC narrow



	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.055	0.070	1.397	1.778
b	0.013	0.019	0.330	0.483
c	0.007	0.010	0.191	0.254
D	0.385	0.400	9.779	10.160
E	0.150	0.160	3.810	4.064
H	0.225	0.245	5.715	6.223
e	.050 BSC		1.27 BSC	
h		0.016		0.406
Q	0.004	0.01	0.102	0.254

Ordering Information

Part/Order Number	Marking	Shipping packaging	Package	Temperature
MK2722-01S	MK2722-01S	tubes	16 pin SOIC	0-70°C
MK2722-01STR	MK2722-01S	tape and reel	16 pin SOIC	0-70°C