## Description

The MK2771-03 is a low cost, low jitter, high performance VCXO and clock synthesizer designed for set-top boxes. The on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3V input voltage to cause the output clocks to vary by ±100 ppm. Using ICS/MicroClock's patented VCXO and analog Phase-Locked Loop (PLL) techniques, the device uses an inexpensive 13.5 MHz crystal input to produce multiple output clocks including a selectable processor clock, a selectable audio clock, a fixed 33.33 MHz or 24.576 MHz, two low skew copies of the 27MHz, and a fixed 13.5 MHz. All clocks are frequency locked to the 27.00MHz output (and to each other) with zero ppm error, so any output can be used as the VCXO output.

This chip directly replaces the MK2771-03 when a 13.5 MHz input crystal is substituted for the 14.31818 MHz used on the -03. Additionally, the -13 adds 25 MHz to the processor clock selection, and 24.576 MHz on the BCLK.

## Features

- Packaged in 20 pin SOIC
- Pin for pin and functional upgrade to MK2771-03
- Ideal for systems using Oak's MPEG decoders
- On-chip patented VCXO with pull range of 200ppm
- VCXO tuning voltage of 0 to 3V
- Processor frequency of 16.67 MHz, 20 MHz, 25 MHz, 32 MHz, 40 MHz, or 50 MHz
- Audio clocks of 8.192, 11.2896, and 12.288 MHz
- Zero ppm synthesis error in all clocks (all exactly track 27MHz VCXO) - patented
- Uses an inexpensive 13.5 MHz crystal
- 25mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- 5V operating voltage

## Block Diagram
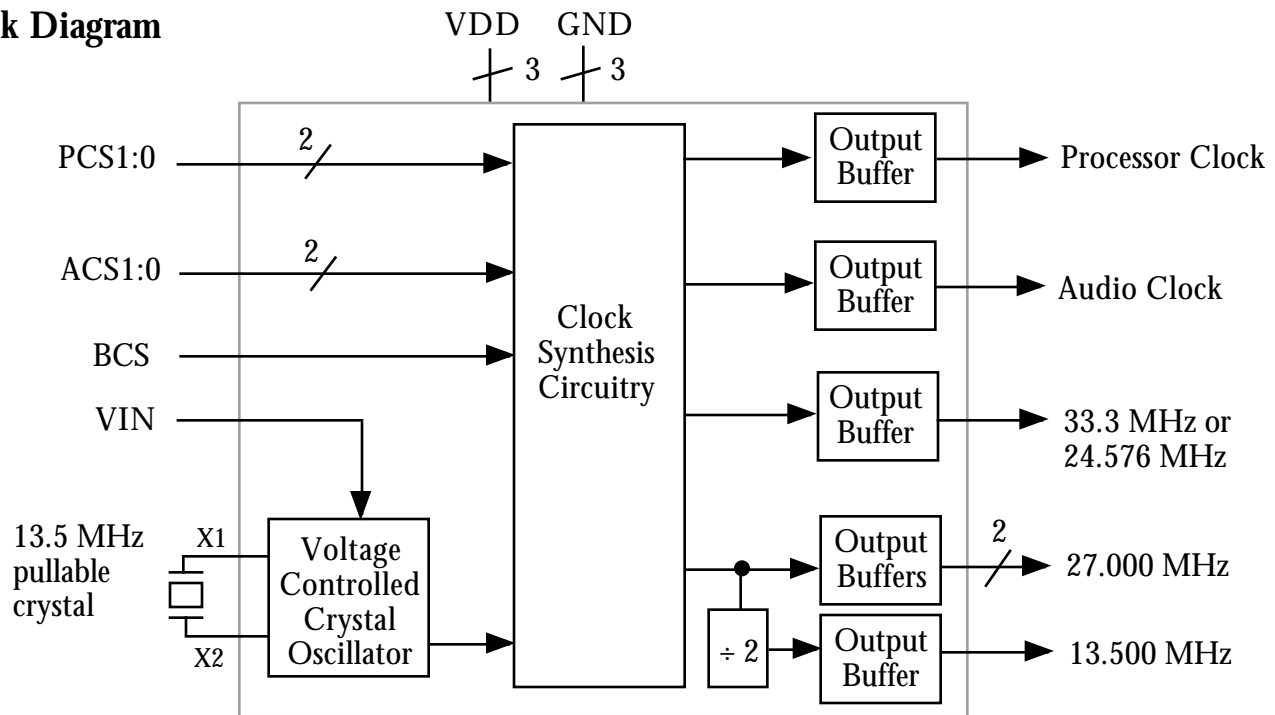
## Pin Assignment

```
PCS0 ☐  1        20 ☐ ACS1
 X2  ☐  2        19 ☐ ACS0
 X1  ☐  3        18 ☐ BCS
VDD  ☐  4        17 ☐ GND
VIN  ☐  5        16 ☐ 27M
VDD  ☐  6        15 ☐ VDD
GND  ☐  7        14 ☐ GND
PCLK ☐  8        13 ☐ 27M
BCLK ☐  9        12 ☐ PCS1
ACLK ☐ 10        11 ☐ 13.5M
```

## Processor Clock Select Table

| PCS1 | PCS0 | PCLK (MHz) |
|------|------|------------|
| 0 | 0 | 50.000 |
| 0 | 1 | 16.667 |
| M | 0 | 25.000 |
| M | 1 | 32.000 |
| 1 | 0 | 40.000 |
| 1 | 1 | 20.000 |

0 = connect directly to ground, 1 = connect directly
to VDD, M = leave floating or unconnected

## Audio Clock Table

| ACS1 | ACS0 | ACLK (MHz) |
|------|------|------------|
| 0 | 0 | 8.192 |
| 0 | 1 | 11.2896 |
| 1 | 0 | 12.288 |
| 1 | 1 | 5.6448 |

## Bus Clock Table

| BCS | BCLK (MHz) |
|-----|------------|
| 0 | 33.333 |
| 1 | 24.576 |

## Pin Descriptions

| Number | Name | Type | Description |
|--------|------|------|-------------|
| 1 | PCS0 | I | Processor Clock Select 0.  Selects PCLK on pin 8. See table above. |
| 2 | X2 | XO | Crystal connection. Connect to a pullable 13.5 MHz crystal. |
| 3 | X1 | XI | Crystal connection. Connect to a pullable 13.5 MHz crystal. |
| 4, 6, 15 | VDD | P | Connect to +5V. |
| 5 | VIN | I | Voltage Input to VCXO. Zero to 3V signal which controls the frequency of the VCXO. |
| 7, 14, 17 | GND | P | Connect to ground. |
| 8 | PCLK | O | Processor clock output determined by status of PCS1,0. See table above. |
| 9 | BCLK | O | 33.33MHz or 24.576 MHz Bus Clock output. See table above. |
| 10 | ACLK | O | Audio clock output determined by status of ACS1,0. See table above. |
| 11 | 13.5M | O | 13.5 MHz clock output. Divide by two of the 27MHz VCXO output. |
| 12 | PCS1 | TI | Processor Clock Select 1.  Selects PCLK on pin 8. See table above. |
| 13 | 27M | O | 27.00 MHz VCXO clock output. |
| 16 | 27M | O | 27.00 MHz VCXO clock output. |
| 18 | BCS | P | Bus Clock Select . Selects BCLK on pin 9. See table above. |
| 19 | ACS0 | I | Audio Clock Select 0.  Selects ACLK on pin 10. See table above. |
| 20 | ACS1 | I | Audio Clock Select 1.  Selects ACLK on pin 10. See table above. |

Key: I = Input, TI = Tri-level input, O = output, P = power supply connection

## Electrical Specifications

| Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| **ABSOLUTE MAXIMUM RATINGS (note 1)** | | | | | |
| Supply voltage, VDD | Referenced to GND | | | 7 | V |
| Inputs and Clock Outputs | Referenced to GND | -0.5 | | VDD+0.5 | V |
| Ambient Operating Temperature | | 0 | | 70 | °C |
| Soldering Temperature | Max of 10 seconds | | | 260 | °C |
| Storage temperature | | -65 | | 150 | °C |
| **DC CHARACTERISTICS (VDD = 5.0V unless noted)** | | | | | |
| Operating Voltage, VDD | | 4.75 | | 5.25 | V |
| Input High Voltage, VIH, X1 pin only | | 3.5 | 2.5 | | V |
| Input Low Voltage, VIL, X1 pin only | | | 2.5 | 1.5 | V |
| Input High Voltage, VIH (except PCS1) | | 2 | | | V |
| Input Low Voltage, VIL (except PCS1) | | | | 0.8 | V |
| Input High Voltage, VIH, PCS1 only | | VDD-0.5 | | | V |
| Input Low Voltage, VIL, PCS1 only | | | | 0.5 | V |
| Output High Voltage, VOH | IOH=-25mA | 2.4 | | | V |
| Output Low Voltage, VOL | IOL=25mA | | | 0.4 | V |
| Output High Voltage, VOH, CMOS level | IOH=-8mA | VDD-0.4 | | | V |
| Operating Supply Current, IDD | No Load, note 2 | | 60 | | mA |
| Short Circuit Current | Each output | | ±100 | | mA |
| Input Capacitance | | | 7 | | pF |
| Frequency synthesis error | All clocks | | | 0 | ppm |
| VIN, VCXO control voltage | | 0 | | 3 | V |
| **AC CHARACTERISTICS (VDD = 5.0V unless noted)** | | | | | |
| Input Frequency | | | 13.500000 | | MHz |
| Output Clock Rise Time | 0.8 to 2.0V | | | 1.5 | ns |
| Output Clock Fall Time | 2.0 to 0.8V | | | 1.5 | ns |
| Output Clock Duty Cycle | At 1.4V | 40 | | 60 | % |
| Maximum Absolute Jitter, short term | | | 200 | | ps |
| Skew of 27 MHz outputs | Rising edges at 1.4V | -500 | 0 | 500 | ps |
| 27 MHz output pullability, note 3 | 0V  VIN  3V | | ±100 | | ppm |

Notes:   1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. With PCLK at 50 MHz.
3. With a pullable crystal that conforms to ICS' specifications

## External Components

The MK2771-13 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.1μF should be connected between VDD and GND on pins 4 and 7, 6 and 7, and 15 and 14, as close to the MK2771-13 as possible. A series termination resistor of 33   may be used for each clock output.The 13.500 MHz crystal must be connected as close to the chip as possible. The crystal should be a parallel mode, pullable, with load capacitance of 14pF. Consult MicroClock for recommended suppliers. See MAN05 for recommended layout of the chip and external components.

## Package Outline and Package Dimensions

**20 pin SOIC**
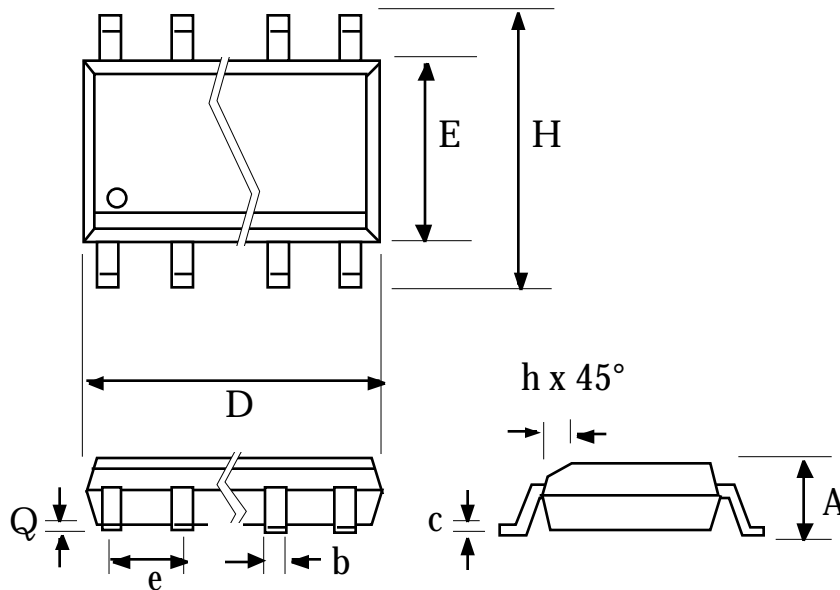
| Symbol | Inches Min | Inches Max | Millimeters Min | Millimeters Max |
|--------|------|------|--------|--------|
| A | 0.092 | 0.104 | 2.3368 | 2.6416 |
| b | 0.014 | 0.019 | 0.356 | 0.483 |
| c | 0.009 | 0.012 | 0.229 | 0.305 |
| D | 0.490 | 0.512 | 12.446 | 13.005 |
| E | 0.290 | 0.300 | 7.366 | 7.620 |
| H | 0.394 | 0.419 | 10.008 | 10.643 |
| e | .050 BSC | | 1.27 BSC | |
| h | | 0.016 | | 0.406 |
| Q | 0.003 | 0.011 | 0.076 | 0.279 |

## Ordering Information

| Part/Order Number | Marking | Shipping packaging | Package | Temperature |
|-------------------|---------|--------------------|---------|-------------|
| MK2771-13S | MK2771-13S | tubes | 20 pin SOIC | 0-70°C |
| MK2771-13STR | MK2771-13S | tape and reel | 20 pin SOIC | 0-70°C |