DATA SHEET

Low Voltage Low Skew CMOS PLL Clock Driver, 3-State

MC88LV915T

The MC88LV915T Clock Driver utilizes phase–locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for high performance PC's and workstations.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple components on a board. The PLL also allows the MC88LV915T to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency. Multiple 88LV915's can lock onto a single reference clock, which is ideal for applications when a central system clock must be distributed synchronously to multiple boards (see Figure 4 on Page 9).

LOW SKEW CMOS PLL CLOCK DRIVER

Five "Q" outputs (Q0–Q4) are provided with less than 500 ps skew between their rising edges. The $\overline{Q5}$ output is inverted (180° phase shift) from the "Q" outputs. The 2X_Q output runs at twice the "Q" output frequency, while the Q/2 runs at 1/2 the "Q" frequency.

The VCO is designed to run optimally between 20 MHz and the 2X_Q F_{max} specification. The wiring diagrams in Figure 2 detail the different feedback configurations which create specific input/output frequency relationships. Possible frequency ratios of the "Q" outputs to the SYNC input are 2:1, 1:1, and 1:2.

The FREQ_SEL pin provides one bit programmable divide–by in the feedback path of the PLL. It selects between divide–by–1 and divide–by–2 of the VCO before its signal reaches the internal clock distribution section of the chip (see the block diagram on page 2). In most applications FREQ_SEL should be held high (÷1). If a low frequency reference clock input is used, holding FREQ_SEL low (÷2) will allow the VCO to run in its optimal range (>20MHz).

In normal phase–locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88LV915T in a static "test mode". In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment. The second SYNC input can be used as a test clock input to further simplify board–level testing (see detailed description on page 11).

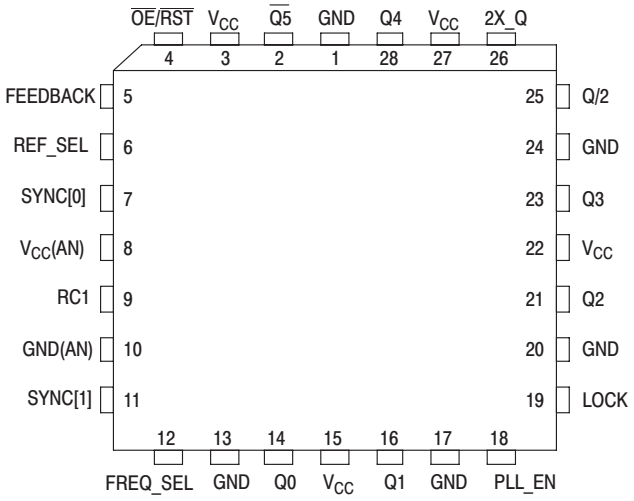
Pulling the $\overline{OE}/\overline{RST}$ pin low puts the clock outputs 2X_Q, Q0–Q4, $\overline{Q5}$ and Q/2 into a high impedance state (3–state). After the $\overline{OE}/\overline{RST}$ pin goes back high Q0–Q4, $\overline{Q5}$ and Q/2 will be reset in the low state, with 2X_Q being the inverse of the selected SYNC input. Assuming PLL_EN is low, the outputs will remain reset until the 88LV915 sees a SYNC input pulse.

A lock indicator output (LOCK) will go high when the loop is in steady–state phase and frequency lock. The LOCK output will go low if phase–lock is lost or when the PLL_EN pin is low. The LOCK output will go high no later than 10ms after the 88LV915 sees a SYNC signal and full 5V V_{CC}.

Features

- Five Outputs (Q0–Q4) with Output–Output Skew < 500 ps each being phase and frequency locked to the SYNC input
- The phase variation from part–to–part between the SYNC and FEEDBACK inputs is less than 550 ps (derived from the t_{PD} specification, which defines the part–to–part skew)
- Input/Output phase–locked frequency ratios of 1:2, 1:1, and 2:1 are available
- Input frequency range from 5MHz – 2X_Q FMAX spec.
- Additional outputs available at 2X and +2 the system "Q" frequency. Also a $\overline{Q}$ (180° phase shift) output available
- All outputs have ±36 mA drive (equal high and low) at CMOS levels, and can drive either CMOS or TTL inputs. All inputs are TTL–level compatible. ±88mA I_{OL}/I_{OH} specifications guarantee 50Ω transmission line switching on the incident edge
- Test Mode pin (PLL_EN) provided for low frequency testing. Two selectable CLOCK inputs for test or redundancy purposes. All outputs can go into high impedance (3–state) for board test purposes
- Lock Indicator (LOCK) accuracy indicates a phase–locked state

Pinout: 28–Lead PLCC (Top View)

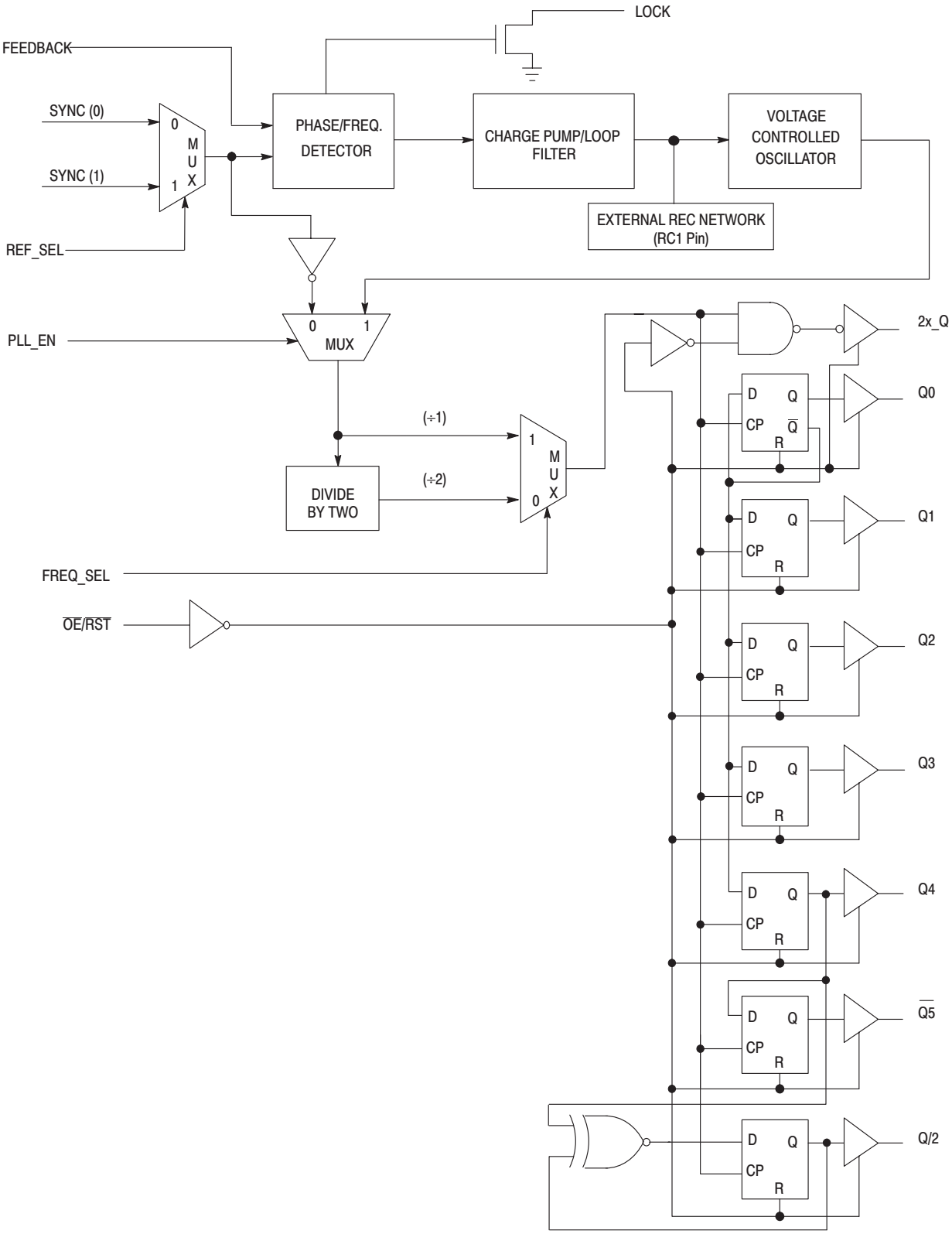


FN SUFFIX
PLASTIC PLCC
CASE 776–02

PIN SUMMARY

Pin Name	Num	I/O	Function
SYNC[0]	1	Input	Reference clock input
SYNC[1]	1	Input	Reference clock input
REF_SEL	1	Input	Chooses reference between sync[0] & Sync[1]
FREQ_SEL	1	Input	Doubles VCO Internal Frequency (low)
FEEDBACK	1	Input	Feedback input to phase detector
RC1	1	Input	Input for external RC network
Q(0–4)	5	Output	Clock output (locked to sync)
$\overline{Q5}$	1	Output	Inverse of clock output
2x_Q	1	Output	2 x clock output (Q) frequency (synchronous)
Q/2	1	Output	Clock output(Q) frequency ÷ 2 (synchronous)
LOCK	1	Output	Indicates phase lock has been achieved (high when locked)
$\overline{OE/RST}$	1	Input	Output Enable/Asynchronous reset (active low)
PLL_EN	1	Input	Disables phase–lock for low freq. testing
V_{CC},GND	11		Power and ground pins (note pins 8, 10 are “analog” supply pins for internal PLL only)

MC88LV915T BLOCK DIAGRAM



MAXIMUM RATINGS*

Symbol	Parameter	Limits	Unit
V_{CC}, AV_{CC}	DC Supply Voltage Referenced to GND	–0.5 to 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, Per Pin	±20	mA
I_{out}	DC Output Sink/Source Current, Per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current Per Output Pin	±50	mA
T_{stg}	Storage Temperature	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits	Unit
V_{CC}	Supply Voltage	3.3 ±0.3	V
V_{in}	DC Input Voltage	0 to V_{CC}	V
V_{out}	DC Output Voltage	0 to V_{CC}	V
T_A	Ambient Operating Temperature	0 to 70	°C
ESD	Static Discharge Voltage	> 1000	V

DC CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	V_{CC}	Guaranteed Limits	Unit	Condition
V_{IH}	Minimum High Level Input Voltage	3.0 3.3	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
V_{IL}	Minimum Low Level Input Voltage	3.0 3.3	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0 3.3	2.4 2.7	V	V_{IN} = V_{IH} or V_{IL} I_{OH}= –24mA
V_{OL}	Minimum Low Level Output Voltage	3.0 3.3	0.44 0.44	V	V_{IN} = V_{IH} or V_{IL} I_{OH}= 24mA
I_{IN}	Maximum Input Leakage Current	3.6	±1.0	µA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	3.6	2.0	mA	V_I = V_{CC} – 2.1V
I_{OLD}	Minimum Dynamic[3] Output Current	3.6	+50	mA	V_{OLD} = 1.25V
I_{OHD}		3.6	–50	mA	V_{OHD} =2.35V
I_{CC}	Maximum Quiescent Supply Current	3.6	TBD	µA	V_I = V_{CC}, GND

1. I_{OL} is +12mA for the $\overline{RST\_OUT}$ output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration 2.0ms, one output loaded at a time.

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$ SYNC Input	Rise/Fall Time, SYNC Input From 0.8V to 2.0V	—	5.0	ns
t_{CYCLE}, SYNC Input	Input Clock Period SYNC Input	$\frac{1}{f_{2X\_Q}/4}$	100	ns
Duty Cycle	Duty Cycle, SYNC Input	50% ± 25%		

FREQUENCY SPECIFICATIONS (T_A = 0°C to 70°C; V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Guaranteed Minimum	Unit
Fmax (2X_Q)	Maximum Operating Frequency, 2X_Q Output	100	MHz
Fmax ('Q')	Maximum Operating Frequency, Q0–Q3 Outputs	50	MHz

NOTE: Maximum Operating Frequency is guaranteed with the 88LV926 in a phase–locked condition.

AC CHARACTERISTICS (T_A =0° C to +70° C, V_{CC} = 3.3V ±0.3V, Load = 50Ω Terminated to $V_{CC}/2$)

Symbol	Parameter	Min	Max	Unit	Condition
$t_{RISE/FALL}$ Outputs	Rise/Fall Time, All Outputs (Between 0.8 to 2.0V)	0.5	2.0	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
$t_{PULSE\ WIDTH}$ (Q0–Q4, $\overline{Q5}$, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q3, Q4, $\overline{Q5}$, Q/2 @ $V_{CC}/2$	$0.5t_{CYCLE} - 0.5$ [1]	$0.5t_{CYCLE} + 0.5$ [1]	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
$t_{PULSE\ WIDTH}$ (2X_Q Output)	Output Pulse Width: 2X_Q @ 1.5V 40MHz 66MHz 80MHz 100MHz	 $0.5t_{CYCLE} - 1.5$ $0.5t_{CYCLE} - 1.0$ $0.5t_{CYCLE} - 1.0$ $0.5t_{CYCLE} - 1.0$	 $0.5t_{CYCLE} + 0.5$ $0.5t_{CYCLE} + 0.5$ $0.5t_{CYCLE} + 0.5$ $0.5t_{CYCLE} + 0.5$	ns	Into a 50Ω Load Terminated to $V_{CC}/2$
t_{CYCLE} (2x_Q Output)	Cycle–to–Cycle Variation 2x_Q @ $V_{CC}/2$ 40MHz 66MHz 80MHz 100MHz	 $t_{CYCLE} - 600ps$ $t_{CYCLE} - 300ps$ $t_{CYCLE} - 300ps$ $t_{CYCLE} - 400ps$	 $t_{CYCLE} + 600ps$ $t_{CYCLE} + 300ps$ $t_{CYCLE} + 300ps$ $t_{CYCLE} + 400ps$		
t_{PD} [2] SYNC Feedback	(With 1MΩ from RC1 to An V_{CC})			ns	
	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins) 66MHz 80MHz 100MHz	 –1.65 –1.45 –1.25	 –1.05 –0.85 –0.65		
t_{SKEWr} [3] (Rising) See Note **4**	Output–to–Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}/2$
t_{SKEWf} [3] (Falling)	Output–to–Output Skew Between Outputs Q0–Q4 (Falling Edges Only)	—	750	ps	All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}/2$
$t_{SKEWall}$ [3]	Output–to–Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling	—	750	ps	All Outputs Into a Matched 50Ω Load Terminated to $V_{CC}/2$
t_{LOCK} [4]	Time Required to Acquire Phase–Lock From Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t_{PZL} [5]	Output Enable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low
t_{PHZ},t_{PLZ} [5]	Output Disable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low

1. T_{CYCLE} in this spec is 1/Frequency at which the particular output is running.
2. The T_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.
3. Under equally loaded conditions and at a fixed temperature and voltage.
4. With V_{CC} fully powered–on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with C1 = 0.1µF, t_{LOCK} minimum is with C1 = 0.01µF.
5. The t_{PZL}, t_{PHZ}, t_{PLZ} minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

Applications Information for All Versions

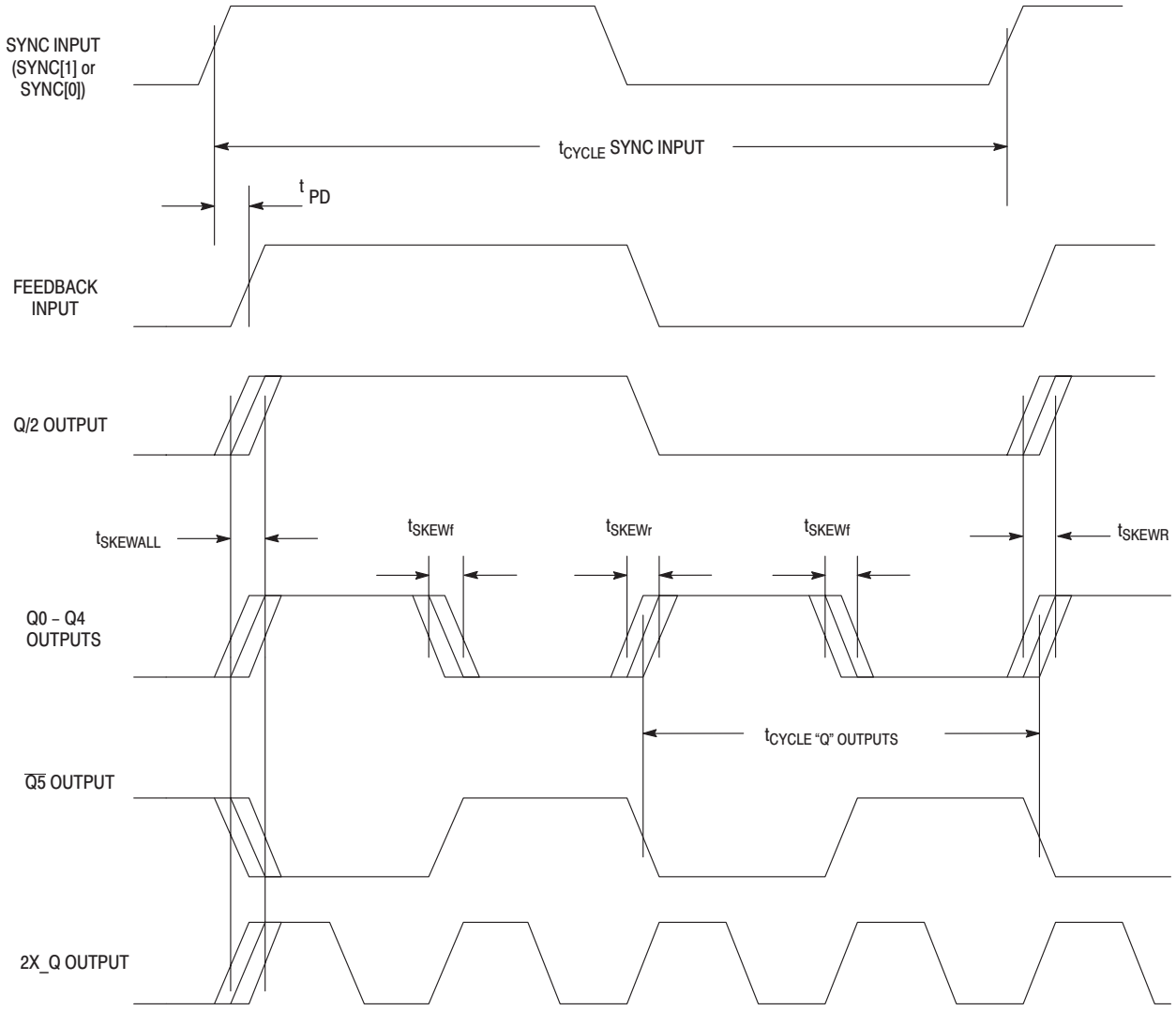
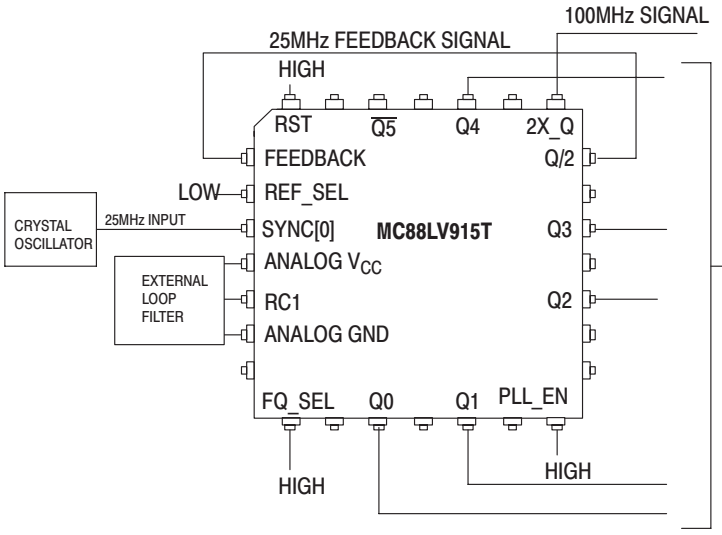


Figure 1. Output/Input Switching Waveforms and Timing Diagrams

(These waveforms represent the hook–up configuration of Figure 2a on page 7)

Timing Notes:

- The MC88LV915T aligns rising edges of the FEEDBACK input and SYNC input, therefore the SYNC input does not require a 50% duty cycle.
- All skew specs are measured between the $V_{CC}/2$ crossing point of the appropriate output edges.All skews are specified as 'windows', not as a ± deviation around a center point.
- If a "Q" output is connected to the FEEDBACK input (this situation is not shown), the "Q" output frequency would match the SYNC input frequency, the 2X_Q output would run at twice the SYNC frequency, and the Q/2 output would run at half the SYNC frequency.



1:2 Input to "Q" Output Frequency Relationship

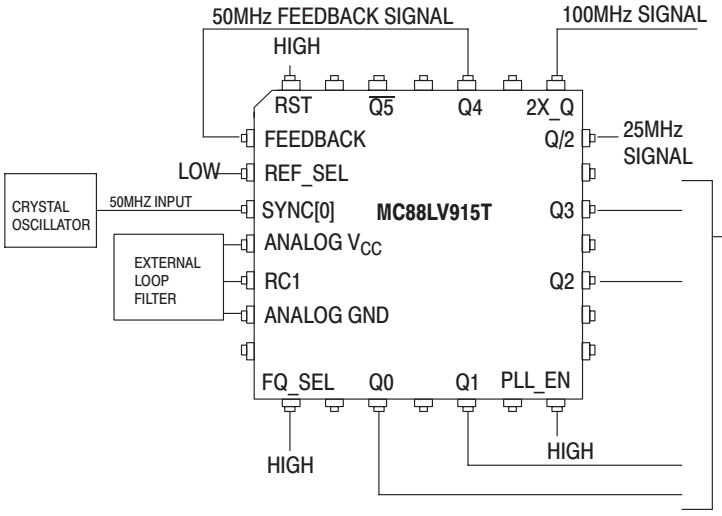
In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The "Q" outputs (Q0–Q4, $\overline{Q5}$) will always run at 2X the Q/2 frequency, and the 2X_Q output will run at 4X the Q/2 frequency.

Allowable Input Frequency Range:

5MHz to (2X_Q FMAX Spec)/4 (for FREQ_SEL HIGH)
2.5MHz to (2X_Q FMAX Spec)/8 (for FREQ_SEL LOW)

Note: If the $\overline{OE}/\overline{RST}$ input is active, a pull–up or pull–down resistor isn't necessary at the FEEDBACK pin so it won't when the fed back output goes into 3–state.

Figure 2a. Wiring Diagram and Frequency Relationships With Q/2 Output Feed Back



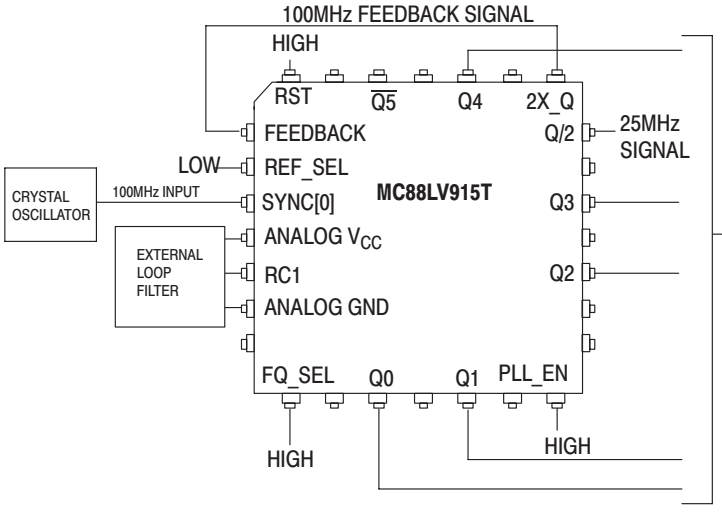
1:1 Input to "Q" Output Frequency Relationship

In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the "Q" outputs) will equal the SYNC frequency. The Q/2 output will always run at 1/2 the "Q" frequency, and the 2X_Q output will run at 2X the "Q" frequency.

Allowable Input Frequency Range:

10MHz to (2X_Q FMAX Spec)/2 (for FREQ_SEL HIGH)
5MHz to (2X_Q FMAX Spec)/4 (for FREQ_SEL LOW)

Figure 2b. Wiring Diagram and Frequency Relationships With Q4 Output Feed Back



2:1 Input to "Q" Output Frequency Relationship

In this application, the 2X_Q output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of 2X_Q and SYNC, thus the 2X_Q frequency will equal the SYNC frequency. The Q/2 output will always run at 1/4 the 2X_Q frequency, and the "Q" outputs will run at 1/2 the 2X_Q frequency.

Allowable Input Frequency Range:

20MHz to (2X_Q FMAX Spec) (for FREQ_SEL HIGH)
10MHz to (2X_Q FMAX Spec)/2 (for FREQ_SEL LOW)

Figure 2c. Wiring Diagram and Frequency Relationships with 2X_Q Output Feed Back

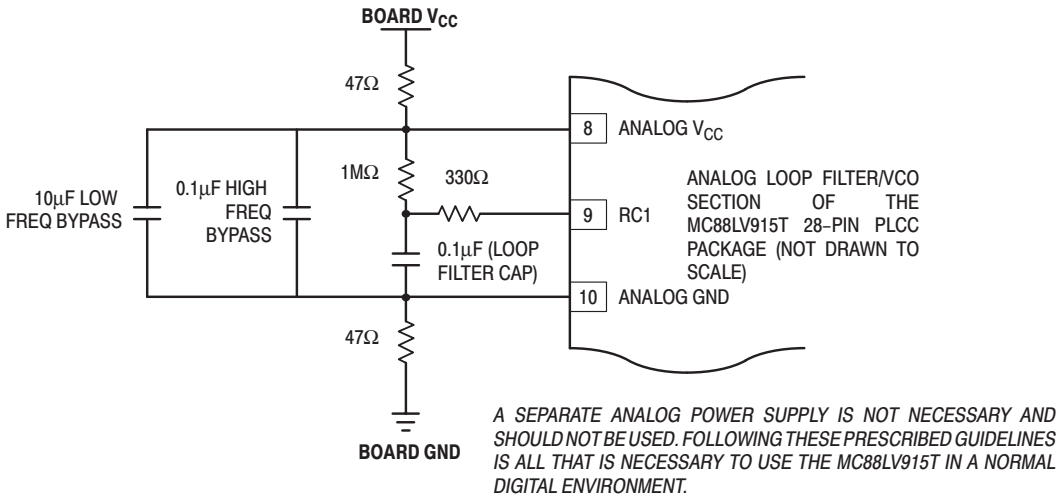


Figure 3. Recommended Loop Filter and Analog Isolation Scheme for the MC88LV915T

Notes Concerning Loop Filter and Board Layout Issues

1. Figure 3 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter–free operation:

1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

1b. The 47Ω resistors, the 10μF low frequency bypass capacitor, and the 0.1μF high frequency bypass capacitor form a wide bandwidth filter that will minimize the 88LV915T's sensitivity to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V_{CC} supply will cause no more than a 100pS phase deviation on the 88LV915T outputs. A 250mV step deviation on V_{CC} using the recommended filter values should cause no more than a 250pS phase deviation; if a 25μF bypass capacitor is used (instead of 10μF) a 250mV V_{CC} step should cause no more than a 100pS phase deviation.

If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88LV915T's digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 3 is to give the 88LV915T additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c. There are no special requirements set forth for the loop filter resistors (1MΩ and 330Ω). The loop filter capacitor (0.1μF) can be a ceramic chip capacitior, the same as a standard bypass capacitor.

1d. The 1M reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead–band. If the VCO (2X_Q output) is running above 40MHz, the 1MΩ resistor provides the correct amount of current injection into the charge pump (2–3μA). For the TFN55, 70 or 100, if the VCO is running below 40MHz, a 1.5MΩ reference resistor should be used (instead of 1MΩ).

2. In addition to the bypass capacitors used in the analog filter of Figure 3, there should be a 0.1μF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88LV915T outputs, in addition to reducing potential for noise in the 'analog' section of the chip. These bypass capacitors should also be tied as close to the 88LV915T package as possible.

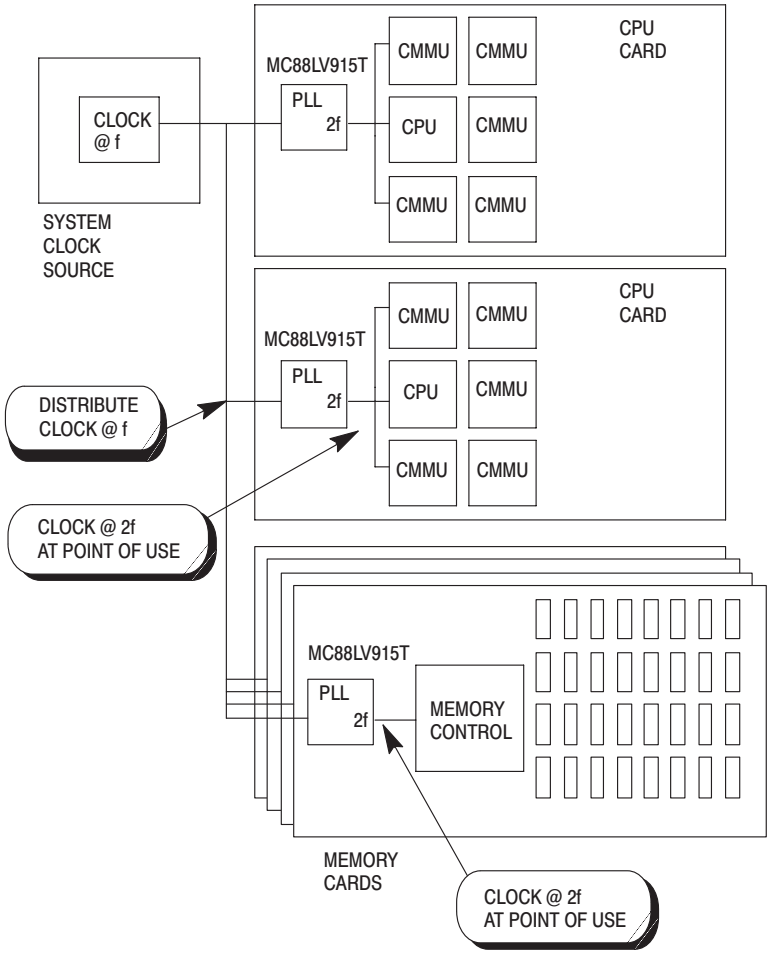


Figure 4. Representation of a Potential Multi–Processing Application Utilizing the MC88LV915T for Frequency Multiplication and Low Board–to–Board Skew

MC88LV915T System Level Testing Functionality

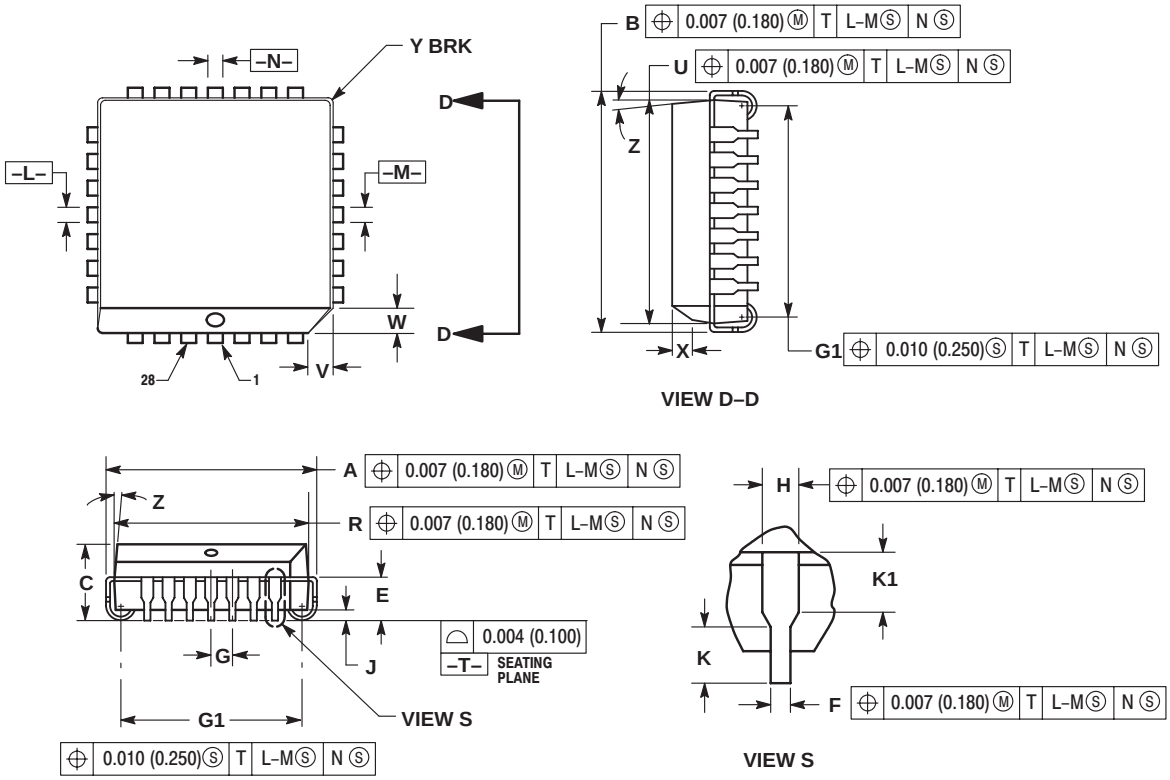
3–state functionality has been added to the 100MHz version of the MC88LV915T to ease system board testing. Bringing the $\overline{OE}/\overline{RST}$ pin low will put all outputs (except for LOCK) into the high impedance state. As long as the PLL_EN pin is low, the Q0–Q4, Q5, and the Q/2 outputs will remain reset in the low state after the $\overline{OE}/\overline{RST}$ until a falling SYNC edge is seen. The 2X_Q output will be the inverse of the SYNC signal in this mode. If the 3–state functionality will be used, a pull–up or pull–down resistor must be tied to the FEEDBACK input pin to prevent it from floating when the fedback output goes into high impedance.

With the PLL_EN pin low the selected SYNC signal is gated directly into the internal clock distribution network, bypassing and disabling the VCO. In this mode the outputs are directly driven by the SYNC input (per the block diagram). This mode can also be used for low frequency board testing.

Note: If the outputs are put into 3–state during normal PLL operation, the loop will be broken and phase–lock will be lost. It will take a maximum of 10mS (tLOCK spec) to regain phase–lock after the $\overline{OE}/\overline{RST}$ pin goes back high.

OUTLINE DIMENSIONS

FN SUFFIX
PLASTIC PACKAGE
CASE 776–02
ISSUE D



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

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Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan
Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe
IDT Europe, Limited
Prime House
Barnett Wood Lane
Leatherhead, Surrey
United Kingdom KT22 7DE
+44 1372 363 339

www.IDT.com

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