

Triple 4-3-3-Input Bus Driver

The MC10123 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with $V_{OL} = -2.1$ Vdc so that the bus may be terminated to -2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter-followers of the MC10123 are "turned-off." This eliminates discontinuities in the characteristic impedance of the bus.

The V_{OH} level is specified when driving a 25-ohm load terminated to -2.0 Vdc, the equivalent of a 50-ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the MC10123, higher impedance values may be used with this part. A typical 50-ohm bus is shown in Figure 1.

$P_D = 310$ mW typ/pkg (No Load)
 $t_{pd} = 3.0$ ns typ
 $t_r, t_f = 2.5$ ns typ (20%–80%)

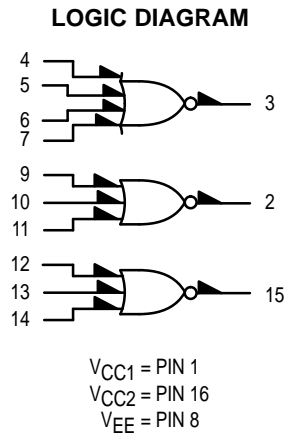
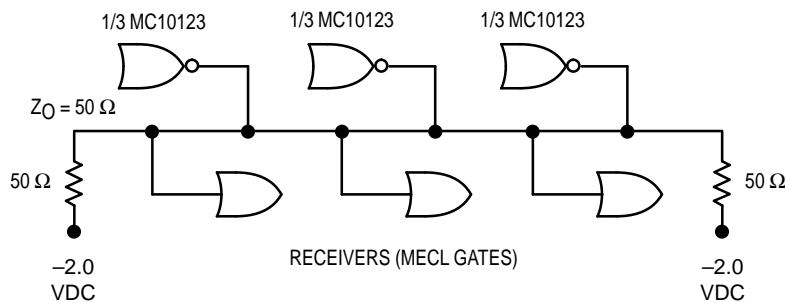
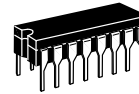


FIGURE 1 — 50-OHM BUS DRIVER (TYPICAL APPLICATION)



MC10123



L SUFFIX
CERAMIC PACKAGE
CASE 620-10

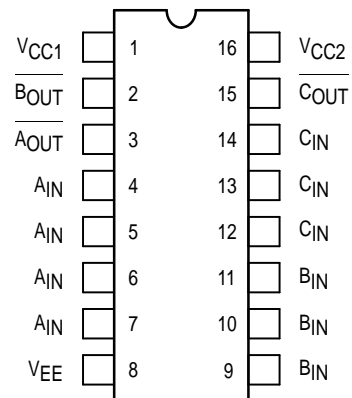


P SUFFIX
PLASTIC PACKAGE
CASE 648-08



FN SUFFIX
PLCC
CASE 775-02

DIP
PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.
 For PLCC pin assignment, see the Pin Conversion
 Tables on page 6–11 of the Motorola MECL Data
 Book (DL122/D).



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			-30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		82		71	75		82	mAdc
Input Current	I_{inH}	4		350			220		220	μ Adc
	I_{inL}	4			0.5					μ Adc
Output Voltage Logic 1	V_{OH}	3	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc
Output Voltage Logic 0	V_{OL}	3	-2.100	-2.030	-2.100		-2.030	-2.100	-2.030	Vdc
Threshold Voltage Logic 1	V_{OHA}	3	-1.080		-0.980			-0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	3		-2.100			-2.100		-2.100	Vdc
Switching Times (50 Ω Load)										ns
Propagation Delay	t_{4+3-}	3	1.2	4.6	1.2	3.0	4.4	1.2	4.8	
	t_{4-3+}	3	1.2	4.6	1.2	3.0	4.4	1.2	4.8	
Rise Time (20 to 80%)	t_{3+}	3	1.0	3.7	1.0	2.5	3.5	1.0	3.9	
Fall Time (20 to 80%)	t_{3-}	3	1.0	3.7	1.0	2.5	3.5	1.0	3.9	

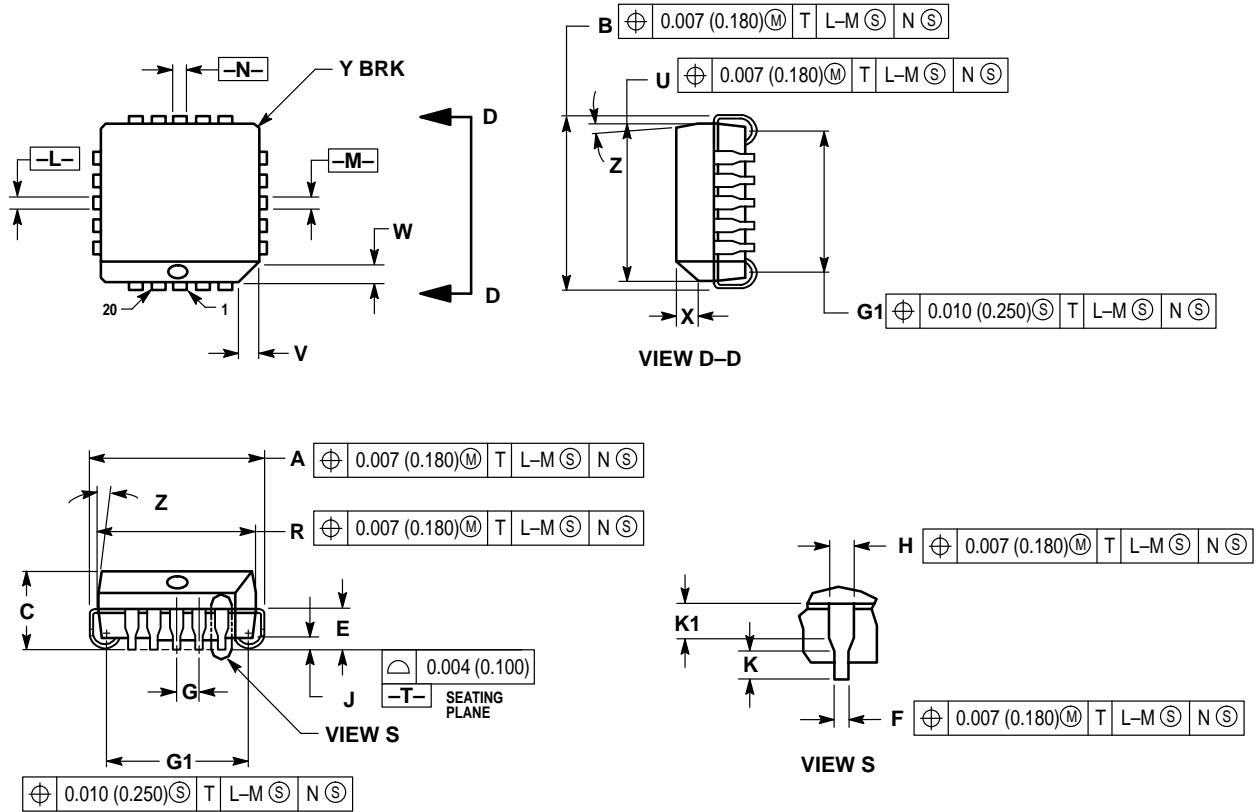
ELECTRICAL CHARACTERISTICS (continued)

			TEST VOLTAGE VALUES (Volts)						
			V_{IHmax}	V_{ILmin}	V_{IHmin}	V_{ILAmax}	V_{EE}		
@ Test Temperature									
-30°C			-0.890	-1.890	-1.205	-1.500	-5.2		
+25°C			-0.810	-1.850	-1.105	-1.475	-5.2		
+85°C			-0.700	-1.825	-1.035	-1.440	-5.2		
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V_{CC}) Gnd	
			V_{IHmax}	V_{ILmin}	V_{IHmin}	V_{ILAmax}	V_{EE}		
Power Supply Drain Current	I_E	8	4,5,6,7,9 10,11,12 13,14				8	1, 16	
Input Current	I_{inH}	4	4				8	1, 16	
	I_{inL}	4		4			8	1, 16	
Output Voltage Logic 1	V_{OH}	3					8	1, 16	
Output Voltage Logic 0	V_{OL}	3	4,5,6,7 9,12				8	1, 16	
Threshold Voltage Logic 1	V_{OHA}	3				4,5,6,7	8	1, 16	
Threshold Voltage Logic 0	V_{OLA}	3	9,12		4,5,6,7		8	1, 16	
Switching Times (50 Ω Load)						Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3				4	3	8	1, 16
	t_{4-3+}	3				4	3	8	1, 16
Rise Time (20 to 80%)	t_{3+}	3				4	3	8	1, 16
Fall Time (20 to 80%)	t_{3-}	3				4	3	8	1, 16

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

OUTLINE DIMENSIONS

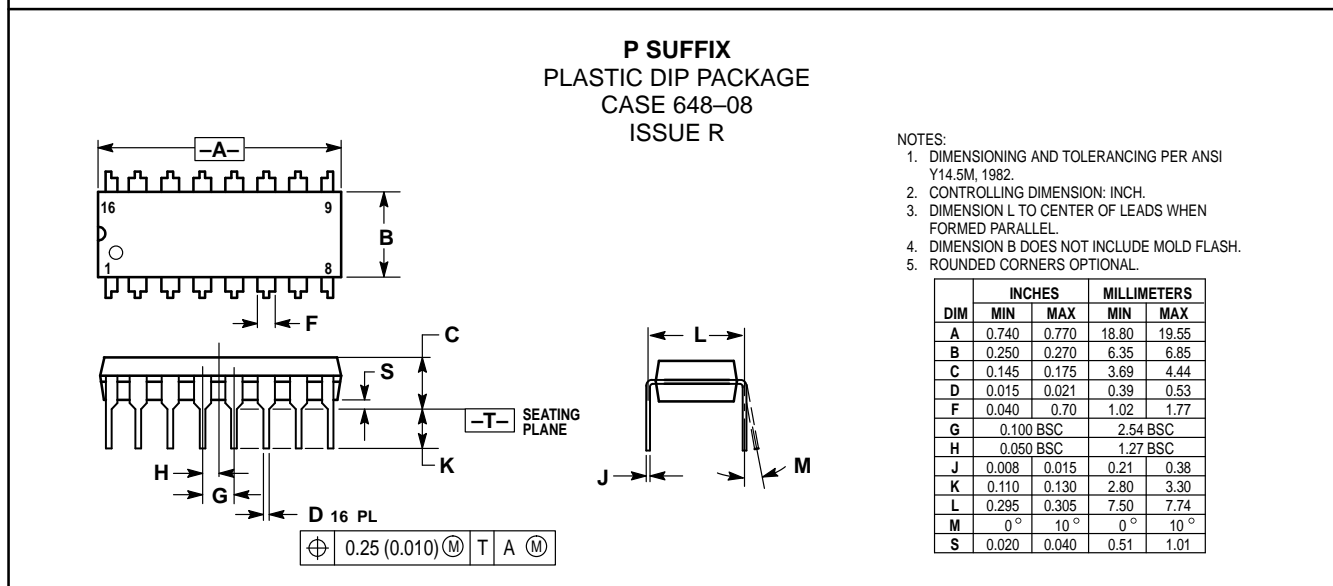
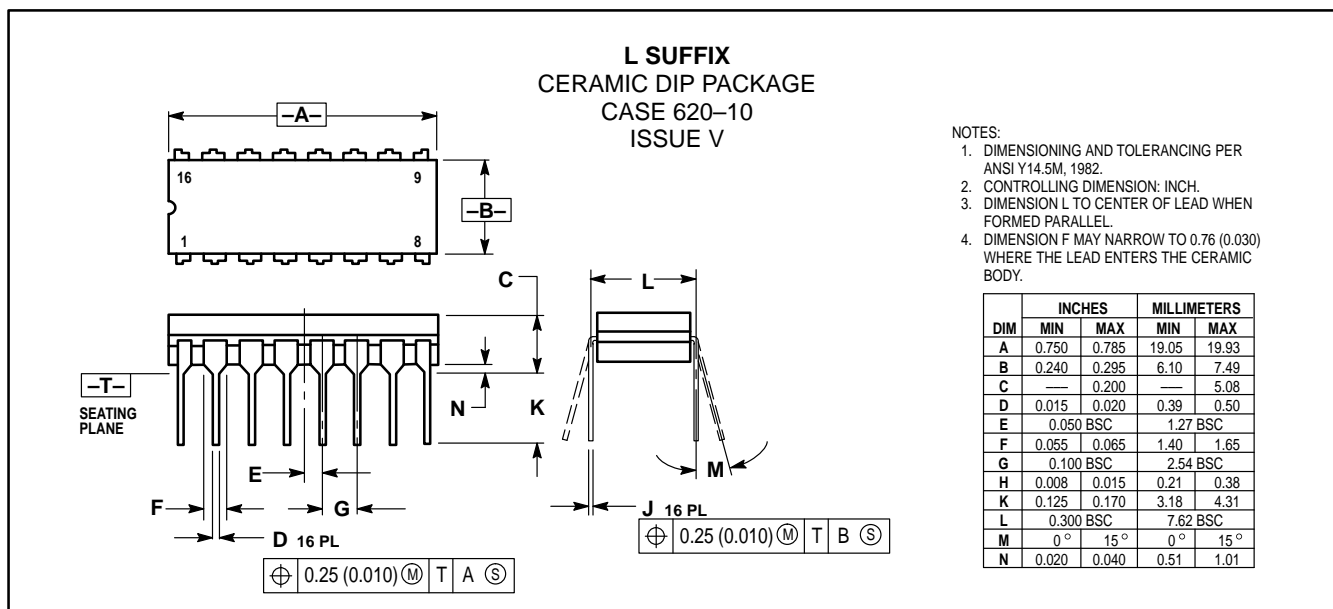
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775-02
ISSUE C




- NOTES:
- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
 - DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
 - DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
 - DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: INCH.
 - THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
 - DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

OUTLINE DIMENSIONS



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