MOTOROLA

MC10130

DUAL LATCH

The MC10130 is a clocked dual D type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{C_E}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock ($\overline{C}$).

Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

The set and reset inputs do not override the clock and D inputs. They are effective only when either $\overline{C}$ or $\overline{CE}$ or both are high.

P_D = 155 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ
t_r, t_f = 2.7 ns typ (20%–80%)

DUAL LATCH

L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

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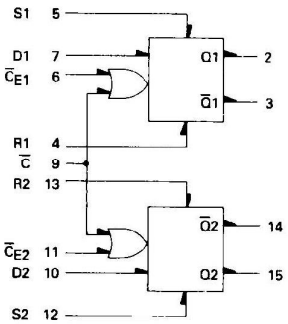
LOGIC DIAGRAM



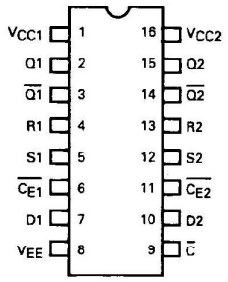
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

D	$\overline{C}$	$\overline{CE}$	Q_{n+1}
L	L	L	L
H	L	L	H
ϕ	L	H	Q_n
ϕ	H	L	Q_n
ϕ	H	H	Q_n

ϕ = Don't Care

DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-line Package.
For PLCC pin assignment, see tables on page 1-35.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one latch. The other latch is tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	MC10130 Test Limits −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	38	–	30	35	–	38	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	6,11	–	350	–	–	220	–	220	µAdc	6,11	–	–	–	8	1,16
		9	–	425	–	–	265	–	265		9	–	–	–		
		4,5,7	–	–	–	–	–	–	–		4,5	–	–	–		
		10,12,13	–	450	–	–	285	–	285		7,10,12,13	9	–	–		
	I_{inL}	4*	0.5	–	0.5	–	–	0.3	–	µAdc	–	4	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	4	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.080	–	-0.980	–	–	-0.910	–	Vdc	–	9	7	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	9	–	–	8	1,16
											+1.11 V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Switching Times (50 Ω Load) (See Figure 1) Propagation Delay	t_{7+2+}	2	1.0	3.6	1.0	2.5	3.5	1.0	3.8	ns	–	–	7	2	8	1,16
	t_{5+2+}					2.7			3.9		6	–	5			
	t_{4+2-}					2.7			3.9		6	–	4			
	t_{6-2+}			4.3		–	4.0		4.1		–	–	6			
Rise Time (20% to 80%)	t_{2+}			3.6	1.1	2.7	3.5	1.1	3.8		–	–	7			
Fall Time (20% to 80%)	t_{2-}			3.6	1.1	2.7	3.5	1.1	3.8		–	–	7			
Setup Time	t_{setup}	2	2.5	–	2.5	–	–	2.5	–	ns	①	–	6,7	2	8	1,16
Hold Time	t_{hold}	2	1.5	–	1.5	–	–	1.5	–	ns	①	–	6,7	2	8	1,16

*All other inputs are tested in the same manner