Low Voltage 1:2 Differential HSTL Clock Fanout Buffer

MC100ES8011H

The MC100ES8011H is a low voltage 1:2 Differential HSTL fanout buffer. Designed for the most demanding clock distribution systems, the MC100ES8011H supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are in high performance clock distribution in computing, networking and telecommunication systems.

1:2 DIFFERENTIAL HSTL CLOCK FANOUT DRIVER

D SUFFIX
8-LEAD SOIC PACKAGE
CASE 751-06

Features

- 1:2 differential clock fanout buffer
- 20 ps maximum device skew
- SiGe Technology
- Supports DC to 625 MHz operation
- HSTL compatible differential clock outputs
- HSTL compatible differential clock inputs
- 3.3V power supply
- Supports industrial temperature range
- Standard 8 lead SOIC package

ORDERING INFORMATION	
Device	**Package**
MC100ES8011HD	SO-8
MC100ES8011HDR2	SO-8

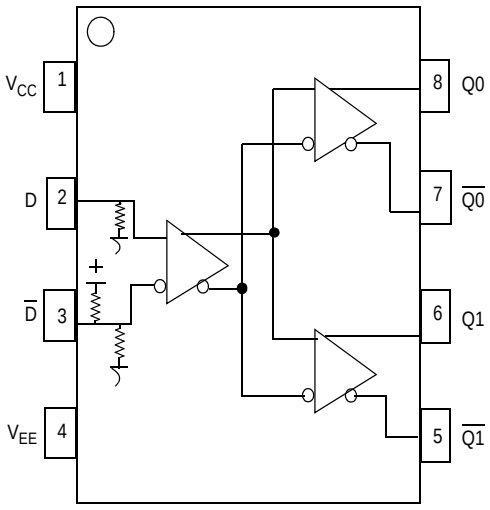


Figure 1. 8-Lead Pinout (Top View) **and Logic Diagram**

PIN DESCRIPTION	
Pin	**Function**
D, $\overline{D}$	HSTL Data Inputs
Qn, $\overline{Qn}$	HSTL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

Table 1. Absolute Maximum Ratings(1)

Symbol	Parameter	Conditions	Rating	Unit
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6V$	V_{CC} + 0.3 V_{EE} – 0.3	V V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 2. DC Characteristics (V_{CC} = 3.3 V ± 5%; T_J = 0°C to 110°C)(1)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
HSTL differential input signals (D, $\overline{D}$)						
V_{DIF}	Differential Input Voltage(2)	0.2			V	
$V_{X, IN}$	Differential Cross Point Voltage(3)	0.25	0.68 – 0.9	V_{CC} – 1.3	V	
I_{IN}	Input Current			±150	mA	$V_{IN} = V_X \pm 0.1V$
HSTL clock outputs (Q[0:1], $\overline{Q[0:1]}$)						
$V_{X, OUT}$	Output Differential Crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1			V	
V_{OL}	Ouput Low Voltage			0.4	V	
Supply Current						
I_{CC}	Maximum Quiescent Supply Current without output termination current		80	105	mA	V_{CC} pin (core)

1. DC characteristics are design targets and pending characterization.
2. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.
3. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 3. AC Characteristics (V_{CC} = 3.3 V ± 5%; T_J = 0°C to 110°C)[1] [2]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
HSTL differential input signals (D, $\overline{D}$)						
V_{DIF}	Differential Input Voltage (peak-to-peak)[3]	0.4			V	
$V_{X, IN}$	Differential Cross Point Voltage[4]	0.68		0.9	V	
f_{CLK}	Input Frequency			625	MHz	Differential
t_{PD}	Propagation Delay D to Q[0:1}	700	920	1200	ps	Differential
HSTL clock outputs (Q[0:1], $\overline{Q[0:1]}$)						
$V_{X, OUT}$	Output Differential Crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1			V	
V_{OL}	Ouput Low Voltage			0.5	V	
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak)	0.5			V	
$t_{SK(O)}$	Output-to-Output Skew			20	ps	Differential
$t_{SK(PP)}$	Output-to-Output Skew (part-to-part)			500	ps	Differential
$t_{SK(P)}$	Output Pulse Skew			100	ps	
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter			1	ps	
t_r / t_f	Output Rise/Fall Times	150		800	ps	20% to 80%

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
3. V_{DIF} (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
4. V_X (AC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (AC) range and the input swing lies within the V_{DIF} (AC) specification. Violation of V_X (AC) or V_{DIF} (AC) impacts the device propagation delay, device and part-to-part skew.

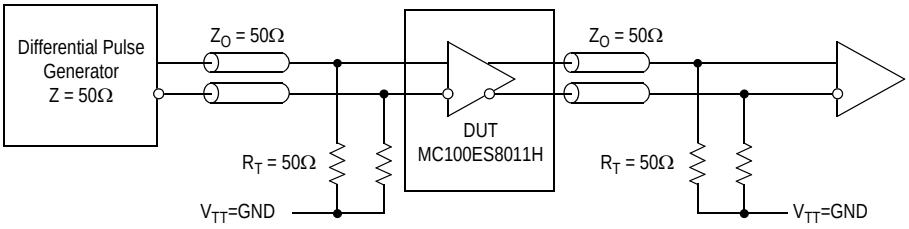


Figure 2. MC100ES8011H AC Test Reference

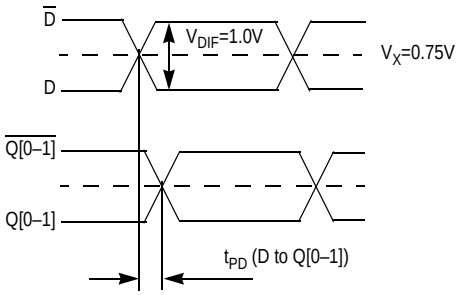
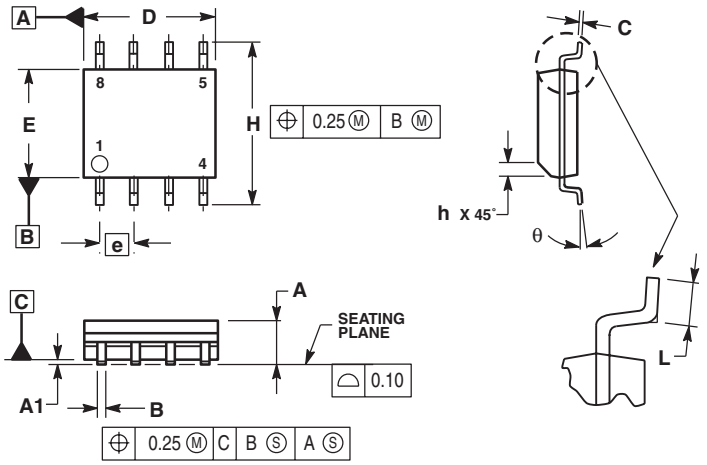


Figure 3. MC100ES8011H AC Reference Measurement Waveform (HSTL Input)

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

D SUFFIX
8-LEAD SOIC PACKAGE
CASE 751-06

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
netcom@idt.com
480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan
Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe
IDT Europe, Limited
Prime House
Barnett Wood Lane
Leatherhead, Surrey
United Kingdom KT22 7DE
+44 1372 363 339

www.IDT.com

XX-XXXX-XXXXX