3.3 V Dual Differential LVPECL to LVTTL Translator

The MC100ES60T23 is a dual differential LVPECL-to-LVTTL translator. The low voltage PECL levels, small package, and dual gate design is ideal for clock translation applications.

Features

- Maximum Frequency 500 MHz
- Differential LVPECL Inputs
- LVPECL Operating Range: V_{CC} = 3.0 V to 3.6 V
- Additive Phase Jitter, RMS: 0.18ps (typical)
- 24 mA LVTTL Compatible Outputs
- 8-Lead SOIC Package
- Ambient Temperature Range: –40°C to +85°C
- 8-Lead Pb-Free Package Available

D SUFFIX
8-LEAD SOIC PACKAGE
CASE 751-07

EF SUFFIX
8-LEAD SOIC PACKAGE
Pb-FREE PACKAGE
CASE 751-07

ORDERING INFORMATION	
Device	**Package**
MC100ES60T23D	SO-8
MC100ES60T23DR2	SO-8
MC100ES60T23EF	SO-8 (Pb-Free)
MC100ES60T23EFR2	SO-8 (Pb-Free)

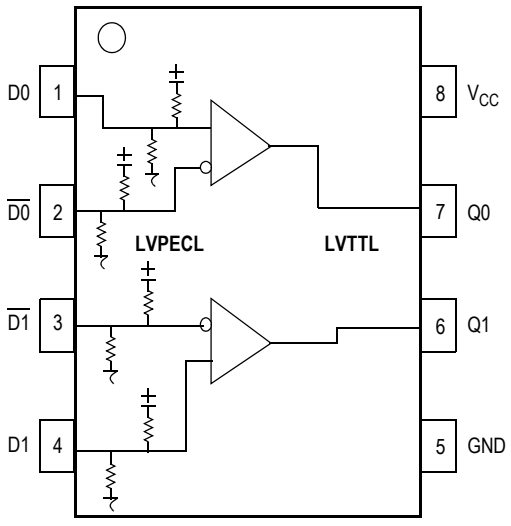


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

PIN DESCRIPTION	
Pin	**Function**
Qn	LVTTL Outputs
Dn, $\overline{Dn}$	LVPECL Differential Inputs
V_{CC}	Positive Supply
GND	Negative Supply

Table 1. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor	D $\overline{D}$	75 kΩ 112.5 kΩ
Internal Input Pullup Resistors		75 kΩ
ESD Protection	Human Body Model Machine Model	> 2000 V > 200 V
θ_{JA} Thermal Resistance (Junction to Ambient)	0 LFPM, 8 SOIC 500 LFPM, 8 SOIC	190°C/W 130°C/W

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 2. Absolute Maximum Ratings(1)

Symbol	Parameter	Conditions	Rating	Unit
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} and V_{EE}	3.9	V
V_{IN}	Input Voltage	V_{CC}–V_{EE} ≤ 3.6 V	V_{CC} + 0.3 V_{EE} – 0.3	V V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. LVPECL Input DC Characteristics (V_{CC} = 3.0 to 3.6 V; V_{EE} = 0 V); T_A = 40°C to 85°C

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CCH}	Power Supply Current (Outputs set to HIGH)		19	25	mA
I_{CCL}	Power Supply Current (Outputs set to LOW)		6.0	33	mA
V_{IH}	Input HIGH Voltage	V_{CC}–1165		V_{CC}–880	mV
V_{IL}	Input LOW Voltage	V_{CC}–1810		V_{CC}–1475	mV
V_{PP}	Differential Input Voltage(1)	0.15		1.3	V
V_{CMR}	Differential Cross Point Voltage(2)	V_{EE} +1.1		V_{CC}–0.65	V
I_{IH}	Input HIGH Current			150	µA
I_{IL}	Input LOW Current	–150			µA

1. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
2. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 4. LVTTL / LVCMOS Output DC Characteristics (V_{CC} = 3.0 to 3.6 V); T_A = 40°C to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –24 mA	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA			0.5	V
I_{OS}	Output Short Circuit Current		–140	–185	–275	mA

Table 5. AC Characteristics (V_{CC} = 3.0 to 3.6 V; V_{EE} = 0 V)[1]; T_A = 40°C to 85°C

Symbol	Characteristic		Test Conditions	Min	Typ	Max	Unit
f_{OUT}	Output Toggle Frequency[2]					500	MHz
t_{PD}	Propagation Delay			0.95		1.75	ns
t_{SK++} t_{SK--} t_{SKPP} t_{SKP}	Data Path Skew++[3] Data Path Skew--[3] Part-to-Part Skew[3] Pulse Skew[3]					120 140 500 250	ps ps ps ps
t_{JIT}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	CLK0/Q0 CLK0/Q0 CLK1/Q1 CLK1/Q1	125MHz, 12kHz - 20MHz 156.25MHz, 12kHz - 20MHz 125MHz, 12kHz - 20MHz 156.25MHz, 12kHz - 20MHz		0.40 0.18 0.38 0.21		ps ps ps ps
V_{PP}	Input Voltage Swing (Differential)[4]			200		1300	mV
V_{CMR}	Differential Cross Point Voltage			V_{EE}+1.2		V_{CC}–0.3	V
t_r / t_f	Output Rise/Fall Times (0.8 V – 2.0 V)			50		250	ps

1. LVTTL output R_L = 500 Ω to GND and C_L = 20 pF to GND. Refer to **Figure 2**.
2. f_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
3. Skews are measured between outputs under identical conditions.
4. 200 mV input guarantees AC Characteristics.

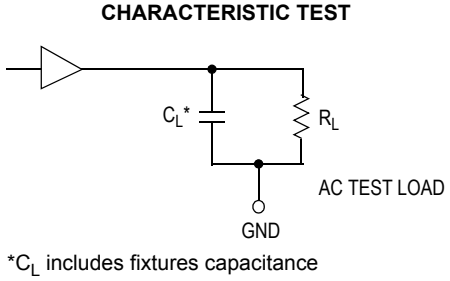
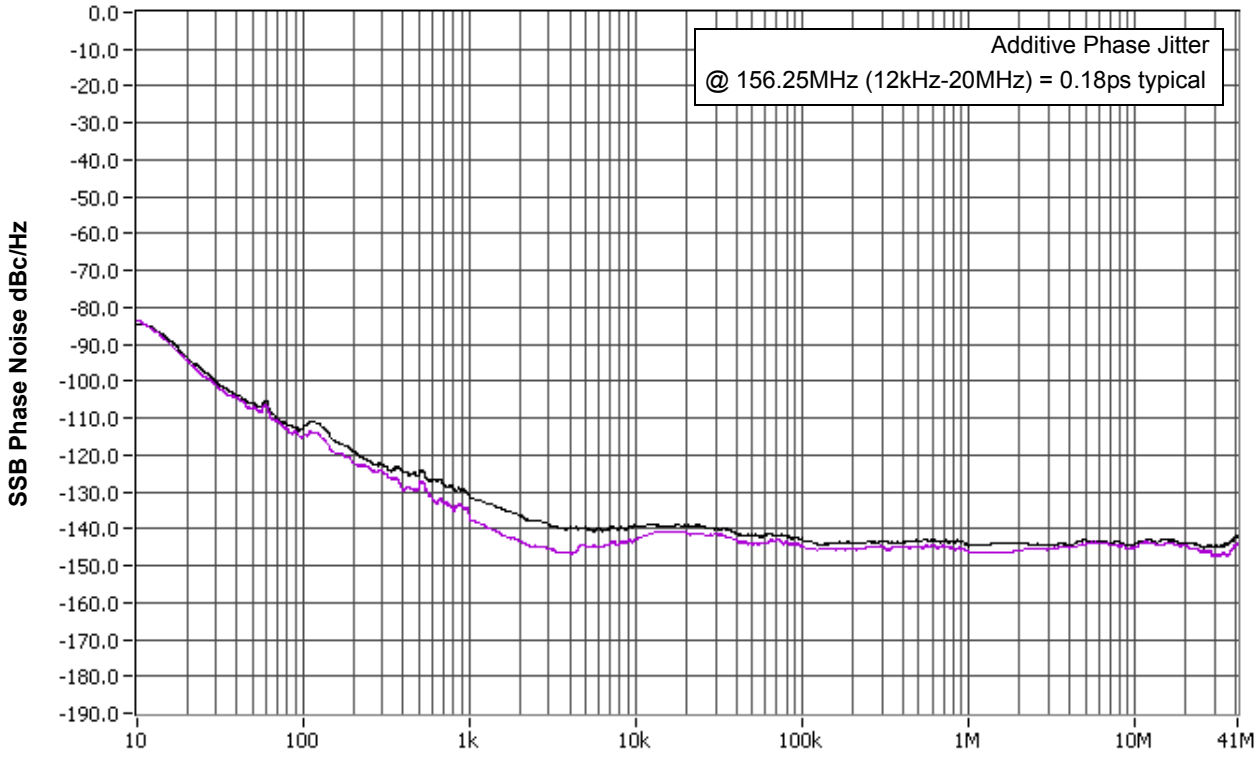


Figure 2. TTL Output Loading Used for Device Evaluation

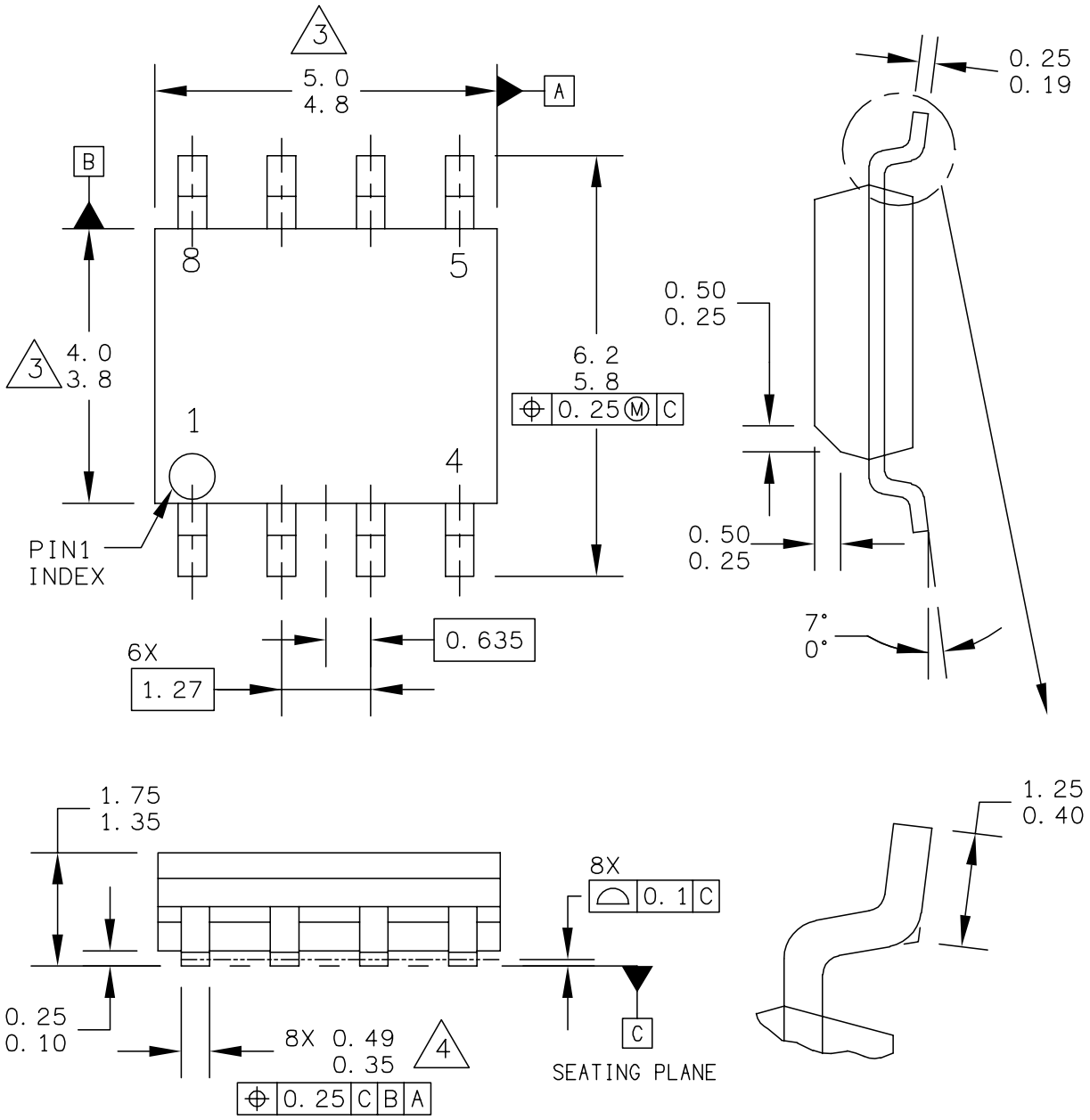
ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the dBc Phase Noise. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a dBc value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

PACKAGE DIMENSIONS



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8-LEAD SOIC PACKAGE

PACKAGE DIMENSIONS

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

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