Data Sheet

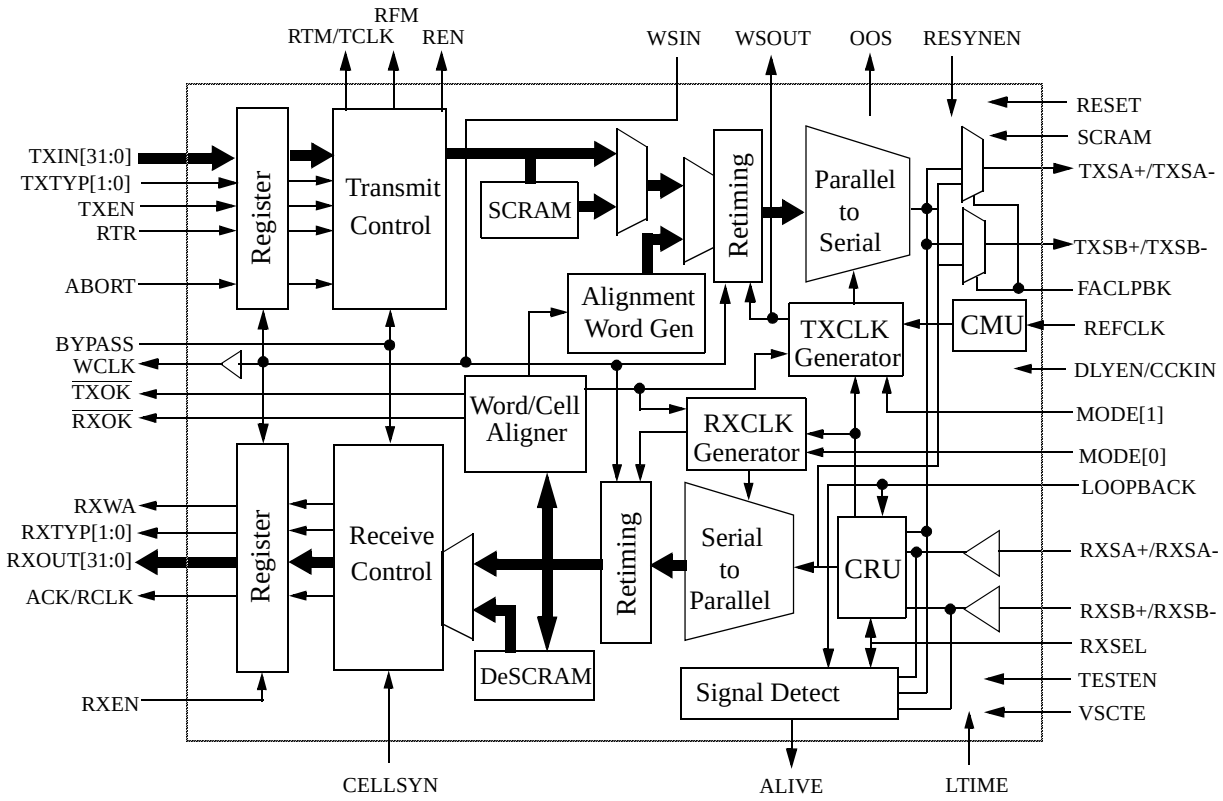
VSC870

High Performance Serial Backplane Transceiver

Features

- Performs 32-Bit Parallel to Serial and Serial to Parallel Functions
- Serial Data Rates are 2.0Gb/s
- Designed in Conjunction with the VSC880 Serial Crosspoint Switch
- Performs Bit Alignment, Word Alignment and Cell Alignment
- Three Modes of Operation: Distributed Control *Packet Mode*, Central Control *Cell Mode* and *Direct Mode*
- Support for Multicast and Multiple Input Queues
- Supports Priorities, Camp-on and Retransmission Capability in Packet Mode
- Built-in Flow Control Channel in Packet Mode
- Supports Cell Synchronization in Cell Mode
- Interfaces Directly with Industry Standard FIFOs
- Contains Redundant Serial I/Os and Internal Loopback Mode
- 5V Tolerant TTL Inputs
- Single 3.3V Power Supply
- Available in 192 BGA Package

VSC870 Block Diagram



© *VITESSE SEMICONDUCTOR CORPORATION* • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

General Description

The VSC870 serial backplane transceiver has been designed to operate with the VSC880 serial crosspoint switch to establish a synchronous high performance switching system. The VSC870 can also connect directly to another transceiver to act as a high bandwidth backplane interconnect link. The transmitter converts a 32-bit parallel interface operating at 62.5Mb/s to a 34-bit serial data stream operating a 2.125Gb/s. The receiver converts a 34-bit serial interface operating at 2.125Gb/s to a 32-bit parallel interface operating at 62.5Mb/s. The transceiver performs automatic bit alignment, word alignment and cell alignment to a connected switch chip or another transceiver. The parallel interface has been designed with industry-standard FIFOs in mind to provide such features as automatic packet retransmission, multicast with retransmission, camp-on and support for virtual output queues. These features can also be bypassed to give the user direct control of the serial data stream. In addition, the transceiver and switch chip can operate in a early arbitration mode that greatly improves bandwidth utilization. The transceiver also contains a built-in a flow control channel and redundant serial I/O buffers.

The transceiver and switch chip have been optimized to be used in both distributed-controlled packet-based switching systems (Packet Mode), and centrally-controlled cell-based switching systems (Cell Mode). The transceiver can also be directly connected to another transceiver (Direct Mode) for backplane interconnect applications. The transceiver runs off a 3.3V power supply. The serial I/O buffers contain on-chip termination resistors (See Figure 19).

Package Pin Descriptions

Symbol	*Name*	*I/O*	*Freq Type*	*Description*
TXIN[31:0]	Transmit Parallel Data In	I	62.5Mb/s TTL	32-bit parallel data input for the transmit side.
TXTYP[1:0]	Transmit Word Type	I	62.5Mb/s TTL	If BYPASS is LOW, these signals designate the transmit word type. If BYPASS is HIGH, these signals directly control the overhead bits sent on the serial channel.
TXEN	Transmit Enable	I	62.5Mb/s TTL	When TXEN is HIGH, TXIN[31:0], TXTYP[1:0] are loaded in to the transceiver on the next WCLK. When TXEN is LOW, the transceiver ignores TXIN[31:0] and TXTYP[1:0] and sends IDLE words at the serial output.
RTR	Ready To Receive	I	62.5Mb/s TTL	When RTR is HIGH, the receiving side memory system is ready to receive data. If LOW, it sends a back pressure (flow control) signal to the source port card telling it to stop sending data. In Cell Mode, set RTR LOW to cell synchronize to the external cell clock. If RTR is HIGH, cell clock is recovered from the bit stream.
RTM/TCLK	Retransmit Mode/ Transmit Cell Clock	O	62.5Mb/s TTL	In Packet Mode, when BYPASS is LOW, RTM/TCLK is set HIGH at the beginning of each data transmission and set LOW when the data packet has been successfully sent to all outputs. In Cell Mode, a HIGH pulse represents the transmit cell clock.
RFM	Read From Mark	O	62.5Mb/s TTL	When BYPASS is LOW, RFM is set HIGH whenever a retransmission of data is required due to contention for destination ports.
$\overline{\text{TXOK}}$	Transmit signal OK	O	<1MHz TTL	This signal is LOW if MODE[1] is HIGH and the transceiver is word aligned on the transmit side. After initialization it will go HIGH for one word clock if there is a cell clock error.
REN	Read Enable	O	62.5Mb/s TTL	When REN is HIGH, the transceiver is ready to read data at TXIN[31:0] and TXTYP[1:0]. This signal can be forced low by the received flow control signal.
MODE[1:0]	Mode Control	I	<1MHz TTL	These mode control pins are used to configure link synchronization. See Section 1.5.
TXSA+/ TXSA-	Transmit Serial Output A	O	2.125Gb/s LVDS	High speed serial differential transmit channel A
TXSB+/ TXSB-	Transmit Serial Output B	O	2.125Gb/s LVDS	High speed serial differential transmit channel B
LOOPBACK	Loop Back	I	<1MHz TTL	When LOOPBACK is HIGH, the CRU and signal detector select the serial data output channel as an input.
RXSA+/ RXSA-	Receive Serial Input A	I	2.125Gb/s LVDS	High speed serial differential receive channel A
RXSB+/ RXSB-	Receive Serial Input B	I	2.125Gb/s LVDS	High speed serial differential receive channel B

© ***VITESSE*** *SEMICONDUCTOR CORPORATION* • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

Symbol	*Name*	*I/O*	*Freq Type*	*Description*
RXSEL	Receive Input Select	I	<1MHz TTL	When RXSEL is LOW and LOOPBACK is LOW, RXSA is selected as the input to the CRU and RXSB is selected as the input to the Signal Detector. When RXSEL is HIGH and LOOPBACK is LOW, RXSB is selected as the input to the CRU and RXSA is selected as the input to the Signal Detector.
ALIVE	Redundant Input Alive	O	<1MHz TTL	This output is high if at least one edge transition is detected every word clock period on the redundant input serial line.
$\overline{\text{RXOK}}$	Receive Signal OK	O	<1MHz TTL	This signal goes LOW if the VSC870 is word aligned on the receive side. After initialization, it goes HIGH if there is error in the IDLE words.
RXEN	Receive Enable	I	62.5Mb/s TTL	When RXEN is LOW, the RXOUT[31:0] and RXTYP[1:0] outputs become high impedance.
RXOUT[31:0]	Receive Parallel Data Out	O	62.5Mb/s TTL	32-bit parallel data output for the receive side.
RXTYP[1:0]	Receive Word Type	O	62.5Mb/s TTL	If BYPASS is LOW, these signals tell the received word type. If BYPASS is HIGH, these signals reflect the overhead bits received on the serial channel.
RXWA	Receive Word Available	O	62.5Mb/s TTL	When RXWA is LOW, RXTYP[1:0] and RXOUT[31:0] is an IDLE word.
ACK/RCLK	Acknowledge / Receive Cell Clock	O	62.5Mb/s TTL	In Packet Mode, the ACK signal will be set high if a Connection Request on the transmit side is granted. In Cell mode, a high pulse represents the receive cell clock.
ABORT	Connection Request Abort	I	62.5Mb/s TTL	When BYPASS is LOW and ABORT is HIGH, the connection request and data transmission process is aborted.
WSIN	Word Synch In	I	62.5MHz TTL	The WSIN signal provides the word clock input and must be driven by a signal frequency locked to the WSOUT signal either from itself or another transceiver.
WSOUT	Word Synch Out	O	62.5MHz TTL	The WSOUT signal is the internally generated word clock and is synchronized to the transmit word clock.
RESYNEN	Resync Enable	I	<1MHz TTL	If RESYNEN is HIGH and the transceiver detects a link error, it will start the Link Initialization process.
OOS	Out Of Sync	O	<1MHz TTL	If OOS is HIGH, the transceiver is in the link initialization process. It is LOW during normal operation.
SCRAM	Scramble Enable	I	<1MHz TTL	If SCRAM is HIGH, data words will be scrambled and descrambled.
BYPASS	Bypass Mode	I	<1MHz TTL	BYPASS is set HIGH for direct control and monitoring of the overhead bits in the serial data streams as in cell mode and direct mode. This also disables the transceiver Packet Mode functions.
CELLSYN	Cell Synchronization Enable	I	<1MHz TTL	CELLSYN is set HIGH to allow cell synchronization during link initialization.

Symbol	*Name*	*I/O*	*Freq Type*	*Description*
DLYEN/ CCKIN	Delay Enable/Cell Clock Input	I	<1MHz TTL	If BYPASS is LOW, this signal can be set HIGH to enable REN delay mode. In Cell Mode, DLYEN/CCKIN can be used as an input for cell clock alignment.
FACLPBK	Facility Loopback	I	<1MHz TTL	When this signal is HIGH, the serial input is looped back to the serial output. It should be normally set LOW.
WCLK	Word Clock	O	62.5MHz TTL	The word clock is a delayed version of the WSIN signal.
REFCLK	Local Reference Clock	I	62.5MHz TTL	A 62.5 MHz local reference clock that is used to keep the CRU close to the incoming bit clock frequency before the alignment process begins. Is also used as a reference clock for the CMU.
RESET	Reset	I	<1MHz TTL	Global chip reset (active HIGH).
TESTEN	Scan Test Enable	I	<1MHz TTL	When TESTEN is HIGH, the REFCLK is used in place of the bit clock for low speed testing. Used for ATE testing only. Set to logic LOW during normal operation.
LTIME	Loop Time Mode	I	62.5Mb/s TTL	LTIME is set HIGH to use the recovered bit clock for the transmit side.
VSCTE	NOR Chain Test Enable	I	<1MHz TTL	Used for ATE testing of the parametric NOR chain in the I/O frame. Set to logic LOW during normal operation.
VDDA	CMU Power Supply	P	3.3V	Clean power supply for CMU
VSSA	CMU Ground	P	0V	Clean ground for CMU

© ***VITESSE*** *SEMICONDUCTOR CORPORATION* • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

Functional Description

The VSC870 transceiver can be used in one of the three operation modes: Packet Mode, Cell Mode and Direct Mode. In Packet mode, the VSC870 is intended to work in conjunction with the VSC880 switch chip to provide a self routing switching system and to support variable length data packets. In Cell Mode, the transceiver works in conjunction with the VSC880 switch chip to provide a cell synchronized switching system. In this mode, it can support only fixed length data packets (cells), and routing decisions are carried out in a user defined controller chip and synchronized to a cell clock. In Direct mode, the VSC870 can connect to other transceivers to provide a high bandwidth serial backplane data link.

The following sections give a detailed description of generic features which are provided in all three modes, followed by the operation of the transceiver in each mode. Most of the discussions in this data sheet include some of the switch chip functions (see the VSC880 data sheet).

1.0 Common Features

1.1 Synchronization

1.1.1 Link Characteristic

The serial link is used to connect the transceivers to the switch chip or to other transceivers. These links operate at 2.125Gb/s and are initialized simultaneously at power up, or separately when a link error occurs. A link is first bit synchronized, then word synchronized and, if CELLSYN is HIGH, cell synchronized. In Packet or Cell mode, the switch acts as the master, generating the bit clock along with the word and cell boundary information. The transceivers act as slaves, recovering the bit clock, word clock and cell clock. In Direct mode, the transceivers can be configured as either masters or slaves using the MODE[1:0] signals, with the masters generating the bit and word clocks. The transceiver also contains redundant serial inputs and outputs which can be used with a redundant switch chip or redundant transceiver.

1.1.2 Data Scrambling

A 15% edge transition density must be guaranteed on the serial data links for the CRU to work properly. All command words and connection request words contain this required density. In order to get this density on data words, scrambling is employed. If SCRAM is set HIGH, the 32-bit data words are scrambled in the transmitter and de-scrambled in the receiver with a $(1+X^1+X^7)$ pattern to guarantee high transition density. This is the same pattern used in SONET scrambling. In all operating modes, data words are recognized by TXTYP[1:0] = 01 or 10. Words such as the connection request and header word in Packet Mode or cell clock in Cell Mode or the IDLE word in Direct Mode are used to initiate the scrambling pattern. If the user can guarantee edge densities greater than or equal to 15%, scrambling can be turned off by setting SCRAM = LOW.

1.1.3 Bit Synchronization

In Packet and Cell Mode, the switch acts as the source of the bit clock. It multiplies the local 62.5MHz word clock by 34 to generate a 2.125GHz clock, and uses this clock to serialize the 32-bit data word and 2 overhead bits.

The transceiver receives and feeds this serial data stream to a digital CRU to recover the bit clock and deserialize the data stream to a 32 bit word plus 2 overhead bits at 62.5MHz. The transceiver also uses this recovered clock to serialize its transmit data words that are sent to the switch. In this way, the switch and all the transceivers are frequency-locked to one clock source which is provided by the word clock on the switch card. The transceiver provides its own CMU which multiplies a local REFCLK by 34. The output of the CMU helps the CRU obtain lock and provides the clock source for the transceiver in loopback mode. This local REFCLK must be within 100ppm of the switch chip reference clock frequency. In Direct Mode, the master transceiver uses the CMU to provide a clock for the transmit data. The slave receivers recover the clock from the serial bit streams.

1.1.4 Word Synchronization

During power up or at reset, the transceiver can initiate the word synchronization process. First, the transceiver sends reset patterns to the switch (or the master transceiver in Direct mode) to request that the switch starts the initialization process. The switch, upon receiving this request, will send out special ALIGN words. The transceiver receives this serial data stream from the switch, and uses the RXCLK Generator to adjust the receive word clock boundary one bit at a time until the Word/Cell Aligner detects proper alignment. Upon detecting the correct word alignment, the $\overline{\text{RXOK}}$ signal is set LOW and the word alignment process is started on the transmit side. In this process, the transceiver continuously sends ALIGN words to the switch using the Alignment Word Generator. The switch uses its own word clock to detect this ALIGN word. If the transmitters word is not aligned to the switch chip word clock when it arrives at the switch, the switch chip continues to send out ALIGN words. After receiving every 32 ALIGN words from the switch chip, the transceiver changes its transmit word boundary by one bit position using the TXCLK Generator and then repeats the process (this limits the distance from the transceiver to the switch to less then 180nS one way). If the switch detects this ALIGN word correctly, it sends IDLE words to the transceiver to signal that the transmitter has now word synchronized with the switch. When the transceiver detects these IDLE words, the signal $\overline{\text{TXOK}}$ goes LOW and the parallel data signals TXIN[31:0], TXTYP[1:0], RXOUT[31:0] and RXTYP[1:0] are then phase aligned to the word clock (WSOUT).

The transmit word clock is output on the pin WSOUT. If a single transceiver is used on a port card, WSOUT must be tied directly to WSIN. The signal WSIN is the clock input for all of the transceiver parallel logic and provides the word clock output (WCLK). Retiming blocks are used in the transceiver to span the phase boundary between WSIN and the transmit word clock and the receive word clock. If two or more transceivers are used in parallel on a port card in order to increase bandwidth, each will have its own transmit word clock. Since these word clocks are derived from the same source on the switch card, they will have the same frequency but a phase difference of up to 8nS. This phase difference (skew) depends on the I/O delay of the switch and transceiver and the serial data line delay between these chips. To properly phase align all transceiver parallel interfaces, one transceiver acts as the master, providing its WSOUT signal not only to its own WSIN, but the WSIN on all other transceivers on the port card (see Application Note 32: Design Guide for a Cell Based Switch with Central Control). This means that the parallel logic blocks on all transceivers are clocked by the same source derived from the transmit word clock of the master transceiver. In this way, skew between the parallel interfaces on all transceivers is minimized. Other logic on the port card can be clocked using WSOUT of the master transceiver, or the WCLK output of any transceiver which is a delayed version of WSOUT. A phase shifted word clock can also be used to drive WSIN provided that it is frequency locked to the WSOUT signal. In this way, both the receive and transmit parallel interfaces can be phase aligned to this word clock.

© VITESSE SEMICONDUCTOR CORPORATION • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

1.1.5 Cell Synchronization

If the CELLSYN signal is set HIGH, after the word synchronization process, the transceiver starts the cell synchronization process. In this process, the transceiver detects the received cell clock sent from the switch. The cell clock is embedded in the command words with overhead bits '00' as described in section 3.2. The received cell clock is output on ACK/RCLK. The switch chip connects each port to itself after link initialization. By sending a special ALIGN word to itself, the transceiver can adjust the transmit cell clock (RTM/TCLK) until it is properly phase shifted relative to the received cell clock. If cells are sent from the transceiver aligned to this transmit cell clock, they will arrive at the switch aligned to the master cell clock which is originated at the switch. The received cell clock on the serial link is therefore shifted by N word clocks to create a phase shifted cell clock which is output on RTM/TCLK. An on-chip counter provides this phase shift, with the frequency and phase shift determined during the cell synchronization process. For this alignment process to work, the minimum cell size is 13 words (52 bytes).

1.1.6 Cell Synchronization for Multiple Transceivers

If two or more transceivers are used in parallel on a port card in order to increase bandwidth, skew between signals could cause the transmit cell clock (RTM/TCLK) in one or more transceivers to be shifted in phase by one word clock relative to the other transceivers. To adjust out this offset, a marker cell clock can be sent to both transceivers. This is done by sending the signal RTM/TCLK from the master transceiver to the DLYEN/CCKIN input on the slave transceivers. At the end of the cell synchronization process, the pipeline offset is adjusted out using this marker cell clock. See Application Note 32 for more details.

1.1.7 Link Error Detection

Receive errors are declared if the transceiver detects a bit pattern error in an IDLE word in the received serial data by generating a HIGH pulse on $\overline{\text{RXOK}}$. In cell mode, if an IDLE word is received at the end of the cell period and it does not contain the embedded cell clock, or it receives an embedded cell clock at the wrong time, it generates a HIGH pulse on $\overline{\text{TXOK}}$. This error is stored internally and if the RESYNEN goes HIGH, the VSC870 will start the link initialization process. The $\overline{\text{RXOK}}$ and $\overline{\text{TXOK}}$ signals can therefore be tied to the RESYNEN signal to start the link initialization process immediately, or the user logic can monitor the $\overline{\text{RXOK}}$ and $\overline{\text{TXOK}}$ signals when OOS is LOW and assert RESYNEN only after an error threshold has been reached. It is up to the user to make sure enough IDLE words are used to detect errors during system operation. The switch can initiate the initialization process by forcing zeroes on the serial link. If the transceiver receives 4 consecutive words of all zeroes, it will immediately start the initialization process.

1.2 Data Encoding Format

To provide self routing and signalling functions, the transceiver and switch require different data types to differentiate between data words, connection request words or command words. Depending on the mode that the transceiver is in, different data types are recognized at the transceiver parallel interface. These word types are encoded using the RXTYP[1:0] or TXTYP[1:0] bits. At the transceiver to switch serial interface, these data types are encoded in the two overhead bits (B[1:0]). Sections 2.2, 3.2 and 4.2 describe these data types in more detail.

The format for data words and command words the transceiver parallel interfaces and on the serial data lines between the transceiver and switch chip are described in the following sections. The format for the connection request word is described later in the Packet Mode section.

1.2.1 Data Word Format at Transceiver Parallel Interface

Data words contain a 32 bit user defined payload which is sent between the transmitting and receiving port cards as shown below. The RXTYP[1:0] and TXTYP[1:0] data word encoding format for different modes are described in later sections.

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
D D D D 31 30 29 28	D D D D 27 26 25 24	D D D D 23 22 21 20	D D D D 19 18 17 16	D D D D 15 14 13 12	D D D D 11 10 09 08	D D D D 07 06 05 04	D D D D 03 02 01 00
---------- Data Payload ----------							

Where:
D[31:0]32 bit data payload

1.2.2 Data Word Format on the Serial Data Lines

The data word format as seen at the serial output of the transceiver or switch chip is shown below. Two overhead bits are added by the transceiver or switch chip to designate a data word to the receiving switch chip or transceiver. The serial data is transmitted with the MSB first (B1, B0, D31, D30... D00).

33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
B B 1 0	D D D D 31 30 29 28	D D D D 27 26 25 24	D D D D 23 22 21 20	D D D D 19 18 17 16	D D D D 15 14 13 12	D D D D 11 10 09 08	D D D D 07 06 05 04	D D D D 03 02 01 00
	---------- Data Payload ----------							

Where:
B[1:0]If BYPASS=0,01=Flow control channel,
10=Flow control channel,
11=Acknowledge from switch chip or data header to switch chip
If BYPASS = 1, RXTYP[1:0]=B[1:0]=TXTYP[1:0]
D[31:0]32 bit data payload

1.2.3 Command Word Format at Transceiver Parallel Interface

There are several command words that are used for sending information to the switch chip or a receiving port card. The command word format at the transceiver parallel interface is shown below. IDLE words are discussed in the next sections. A delay enable value can also be programmed into the transceiver for Packet Mode using this command word.

31 30 29	28 27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
X X X	C C C C C 04 03 02 01 00	D D D D 15 14 13 12	D D D D 11 10 09 08	D D D D 07 06 05 04	D D D D 03 02 01 00	X X X X	X X X X
	-- Command --	-- Data --					

Where:
C[4:0]Command type:
00XXX=Link Control (00111=IDLE word)
01XX0=Command word for transceiver (01000=set DLYEN/CCKIN value)
10XX0=Command word for switch

11XX0=Command word for receiving port card

D[15:0]Optional data payload:

Default=1010101010101010

IDLE Word from switch=Output(s) this port is connected to;

D[15] is equal to port 0, and D[0] is equal to port 15.

If C[4:0]=01000, D[3:0]=DLYEN/CCKIN value

1.2.4 Command Word Format on the Serial Data Lines

The command word format as seen at the serial output of the transceiver or switch chip is shown below. Two overhead bits are added by the transceiver or switch to designate a command word (00) to the receiving switch chip or transceiver. The serial data is transmitted with the MSB first. In Packet Mode, the IDLE word from the switch always returns the current output connections for the port.

33 32	31 30 29	28 27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
0 0	1 B B 1 0	C C C C C 04 03 02 01 00 -- Command --	D D D D 15 14 13 12	D D D D 11 10 09 08	D D D D 07 06 05 04	D D D D 03 02 01 00 -- Data --	1 0 1 0	1 0 1 0

Where:

B[1:0]00=Undefined (during normal operation) or alignment word

01=Flow control channel,

10=Flow control channel,

11=Acknowledge (from switch chip only) or link initialization reset or cell clock in cell mode

C[4:0]Command type:

00XXX=Link Control (00000=ALIGN word, 00111=IDLE word)

01XX0=Command word for transceiver (01000=set DLYEN/CCKIN value)

10XX0=Command word for switch

11XX0=Command word for receiving port card)

D[15:0]Optional data payload:

Default=1010101010101010

IDLE Word from switch=Output(s) this port is connected to;

D[15] is equal to port 0, and D[0] is equal to port 15.

If C[4:0]=01000, D[3:0]=DLYEN/CCKIN value

1.2.5 IDLE Words

IDLE words are the default word used on the serial channel when none of the other word types are present. In most cases, these words are automatically generated by the transceiver or switch chip. In Packet Mode, IDLE words are inserted between packets and the IDLE word from the switch always returns the current output connections for the port that is receiving the IDLEs. If the user does not have data to send, IDLE words can be loaded into the parallel interface, or the TXEN signal can be set LOW which forces the transceiver to send IDLEs to the switch chip. In cell mode, IDLEs will be transmitted from the switch chip if the Force IDLE bit is set in the switch chip (see the VSC880 data sheet). See sections 2.0 and 3.0 for more details. IDLE words are also used to detect link error conditions. If the transceiver detects and IDLE word, it uses a bit mask to verify the proper bit pattern within the word.

1.3 Loopback Mode

The VSC870 supports two loopback functions at the serial interface. If the LOOPBACK signal is set HIGH, the serial transmit data is looped back to the CRU on the serial receiving side. The transmitted serial data is generated using the CMU clock. This mode can be used to test the high speed circuitry (except for the serial input/output buffers) using the low speed parallel interface. The serial data can also be looped back through the I/O of the switch chip or other connected transceiver if the other device is in FACLPBK mode (see the table below). If FACLPBK is set HIGH, the receive serial data is recovered using the CRU and looped back to the serial output.

1.4 Redundancy

There are two serial output buffers and two serial input buffers on the transceiver. These can be used to connect to redundant switch chips or redundant transceivers. The serial inputs are also connected to a signal detector circuit which is used to determine if there is an average of one transition for every 34 bits of data. If there is, the signal ALIVE remains HIGH. Which ever input is not connected to the CRU is connected to the signal detector. An example system would have the redundant serial output connected to a redundant switch chip. This switch chip has the LPBK bits in the status and control registers set HIGH such that the transceiver output signal (which is looped through the switch input/output buffer) comes back to itself at the redundant serial input buffer (see Application Note 35). If the primary switch chip fails, and the ALIVE signal is HIGH on all transceivers, the redundant switch chip can be activated in its place after it goes through the link initialization process. The signal RXSEL on the transceiver is used to select the redundant input buffer.

1.5 Operating Modes

The following table summarizes the operating modes for the transceiver that have been discussed in the previous sections. The pin LTIME selects the source of the bit clock for the transmit side. LTIME is normally set HIGH. In this case, the received bit clock is use for the transmit bit clock. If LTIME is set LOW, the transceivers CMU is used as the source of the transmit bit clock. This signal must be set LOW to test the transceiver in loopback mode or when used as a master transceiver in Direct Mode (see section 4.0).

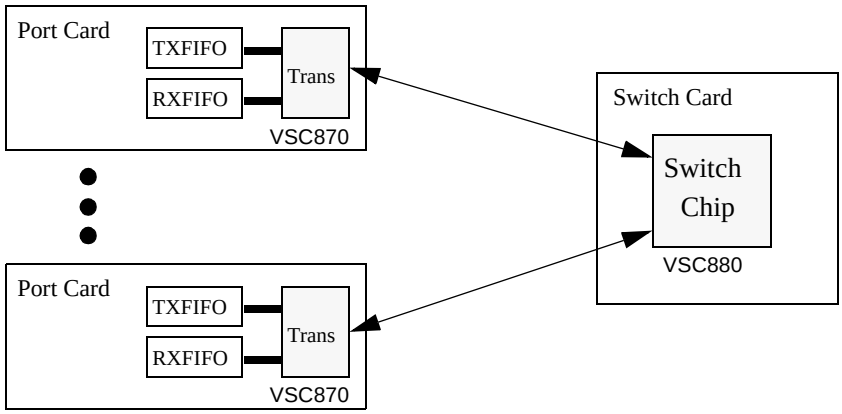
Control Signal Name						*Description of Operation*
LOOP BACK	*LTIME*	*MODE[1]*	*MODE[0]*	*BY PASS*	*CELL SYN*	
0	1	1	1	0	0	Normal Packet Mode operation
0	1	1	1	1	1	Normal Cell Mode operation
0	0	0	1	1	0	Master transceiver in Direct Mode (figure 13)
0	1	0	1	1	0	Slave transceiver in Direct Mode (figure 13)
0	0	0	0	1	0	Master transceiver in Direct Mode (figure 14)
0	1	1	1	1	0	Slave transceiver in Direct Mode (figure 14)
1	0	1	0	1	0	Loopback mode internal to the transceiver
0	1	1	0	1	0	Loopback mode through a VSC880
0	0	1	0	1	0	Loopback mode through an external cable
0	X	0	0	0	1	Mux/Demux Mode - No word alignment

2.0 Packet Mode

2.1 Overview

In Packet Mode the BYPASS signal is set LOW to allow the transceiver to utilize the built-in retransmission, camp-on, virtual output queue and delayed read enable logic. In addition, the signal CELLSYN is held LOW to disable the cell synchronization process. A special command word can be sent through the transceiver to the switch chip requesting connection to one or multiple output ports. Acknowledge (ACK) information will be returned to the transceiver from the switch allowing the port card to start transmitting data (see Application Note 31: Design Guide for a Packet Based Switch with Distributed Control). This special command word, a Connection Request (CRQ) Command, can be put on the front of the data packet to make the packet self routing. In this mode of operation, no controller chip needs to be connected to the switch chip as the switch chip handles all arbitration for connection requests (see the VSC880 data sheet). If the system designer wants to bypass the features described in this section, the signal BYPASS can be set HIGH. The user will then have direct control of the data stream between the transceiver and the switch. A picture of a Packet Mode system is shown below. The minimum packet size in this mode of operation is 4 words or 16 bytes.

Figure 1: Packet Mode System



2.2 Data Encoding Format

The data and command words are described in section 1.0. In this section the Connection Request (CRQ) word format at 4 interfaces (transceiver parallel transmit port, serial line to switch, serial line from switch and transceiver parallel receive port) is described. In this mode the TXTYP[1:0] and RXTYP[1:0] bits are encoded differently than the overhead bits (B[1:0]) to effectively support a variety of features in the Packet Mode. The encoding for these data types are described in the following section.

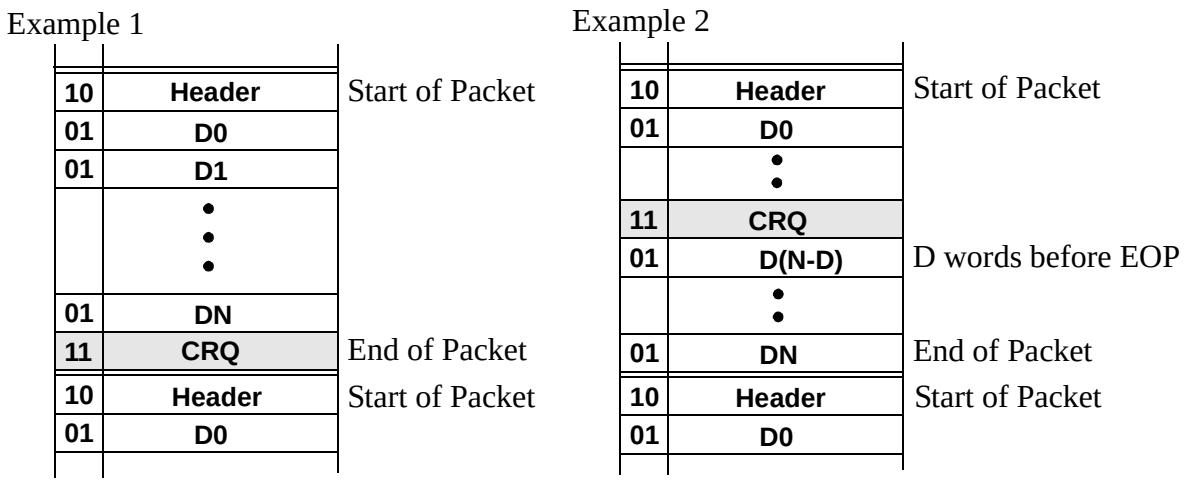
2.2.1 Packet Format

At both the transmit and receive sides, a start of packet is identified using a header word with TXTYP[1:0] and RXTYP[1:0] set to "10". Following this header word are the rest of the data words with TXTYP[1:0] and RXTYP[1:0] set to "01". This is shown in the table below.

TXTYP[1:0] RXTYP[1:0]	*Transmit B[1:0]*	*Receive B[1:0]*	*Word Type*	*SCRAM = 1*	*SCRAM = 0*	*Error Check*
0 0	0 0	0 0	Command Word	No Scramble	No Scramble	IDLE words
0 1	01 or 10	01,10,11	Data Word	Scramble	No Scramble	No
1 0	1 1	0 0	Header Word	No Scramble	No Scramble	No
1 1	0 0	0 0	Connection Request	No Scramble	No Scramble	No

Two general ways of transmitting a data packets are shown in the figure below. In the first example, when the transceiver reads a CRQ word (which signals the start of a new packet) it waits for the ACK signal before transmitting the header word. In the second example, the CRQ word is sent D words before the end of the packet in order to utilize early arbitration and optimize the throughput. If there is no available packet for the next transmission, a null CRQ word and a null header word are used as end of packet. Command words such as IDLEs can be embedded inside the packet. On the receive side, the packets are delineated by the header word at the beginning and a CRQ word at the end. The word sequence loaded into the VSC870 parallel interface is also shown in the figure below. More details can be found in Application Note 31.

Figure 2: Packet Transmission Format



© *VITESSE SEMICONDUCTOR CORPORATION* • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

The IDLE word acts as a null word. The transceivers ignore these words at the transmit side. If there is no valid word at the transmit side, the signal TXEN should be set LOW. When the transceiver is loaded with IDLE words at the parallel transmit side, the transceiver will formulate its own IDLE word and send it through the serial output. At the receiving side, the transceiver sets the RXWA signal LOW if it receives an IDLE word from the serial line. IDLE words contain switch connection information that may be used by external logic. This information is also used for automatic packet retransmission as discussed in section 2.3.6. The connection information is in the same format as shown in section 2.2.4 below. The next CRQ word will also be forwarded through the switch to the current receiving port card. These can be ignored.

2.2.2 Header Word Format at the Transceiver Parallel Interface

The header word format at the transceiver parallel interface is shown below. A maximum of 20 bits can be used to send data to the receiving port card. These bits can contain the first bytes of the data packet or other information. For a NULL header word, these bits are all X's.

31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
X X X X	X X X X	D D D D 19 18 17 16	D D D D 15 14 13 12	D D D D 11 10 09 08	D D D D 07 06 05 04	D D D D 03 02 01 00	X X X X
		---------- Data Payload ----------					

Where:
D[19:0]20 bit data payload

2.2.3 Header word Format on the Serial Data Lines

The header word format as seen at the serial output of the transceiver or switch chip is shown below. Two overhead bits are added to designate a header word to the receiving chip. The serial data is transmitted with the MSB first.

33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
A A 1 0	0 B B 1 1 0	0 1 1 0	D D D D 19 18 17 16	D D D D 15 14 13 12	D D D D 11 10 09 08	D D D D 07 06 05 04	D D D D 03 02 01 00	1 0 1 0
			---------- Data Payload ----------					

Where:
A[1:0]11=to switch chip, 00=from switch chip
B[1:0]00=Undefined,
01=Flow control channel,
10=Flow control channel,
11=Acknowledge
D[19:0]20 bit data payload

2.2.4 CRQ Format at the Transceiver TXIN[31:0] Interface

The connection request command word format at the TXIN[31:0] interface is shown below. The signals CT[2:0] and MD[1:0] are used by the transceiver to control modes of operation that are described later in this section. For a NULL CRQ word, set all the connection bits LOW.

31 30 29	28 27 26	25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
X X X	C C C T T T 2 1 0	M M D D 1 0	C C C C 00 01 02 03	C C C C 04 05 06 07	C C C C 08 09 10 11	C C C C 12 13 14 15	D D D D 03 02 01 00	X X X X
			------ Connection Bits ------				-- Data--	

Where:
CT[2:0]Control bits
MD[1:0] Mode; 00=Camp-on with Priority Mode, CT[2:0]=camp-on frequency
01=Camp-on with Recast Mode, CT[2:0]=number of CRQ commands to send
10=Multi Queue Mode, CT[2:0]=camp-on frequency
C[0:15]] Connection request bit map. Set bit high for each output requested.
C[0] is for port 0 and C[15] is for port 15.
D[3:0] User defined data sent by transmitting port card

2.2.5 CRQ Word Format on the Serial Data Lines to the Switch

The CRQ command word format as seen at the output of the transceiver is shown below. Two overhead bits are added by the transceiver to designate a CRQ word to the receiving switch chip. The signals AOA and BRK are used to control modes of operation in the switch chip which are discussed in the VSC880 data sheet. The serial data is transmitted with the MSB first.

33 32	31 30 29 28 27	26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
0 0	0 B B 1 0 1 0	A A B R O R B A K	C C C C 00 01 02 03	C C C C 04 05 06 07	C C C C 08 09 10 11	C C C C 12 13 14 15	D D D D 03 02 01 00	1 0 1 0
			------ Connection Bits ------				--Data--	

Where:
B[1:0]00=Undefined,
01=Flow control channel,
10=Flow control channel,
11=Undefined
ARB1=Multi Queue arbitration, 0=Normal operation
AOA1=Acknowledge-On-All connections granted, 0=Acknowledge-On-Any connections granted
BRK 1=Break previous connection, 0=Do not break previous connection
C[0:15] Connection request bit map. Set bit high for each output requested, C[0] for output port 0 etc
D[3:0] User defined data sent by transmitting port card

2.2.6 CRQ Word Format on the Serial Data Lines from the Switch

The CRQ command word format as seen at the output of the switch chip is shown below. Two overhead bits are added by the switch chip to designate a command word (00) to the transceiver. This command word contains the current active connections for the transmitting port card. The serial data is transmitted with the MSB first.

33 32	31 30 29 28 27 26 25	24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
0 0	0 B B 1 0 1 0 1 0	B R K	M M M M 00 01 02 03	M M M M 04 05 06 07	M M M M 08 09 10 11	M M M M 12 13 14 15	D D D D 03 02 01 00	1 0 1 0
			------ Active Connections ------				--Data--	

Where:
B[1:0]00=Undefined,
01=Flow control channel,
10=Flow control channel,
11=Acknowledge
BRK1=This is the CRQ word for the next packet, 0=End of packet
M[0:15]Current outputs the transmit side is connected to
D[3:0] User defined data sent by transmitting port card

2.2.7 CRQ Word Format at the Transceiver RXOUT[31:0] Interface

This is the CRQ command word format on the parallel interface RXOUT[31:0] of the transceiver. The two overhead bits are removed. This word arrives at the transceiver D words before the end of packet and also at the end of packet. The BRK bit is used to designate the end of packet (see Application Note 31). The data bits D[3:0] can be used by the transmitting port card to send information to the receiving port card such as port ID number.

31 30 29 28	27 26 25	24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
0 0 0 0	0 0 0	B R K	M M M M 00 01 02 03	M M M M 04 05 06 07	M M M M 08 09 10 11	M M M M 12 13 14 15	D D D D 03 02 01 00	0 0 0 0
			------ Active Connections ------				--Data--	

Where:
BRK1=This is the CRQ word for the next packet, 0=End of packet
M[0:15]Current outputs the transmit side is connected to
D[3:0] User defined data sent by transmitting port card

2.3 Transmitter Operation

In Packet Mode, the transmitter is loaded with a connection request (CRQ) word followed by data words at the parallel interface. The operation of the transceiver is such that a single CRQ word loaded into TXIN[31:0] may cause the transceiver to send multiple CRQ words to the switch chip. When this happens, data may be blocked for several word clocks until the switch grants the request. In order to improve bandwidth utilization, a system wide mode of operation (called ‘early arbitration’) can be used where the switch matrix reconfiguration time is delayed D word clocks from the time arbitration results are determined. This allows the user logic to receive arbitration results just as the first word of the next data packet is ready for transmission, thus improving bandwidth utilization.

The CRQ word has several control bits that are shown in the definitions above. Five of these bits control the operation of the transceiver. The mode bits MD[1:0] determine the transceiver operating mode for a particular connection request. The control bits CT[2:0] determine priority levels or time-out values depending on the mode of operation. A summary of these operating modes is shown below. All of these modes will operate with early arbitration as described in the next sections.

© VITESSE SEMICONDUCTOR CORPORATION • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

MD[1:0]	CRQ Mode	CT[2:0] Definition
0 0	Camp-on with Priority Mode	Number of IDLE words between each CRQ word
0 1	Multicast with Recast Mode	Number of CRQ words to send in a row
1 0	Multi Queue Mode	Number of IDLE words between each CRQ word

Camp-on with Priority means the transceiver sends a repeated sequence of connection request words to the switch at a variable frequency until the request is granted. Multicast with Recast means the transceiver sends a fixed number of connection request words to the switch. If some but not all outputs are granted, the packet is sent. After the packet is transmitted successfully, the process is repeated for the rest of the ungranted outputs. In this mode, the FIFO or memory system is required to provide retransmit capability. Multi Queue mode allows multiple unicast requests to be sent to the switch in the same CRQ word. The switch returns data to the transceiver describing which connection was granted. This mode also supports priority camp-on as described above. In all of these modes, to release its connection, the port sends a new CRQ to the switch. If the CRQ does not have any output port bit set, the switch interprets this as a connection release command. If a destination is released, the switch keeps sending IDLE words to the destination port until a new connection is made.

2.3.1 ABORT Signal

If the CRQ cannot be granted by the switch (for example, a time out expires in the user logic), the user can set the ABORT signal HIGH to abort the transaction. Upon detecting that the ABORT signal is HIGH, the transceiver sends out one more CRQ command with the connection request bit map cleared. This will force the switch to release any connections it has accumulated and all data words up to the next CRQ at the user interface will be read and ignored. The ABORT signal has to be held HIGH longer than the round trip delay between the transceiver and switch chip (> 9 clock cycles). This guarantees that any ACK generated during that time will be discarded. If ABORT is held HIGH for only a single cycle, then it can not be followed by another CRQ within 9 cycles. If the ABORT is set HIGH in the middle of a packet, the transceiver will also send a CRQ to the switch to break the current connections.

2.3.2 Early Arbitration

In order to optimize throughput, early arbitration can be performed by sending the CRQ words to the switch D words before the end of the current packet. When arbitration results are known, the arbiter reserves the switch output for the granted input until the current data transmission is completed for that output. The end of the current transmission is identified by the header word of the next packet. When the switch receives the header word, the switch matrix will be reconfigured for the outputs that were reserved from the last arbitration. The maximum value for D is based on the round-trip delay from the time the port submits a CRQ until an ACK is received and the FIFO is ready to send a data word. In a typical system, the round trip delay is 9 cycles plus the FIFO response time. If the transmission line delay on the serial data line is significant, this time will increase. The value of D can be set higher than the round trip delay only if the minimum delay enable value (see section 2.3.3) is equal to the difference between D and the round trip delay (i.e. maximum D = 9 + delay enable value). For example, if the round trip delay is 9 and D is set to 10, the minimum delay enable value is 2. The number D is a system wide value that must be used by all port

cards. During Early Arbitration, the early CRQ is camped on in the switch and is arbitrated every cycle until another IDLE or CRQ word arrives. This means it is at the highest priority level regardless of CT counter. If the connection has not been granted at this point, CRQ sequences begin based on the MD and CT bits in the CRQ word as described below.

2.3.3 Delay Enable Signal

If the signal DLYEN/CCKIN is set HIGH, a pre-programmed delay will occur between the time an ACK is received from the switch chip, and the signal REN (read enable) goes HIGH to start reading data at the parallel interface. Users can set this number to any value between 0 & 15 by using the 4 bits described in the command word in section 1.2.3. The default value is 6 word clock cycles. If the signal DLYEN/CCKIN is set LOW, the value is 0 no matter what value was programmed in. If the input buffer system is a single queue FIFO, after receiving ACK, the FIFO can send data out at once. In this case, the DLYEN/CCKIN signal can be set LOW to force REN HIGH right after receiving ACK signal. If the input buffer system is designed with multiple data queues, users can use the Multi Queue mode to improve throughput. In this mode, after the ACK signal is sent back to the FIFO, the transceiver takes 4 more cycles to send 4 bits of information containing the granted queue ID. The FIFO might take some extra time to process this information before it can send out data to the new destination. To account for this extra latency, The DLYEN/CCKIN signal can be set HIGH to force the transceiver to wait for 6 more cycles after receiving ACK before it can sends the data for the next packet. This 6 cycles of delay is set by default in the transceiver after reset. If the default value of 6 cycles is used, the value for early arbitration should be set to 9+6=14.

2.3.4 Out of Synch Conditions

There are two out of synch conditions that can occur during packet mode operation. The serial link from the transmitting port card can go out of synch, or the serial link to the receiving port card can go out of synch. If the serial link on the transmitting side goes out of synch, the switch will send alignment patterns to the transceiver, and the transmitting port card is signaled on the OOS pin of the transceiver. When this happens, there is a chance that the receiving port card will receive only a partial packet. In this case, the CRQ word with BRK set HIGH will not be received; therefore, the receiving port card knows it did not receive the end of packet properly. If the serial link on the receiving side goes out of synch, the receiving transceiver will set the $\overline{\text{RXOK}}$ and $\overline{\text{TXOK}}$ pins high, and the OOS pin will also go high to indicate that the transceiver is in the link initialization process. The transmitting port card is not signaled for this condition through the switch chip. The user must make this condition known to the transmitting port card through some other means. If one of the output ports on the switch chip is in the out of synch state, any request for connection to this output will always be granted. In addition, no flow control back pressure will be applied from this output. This is to make sure multicast connections will not get permanently locked up, but packets could be lost in this case.

2.3.5 Unicast / Multicast Camp-on with Priority Mode (MD[1:0] = 00)

In this mode, after the transceiver is loaded with a single CRQ at the parallel interface, it will send one CRQ word to the switch and wait for the ACK. During early arbitration, the switch will store this CRQ and arbitrate until all the outputs requested are granted. During this time, the transceiver can send more data words for the end of the last packet (the number of data words sent must be less than or equal to D). The value for D can also be set to zero. If the transceiver detects the header word for the next packet at the parallel interface before receiving an ACK (see figure

2), it stops reading from the parallel interface by setting REN LOW, sets RTM/TCLK HIGH and starts sending a repeated sequence of CRQ words to the switch which are arbitrated only on the cycle that they arrive. During this operation, the CRQ words are not stored at the switch. If all connections are granted, the transceiver will receive an ACK from the switch. If DLYEN/CCKIN is LOW, it sets the REN signal HIGH when it receives the ACK, and sends the header word and data to the switch. If DLYEN/CCKIN is HIGH, it waits for N more cycles before it sets REN HIGH and then sends header word and data to the switch.

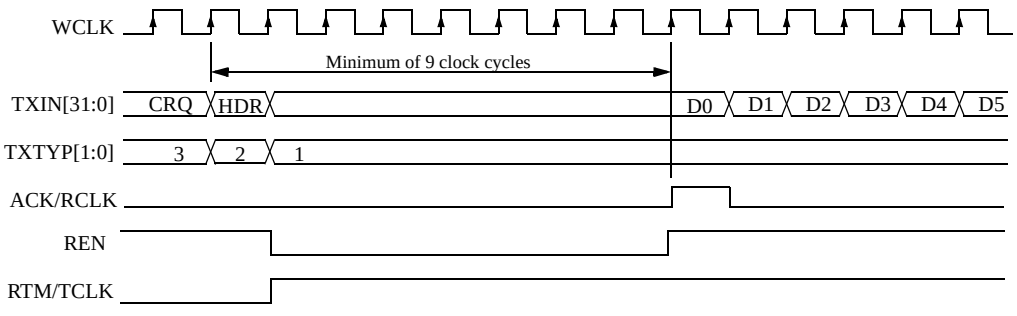
During the repeated sequence of CRQs described above, different priorities for connections can be established by the number of the IDLE words sent between each CRQ words (determined by the CT[2:0]). The number of IDLEs after each CRQ word can range from 0-7 as shown in the table below. Generally, the more often a CRQ is received by the switch, the higher the probability that this connection will be granted.

CT[2:0]	*Number of IDLE Words*
0 0 0	0
0 0 1	1
0 1 0	2
0 1 1	3

CT[2:0]	*Number of IDLE Words*
1 0 0	4
1 0 1	5
1 1 0	6
1 1 1	7

The functional timing diagram for camp-on mode with DLYEN/CCKIN set LOW is shown in figure 3. There are a minimum of 9 word clock cycles between loading the CRQ into the transceiver and the signal REN going HIGH (to start sending the data packet D0, D1, D2 etc.). This time will be longer if the requested output is busy or the port card is located further from the switch card. For multicast, the switch will reserve any available outputs and accumulate them as more CRQ commands are processed. This continues until all connections are reserved. At this point an ACK signal is sent back to the transceiver.

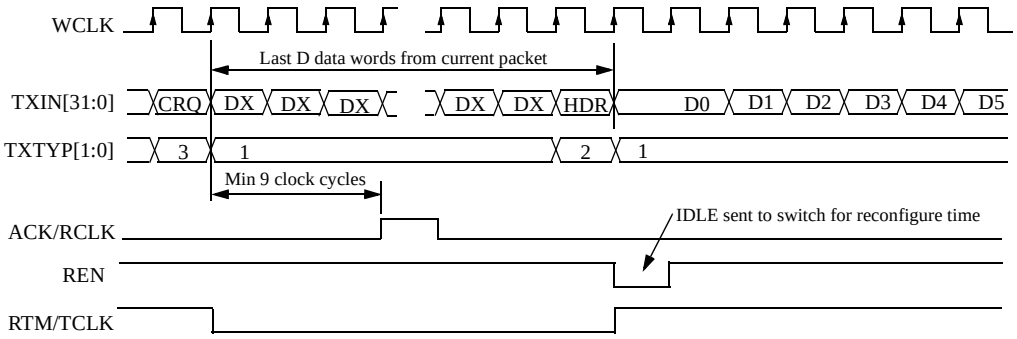
Figure 3: Camp-on with Priority Transmitter Functional Timing (no early arbitration)



© *VITESSE SEMICONDUCTOR CORPORATION* • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

If early arbitration is used, the first CRQ word is sent to the switch D cycles before the end of the current packet. If the ACK is not received before the end of the current packet, the transceiver then operates the same as shown in the figure above. If the ACK is received before the end of the current packet, the transceiver will set the signal REN low for one cycle at the end of the current packet after the DLYEN/CCKIN counter has expired. The transceiver then sends an IDLE to the switch to give it time to reconfigure before the next data packet arrives. The functional timing diagrams are shown below.

Figure 4: Camp-on with Priority Transmitter Functional Timing (with early arbitration)



In the first CRQ the transceiver sends to the switch, the BRK bit is set. In subsequent CRQ words, this bit is cleared. The AOA bit is always set in this mode. The user logic can monitor the RTM/TCLK signal, which goes HIGH after the transceiver receives a new header word, and set LOW when the transceiver sees a new CRQ. In the case of multicast-with-recast, the RTM/TCLK signal will not go low until it sees a new CRQ during the last recast. If the RTM/TCLK signal stays HIGH too long, the user logic can abort the CRQ by setting ABORT HIGH.

Because these are camp-on requests, when several multicast CRQs of this type are received by the switch, there is a potential for a lock-up condition. The chances for lock-up can be reduced by minimizing the number of multicast requests. Lock-up can be broken by aborting the CRQ after a time-out period determined by the RTM/TCLK signal. If each port card uses a random time-out period before aborting, there is a higher probability that one of the multicast requests will be granted. A more efficient multicast method is shown in the next section.

2.3.6 Multicast with Recast Mode (MD[1:0] = 01)

In this mode, after the transceiver is loaded with a single CRQ at the parallel interface, it will send one CRQ word to the switch and wait for the ACK. During early arbitration, the switch will store this CRQ and arbitrate until all the outputs requested are granted. During this time it can send a maximum of D (D can be greater than or equal to zero and is described in section 1.2.3) more data words until the packet header. If the transceiver detects the header word for the next packet at the parallel interface (see figure 2), it stops reading from the parallel interface by setting REN LOW. It also sets RTM/TCLK HIGH and starts sending more CRQ words to the switch depending on the value of CT[2:0]. During this camp-on period, the switch chip will accumulate the available outputs that were requested. If all connections are granted at some point during this period, the transceiver will receive an ACK from the switch. If DLYEN/CCKIN is LOW, at this time it sets the REN signal HIGH and sends the header word and data to the switch

as shown in Figure 3. If DLYEN/CCKIN is HIGH, it waits for N more cycles before it sets REN HIGH. If the counter set by the CT[2:0] bits has expired and the transceiver has not received the ACK signal, it sends out a CRQ word with AOA bit set LOW so that an ACK is returned if any output is granted. The transceiver keeps sending this CRQ word until it receives the ACK signal. When the ACK is received, the transceiver sets the REN signal HIGH and sends the header word and data to the switch for any output that was granted. This occurs right after receiving ACK if DLYEN/CCKIN is LOW or N cycles later if DLYEN/CCKIN is HIGH. The table below shows the number of CRQ words sent for each value of CT[2:0].

CT[2:0]	*Number of CRQ Words*
0 0 0	1
0 0 1	8
0 1 0	16
0 1 1	32

CT[2:0]	*Number of CRQ Words*
1 0 0	64
1 0 1	128
1 1 0	256
1 1 1	512

Recast Operation

If an ACK is not received before the CT[2:0] counter expires, the transceiver converts to recast mode. In this mode, the memory system or FIFO should support retransmit capability. When the transceiver first reads the Header word from the user interface, it sets the signal RTM/TCLK HIGH (Figure 5). This signal can be used to mark the FIFO location of the first data word in this packet and not allow the user logic to overwrite this data packet in the FIFO (see Application Note 31). The signal RTM/TCLK goes LOW when data has been sent to all requested destinations or if ABORT signal is asserted HIGH. If during a multicast, the CT[2:0] counter expires and some connections were not granted, an IDLE word or CRQ word will be returned to the transceiver from the switch chip describing the current connection status of the port. Upon detecting the CRQ word for the next packet at the parallel transmit interface, the transceiver will use this information from the switch to automatically form a new CRQ word requesting the outputs that were not granted. This CRQ word will replace the CRQ word at the parallel interface and is sent to the switch followed by remaining data if early arbitration is used. The process is repeated as if this is a new multicast CRQ for the current Packet. Also in early arbitration mode, the CRQ for the next packet remains in the external FIFO or memory system, and it is used after the last recast for the current packet. The ACK will toggle every time the transceiver performs recast.

When the transceiver reads the header of the next packet, the RFM signal is toggled to set the FIFO pointer back to the earlier location marked by RTM/TCLK in order to recast this packet to the new locations (Figure 6). Note that the RTM/TCLK signal is set after the transceiver loads the Header word for the current packet. Therefor the header word is lost and not retransmitted. During recast, this word will not be sent to the new locations if RTM/TCLK is used to mark the retransmit location. Users can externally adjust the RTM/TCLK to account for this latency or use an extra header word which will be lost during recast (see Application Note 31).

If the end of packet is reached before the connection information is returned from the switch, IDLE words will be sent to the switch while waiting for this response word. The retransmission process will continue until the data has been sent to all the requested destinations or ABORT is set HIGH. If ABORT is set HIGH (transmission is aborted), all of the following data words will not be retransmitted and will be ignored. The transceiver will then look for the next CRQ word at the parallel interface.

Figure 5: Multicast Recast Functional Timing (Beginning of Multicast)

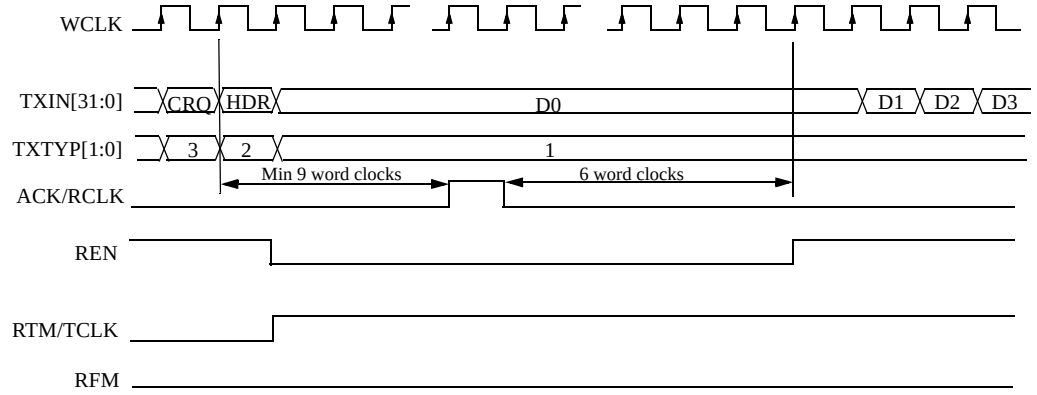
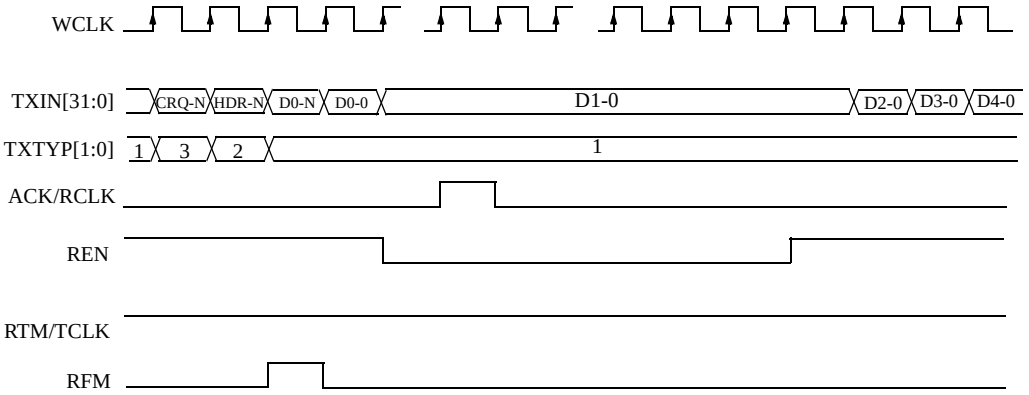


Figure 6: Multicast Recast Functional Timing (At the End of Packet then Recast)



NOTE: CRQ-N, HDR-N, D0-N: CRQ, header and first data word of the next packet; these bytes are ignored by the transceiver during recast.
D0-0, D1-0, D2-0...: Data words of the recasted packet.

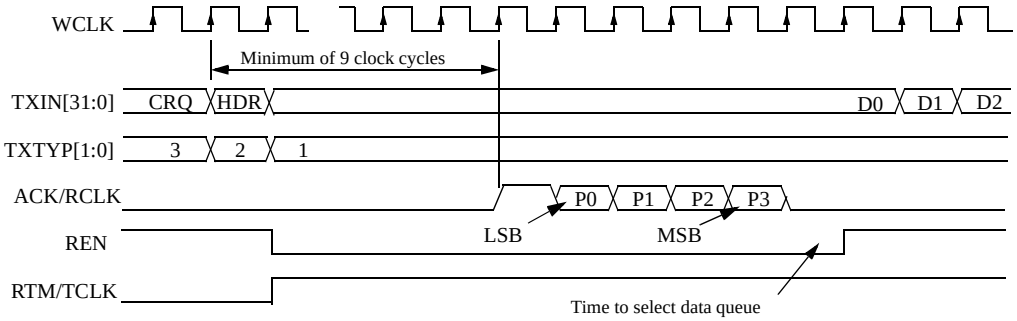
2.3.7 Unicast Multi Queue Mode (MD[1:0] = 10)

Muti Queue mode assumes there are several unicast data queues on each port card such as virtual output queues or priority queues, and allows the port card to make multiple connection requests at the same time. The switch chip performs two levels of arbitration in two word clock cycles. The first level determines which of the requested outputs are available and holds these outputs. The second level chooses one winner from the available outputs then releases the rest. Because outputs can be blocked during the first level of arbitration, all Muti Queue CRQ commands are held at the switch chip and continue to request outputs until one is granted. As in section 2.3.5, if an ACK is not received before a header word is detected at the parallel interface, a repeated sequence of CRQs are sent to the switch chip until an output is granted. This sequence depends on the value of CT[2:0]. The port number of the granted output (P[3:0]) is returned to the port card following the ACK pulse on the ACK/RCLK output. The functional timing diagram for this mode is shown in Figure 7.

Similar to the Unicast/Multicast Camp-on request, in this mode, after the CRQ word is loaded in the transceiver parallel interface, it will transmit the CRQ word to the switch and wait for the ACK signal to be returned. During this time, the user logic should send a maximum of D data words from the parallel interface to the switch. If the transceiver detects the header word for the next packet at the parallel interface, it stops reading from the FIFO, sets RTM/TCLK HIGH and starts sending a sequence of CRQ words to the switch.

If user wants to operate in a mode where the CRQ is modified after the early CRQ is submitted to the transceiver, then the header word should not be loaded into the parallel interface until an ACK is received. After the last data word of the current packet, a new CRQ can be loaded into the parallel interface of the transceiver. This new CRQ replaces the current one and is sent to the switch. Since the header word is not seen at the parallel interface, the repeated sequence of CRQ words is not automatically sent to the switch. Priority can instead be supported by sending higher priority queue CRQs first and more often then lower priority queue CRQs (see Application Note 31). When ACK and P[3:0] bits are received, the header word and then data words can then be sent to the transceiver as before.

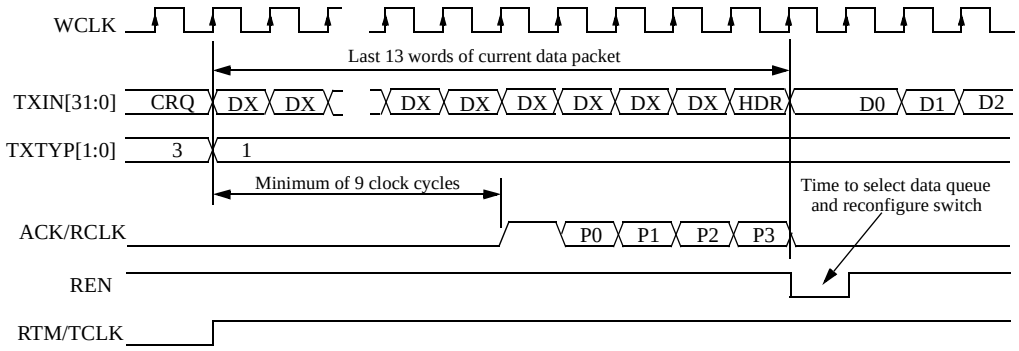
Figure 7: Multi Queue Transmitter Functional Timing (no early arbitration)



When using early arbitration, the CRQ word is sent to the switch chip D cycles before the end of the current data packet. If the P[3:0] bits are returned with-in time D, very high bandwidth utilization of the switch can be achieved as shown in the Figure 8. If the signal RTM/TCLK remains high for too long, the current CRQ can be cancelled by setting the ABORT signal HIGH. At the switch, the current CRQ will continue to requested a connection until it is granted or a new CRQ command arrives (this can also be a NULL CRQ to cancel the current request).

After the transceiver receives ACK signal, if DLYEN/CCKIN is LOW, it immediately sets the REN signal HIGH and sends the header word and data to the switch. If DLYEN/CCKIN is HIGH, it waits for N more cycles before it sets REN HIGH and sends the header word and data to the switch. During this time, the transceiver sends 4 response bits (P[3:0]) to the queue selection logic and waits for the selection to take place before sending data to the new destination. The default value for N is 6 which allows time to receive the P[3:0] bits plus queue processing.

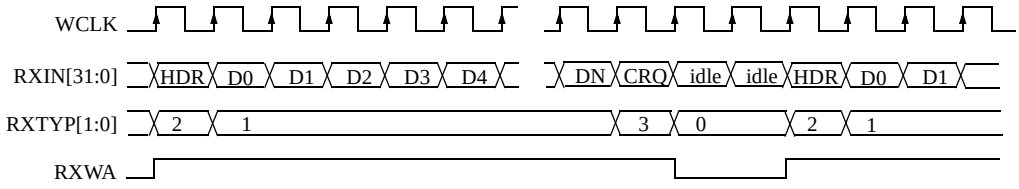
Figure 8: Multi Queue Transmitter Functional Timing (with early arbitration)



2.4 Receiver Operation

In Packet Mode, the receiver examines incoming words and generates the data type signals accordingly. Refer to section 2.2 “Data Encoding Format” for the coding of these signals. If the receive word is an IDLE word, the RXWA signal is set LOW so the FIFO can use this signal to filter out these null data words. If the receiver detects an ACK for the connection request on the transmit side, the ACK/RCLK signal is asserted for one word clock. The RXOUT data bus and RXTYP outputs can be tristated by asserting RXEN. CRQ words, header words, IDLE words and data words are sent to the receiving port card. A functional timing diagram for a typical receiver operation is shown in the following figure. See Application Note 31 for more detailed information.

Figure 9: Receive Channel Functional Timing



2.5 Flow Control Channel

The transceiver can support a back pressure mechanism by providing a flow control channel. This channel supports two logic states that are sent from the receiving port card back to the transmitting port card. The flow control channel is time shared with the signaling between the switch chip and the transceiver for acknowledgment and response bits for Multi Queue connection requests. Therefore, it can only guarantee to pass the state information from the RTR pin at the receiving port card through the switch and to the REN pin at the transmitting port card. The REN pin is also shared between the flow control channel and the transceiver’s connection request retransmission logic. To apply backpressure to the transmitting port card, the RTR signal should be set LOW. An application for this flow control channel is to prevent the FIFO on the receiving side from overflowing. In this case, the

$\overline{\text{ALMOST\_FULL}}$ signal from the receiving FIFO is connected to the RTR pin, and the REN signal is connected to the transmitting FIFO READ_ENABLE signal. In this way, when the receive FIFO is almost full, the transmit FIFO will be disabled from sending data. For multicast, all incoming flow control data is ORed to the transmitting port.

The latency from the time the backpressure is applied at the RTR pin until the REN output at the transmitting port card is asserted is 9 clock cycles. This number can be 5 cycles longer if the flow control channel is temporarily interrupted by the ACK or Multi Queue response bits. When using early arbitration, during the time between the early CRQ and the header, the transceiver ignores the flow control bits. This time is D word clock cycles. The maximum latency is therefore D+14 cycles not including the serial transmission line delays. This means that the receive FIFO must signal an almost full condition at least D+14 words before the full condition is reached. This can be larger if the transceivers are more than 16 nS away from the switch chip.

Back pressure is not supported in transceiver loopback mode.

2.6 Packet Mode with BYPASS set HIGH

When the signal BYPASS is HIGH, most of the logic functions described in this section are disabled. In this mode, the transceiver acts as a 34:1 MUX using TXTYP[1:0] as the two MSBs, and a 1:34 DEMUX using RXTYP[1:0] as the two MSBs. The data presented at the parallel interface will get serialized on the transmit side without any modification to the overhead bits, and the reverse is true for the receive side. In this mode, it is up to the user to make sure the data transmitting from the transceiver conforms to the format of the 34-bit command words that are recognizable by the VSC880. The format of the 34-bit command words to and from the switch chip can be found in the VSC880 data sheet. This mode allows the user to define logic to implement specialized packet mode functions that are not implemented in the transceiver logic. See section 4.0 for more information.

3.0 Cell Mode

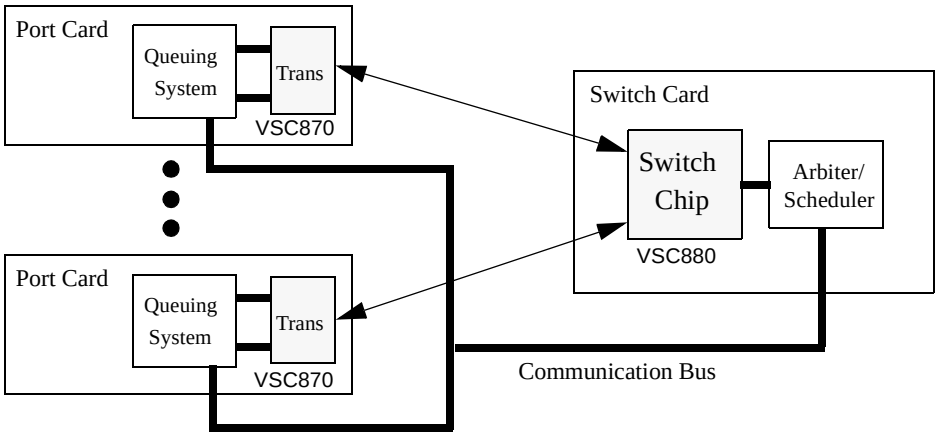
3.1 Overview

In Cell Mode, a more sophisticated arbitration scheme can be supported by using the VSC870 and the VSC880 in conjunction with a user defined queuing logic on the port cards and a scheduling device on the switch card. To activate this mode, the signal BYPASS is set HIGH and the signal CELLSYN is set HIGH. In this mode, only fixed length data packets (cells) can be supported. The central scheduling chip can control the switch using the parallel configuration interface of the switch chip. Messages containing port card queue information are sent to the scheduling chip using an out-of-band control bus. The scheduler performs arbitration and routing based on these messages. Results of the arbitration and flow control are then sent back as messages to the port cards using the out-of-band control bus (see the VSC880 data sheet for more information). Multiple transceivers and switch chips can be used in parallel to achieve higher bandwidth (see Application Note 32: Design Guide for a Cell Based Switch with Central Control).

If multiple transceivers are used on a port card, RTR should be set LOW. In this case, the switch and the transceiver provide a cell synchronous switching fabric for data transfer between port cards and the scheduler chip. Transaction between ports, switch and scheduler are synchronized to a master cell clock. This cell clock, which is also used by the scheduler chip, is connected to the switch chip or to multiple switch chips. The switch chip distributes the cell clock to all connected transceivers during link initialization. The transceivers at the port cards adjust their transmit cell clocks so that all transceivers send the first word of a cell at such time that it arrives at the switch chip aligned to the switch chip cell clock. On the receiving side, all transceivers adjust their receiving pipeline in order to match the delay from their transmitting cell clock to their receiving cell clock by a predetermined number of word clocks. In this way, parallel transceivers can align receiving data to a common cell clock boundary. The word clock delay number depends on the distance from the transceivers to the switch and can be adjusted by using command words as described in 1.2.3. In this mode, the BYPASS signal and CELLSYN signal in the transceiver and the CMODE signal on the switch chip must be set HIGH. By setting the BYPASS signal HIGH, all logic in the transceiver used for the self-routing capability in Packet Mode is disabled. A picture of a cell based system is shown below.

If a single transceiver is used on a port card, set RTR HIGH. In this case, the master cell clock sent from the switch chip to the transceivers is embedded in the serial data. This cell clock is recovered by the transceiver during initialization. The transmit cell clock is generated from this recovered cell clock and phase shifted so that the transmitted cell boundary is aligned with the cell clock at the switch.This recovered cell clock can be used to clock other slave transceivers as in the case RTR=LOW. In this case, the transceiver does not perform pipeline stage adjustment as in the case of RTR=LOW.

Figure 10: Cell Based System



3.2 Data Encoding Format

The data word and command word format is described in section 1.0. These word formats are similar for both the transceivers at the port cards and the transceivers at the controller chip. The BYPASS signal is set HIGH so the RXTYP[1:0] and TXTYP[1:0] are the direct representation of the overhead bits (B[1:0]) in the serial channels. For data words, the user can use these bits for signaling to the receiving port card. Information such as start of frame and end of frame can be passed through the switch in this manner. At the serial interface, the data words must be scrambled to increase the signal edge transition density by setting the SCRAM input HIGH. The scrambling pattern is reset at cell clock. The transceiver checks the bit pattern on IDLE words to detect a link error condition. The encoding for these data types is described in the following table.

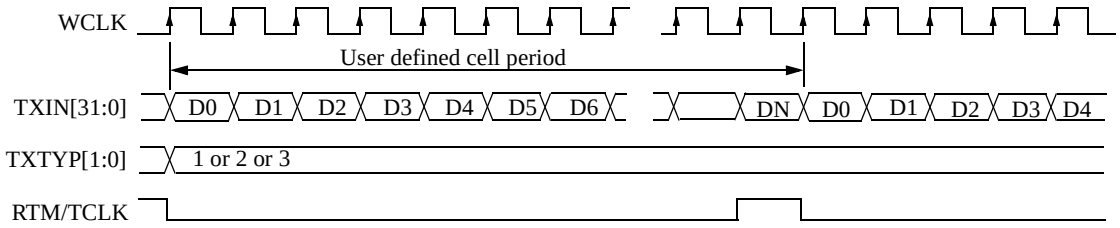
TXTYP[1:0] RXTYP[1:0]	*B[1:0]*	*Datatypes*	*SCRAM = 1*	*SCRAM = 0*	*Error Check*
0 0	0 0	Command Word	No Scramble	No Scramble	IDLE word
0 1	0 1	Data Word	Scramble	No Scramble	No
1 0	1 0	Data Word	Scramble	No Scramble	No
1 1	1 1	Data Word	Scramble	No Scramble	No

3.3 Transmitter Operation

When BYPASS is set HIGH, all of the retransmit and self-routing functions in Packet Mode are disabled. The CELLSYN input is set HIGH to allow the cell synchronization process. All words, either data words or command

words, are passed through the switch matrix. In this case, command words such as IDLEs must be used periodically for checking the link integrity. At the last word of a cell clock period, if the user sends an IDLE word, bits B[1:0] of the IDLE word are set to '11' to embed the cell clock information. The switch will flag a cell sync error if this IDLE word does not contain a cell clock. The transmitter can force an IDLE word at the end of any given cell period by setting the signal TXEN LOW.

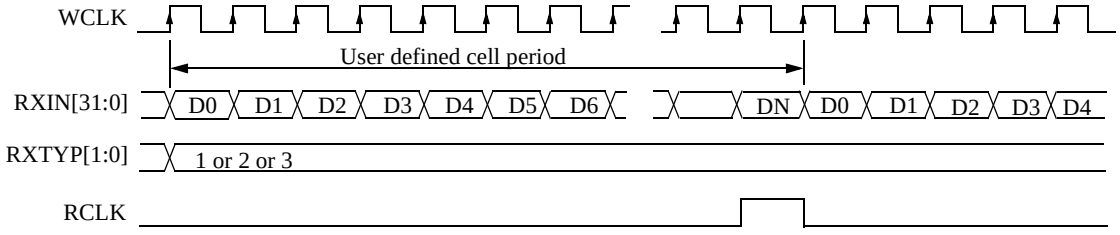
Figure 11: Cell Mode Transmitter Functional Timing at Port Card



3.4 Receiver Operation

At the receiving side, the transceiver examines incoming words and overhead bits. Figure 12 shows the receiver timing diagram. If the received words are data, the overhead bits RXTYP[1:0] will be set to 01, 10 or 11. If the received word is a command word, RXTYP[1:0] will be set to 00. If the received word is an IDLE word, the signal RXWA will also go LOW. If the transceiver receives an IDLE word during the last word of the cell clock period without B[1:0] = 11, a cell sync error condition will be flagged, and the signal $\overline{\text{TXOK}}$ will pulse HIGH.

Figure 12: Cell Mode Receiver Functional Timing at Port Card



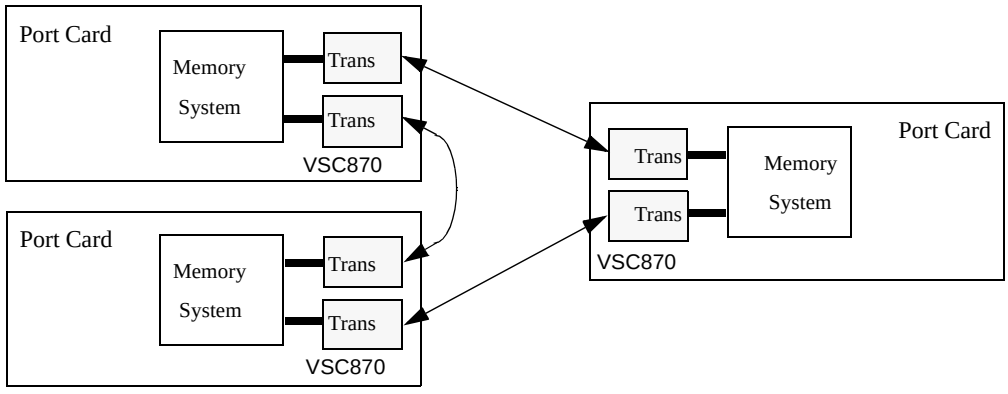
© ***VITESSE*** *SEMICONDUCTOR CORPORATION* • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

4.0 Direct Mode

4.1 Overview

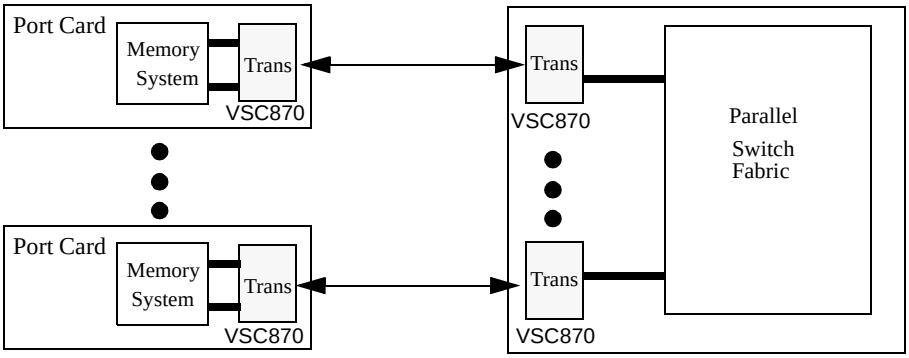
The transceivers can directly connect to each other without a switch chip to form a simple port to port link. In this mode, the signal MODE[1] is set LOW and MODE[0] is set HIGH so that the CMU is selected as the transmit clock and the transceiver word aligns only on the receiving side. The signal LTIME must be set low so the transmitter will use the CMU as the source of the bit clock. The signal BYPASS should also be set HIGH in Direct Mode to disable the retransmit and self-routing features used in Packet Mode. The signal CELLSYN is set LOW to disable the cell synchronization feature. In this configuration, the transceivers will bit and word synchronize to each other. Section 1.5 summarizes these configurations. Also, only data words and command words are used (data word and command word formats are shown in section 1.2). An example of a three port card system with no switch chip is shown below. See Application Note 33 for more information.

Figure 13: Switch System using VSC870 Transceiver Only



The transceiver can also be used as a high speed backplane interconnect link. The ability of the transceiver to perform word and cell synchronization on both transmit and receive sides to a master clock source can help provide a synchronous system up to the word or cell level. In this mode, the signal BYPASS should be set HIGH to disable retransmit and self-routing features used in Packet Mode. The signal CELLSYN is set LOW to disable the cell synchronization feature. In this configuration, the MODE[1:0] signals for transceivers on the switch card are set LOW to allow these transceivers to be aligned to a common word boundary and act as the master clock source. The MODE[1:0] signals for transceivers on the port cards are set HIGH to allow these transceivers to be word aligned at both the transmit and receive sides to the word boundary set by transceivers on the switch card. Multiple transceivers on a given port card can be word synchronized to each other as described in Application Note 32. An example of using these transceivers as backplane interconnect links in a parallel switching fabric is shown below.

Figure 14: Back Plane Interconnect Using VSC870 Transceivers



4.2 Data Encoding Format

When the BYPASS signal is HIGH, the RXTYP[1:0] and TXTYP[1:0] signals are the direct representation of the overhead bits (B[1:0]) in the serial channels. For data words, the user can use these bits for signaling to the receiving port card. Information such as start of frame and end of frame can be passed with the data in this manner. Scrambling must be used in all cases. At the serial interface, the data words are scrambled to increase the signal edge transition density by setting the SCRAM input HIGH. When scrambling is enabled, a command word must be used to initialize the scrambling sequence. The transceiver checks for bit patterns on IDLE words to detect a link error condition. The encoding for the data at the parallel interface and the two overhead bits at the serial interface are described in the following table. The format for data words and command words is described in section 1.2.

TXTYP[1:0]RX TYP[1:0]	*B[1:0]*	*Direct Mode CELLSYN = 0*	*SCRAM = 1*	*SCRAM = 0*	*Error Check*
0 0	0 0	Command Word	No Scramble	No Scramble	IDLE words
0 1	0 1	Data Word	Scramble	No Scramble	No
1 0	1 0	Data Word	Scramble	No Scramble	No
1 1	1 1	Data Word	Scramble	No Scramble	No

4.3 Loop Timing

Loop timing depends on the source of the transmitters bit clock. For the case of using the transceiver in a simple port to port switching system, one transceiver can act as the master and one as the slave. The master will have LTIME set LOW so that its CMU will generate the bit timing. The slave will have LTIME set HIGH so that its transmitter uses the bit clock recovered from its clock recovery unit, therefore the whole system is in a single clock domain.

For the case of using the transceivers as a backplane interconnect link, all transceivers on the switch card have

© ***VITESSE*** *SEMICONDUCTOR CORPORATION* • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

their reference clock inputs from the same source and use their internal CMU as the transmit bit clock. In this case the LTIME signal is set LOW. The transceivers on the port card use the recovered bit clock as the source of the transmit bit clock, so LTIME must be set HIGH. The table in section 1.5 summarizes these modes of operation.

4.4 Link Initialization

Link initialization is completed at power up or at user request. Word alignment is done automatically on both transmit and receive data links. Either the transmit or receive side can be word aligned independently of each other. Either side can create a transmit clock from its local CMU source or from the clock recovered from the received serial data stream. The MODE[1] signal enables transmitter word alignment when it is set HIGH. The MODE[0] signal enables receiver word alignment when it is set HIGH. For any given serial connection, only one of these signals on each end of the link should be set HIGH.

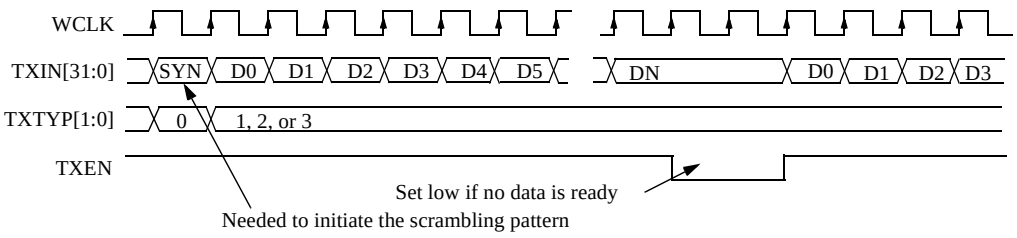
For the case of using the transceiver in a simple port to port switching system, only the receiver word aligner is enabled. The initialization sequence is as described in section 1.1 except that both transceivers start sending ALIGN words at power up. In this configuration, without the switch to act as the master in the initialization process, the receiver has to align to both the ALIGN words and the IDLE words for its word boundary.

For the case of using the transceivers in the backplane interconnect link, all transceivers on the switch card are used in master clock mode where they generate both the transmit and receive word boundary which the port cards align to. In this case, MODE[1:0] are set LOW for transceivers on the switch card. These transceivers are synchronized to a master REFCLK. Since each transceiver is word aligned to the REFCLK, they are all synchronized to the same word boundary and the same clock frequency at the switch fabric interface. Transceivers at the port cards perform word alignment on both the transmit and receive side so MODE[1:0] are set HIGH. The link initialization process is similar to the case of transceiver to the switch synchronization as described earlier in section 1.1.4.

4.5 Transmitter Operation

The functional timing diagram for the transmit side is shown below. Synch words be inserted into the data by setting TXTYP[1:0] = 00. This initiates the data scrambling sequence in the transceiver. Normal data words should be loaded into the transceiver with these bits set to 01, 10, or 11. If no data is ready to be transmitted at the parallel interface, TXEN should be set LOW and the transceiver will send out IDLE words.

Figure 15: Direct Mode Transmitter Functional Timing

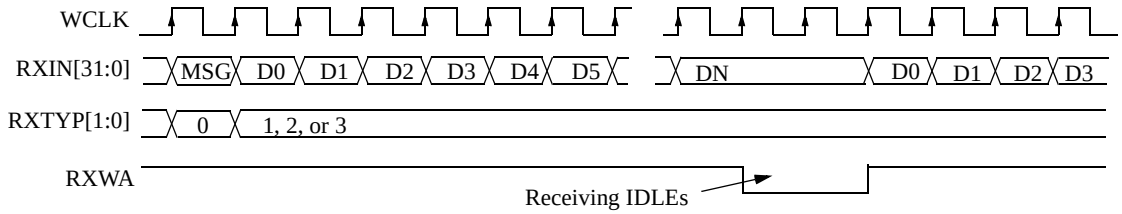


© VITESSE SEMICONDUCTOR CORPORATION • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

4.6 Receiver Operation

The functional timing diagram for the receive side is shown below. If a synch word is received, the signals RXTYP[1:0] will be set to 00. If data is received, these bits will be set to 01, 10, or 11. If IDLE words are received, the signal RXWA will go LOW.

Figure 16: Direct Mode Receiver Functional Timing



AC Characteristics

Table 1: LVDS and TTL Outputs

Parameters	Description	Min	Typ	Max	Units	Conditions
$T_{R,TTL}$	TTL Output Rise Time	2.5			ns	10-90% @ 50pF
$T_{F,TTL}$	TTL Output Fall Time	2.5			ns	10-90% @ 50pF
$T_{R,LVDS}$	LVDS Output Rise Time		100		ps	20-80%
$T_{F,LVDS}$	LVDS Output Fall Time		100		ps	20-80%

Figure 17: Transmit Data Input Timing Diagram

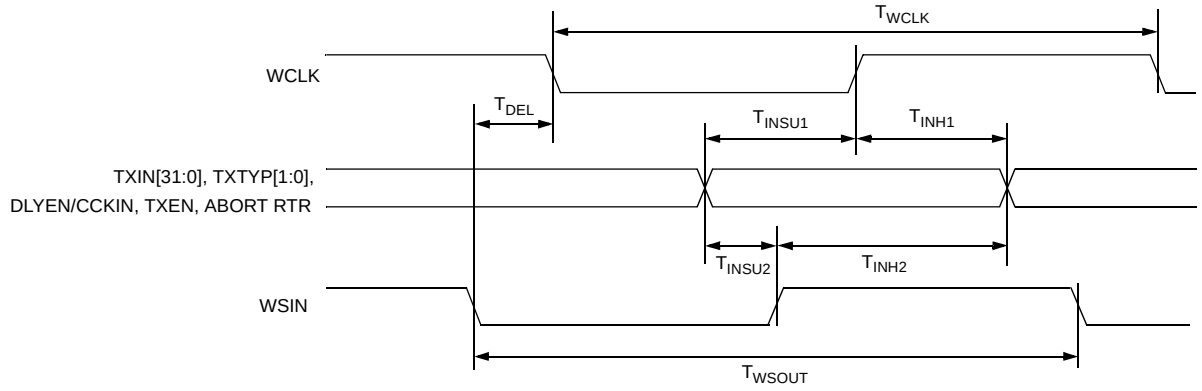


Table 2: Transmit Data Input Timing Table

Parameter	Description	Min	Typ	Max	Units
T_{WCLK}	Word clock period		16.0		ns
T_{INSU1}	TXIN[31:0] setup time with respect to WCLK	5.5			ns
T_{INSU1}	TXTYP[1:0] setup time with respect to WCLK	6.0			ns
T_{INSU1}	TXEN setup time with respect to WCLK	7.0			ns
T_{INSU1}	ABORT, RTR setup time with respect to WCLK	8.5			ns
T_{INH1}	Data hold time with respect to WCLK	0.0			ns
T_{WSOUT}	Word Synch Output clock period		16.0		ns
T_{INSU2}	TXIN[31:0] setup time with respect to WSIN	2.0			ns
T_{INSU2}	TXTYP[1:0] setup time with respect to WSIN	2.0			ns
T_{INSU2}	DLYEN/CCKIN, TXEN setup time with respect to WSIN	2.5			ns
T_{INSU2}	ABORT, RTR setup time with respect to WSIN	4.5			ns
T_{INH2}	Data hold time with respect to WSIN	2.0			ns
T_{DEL}	Delay time from WSIN to WCLK	1.6		5.5	ns

NOTE: Duty cycle for WCLK and WSOUT is 50% +/- 10% worst case.
During initialization, the WSOUT minimum pulse width can be reduced by an additional 1nS.

Figure 18: Receive Data Output Timing Diagram

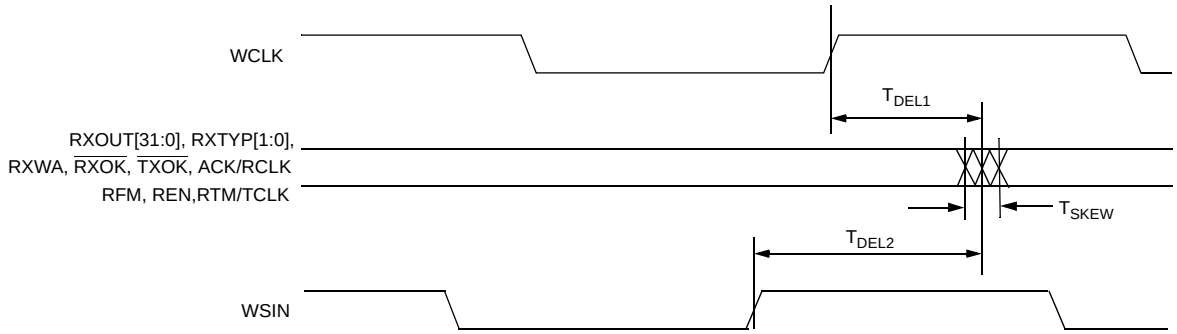


Table 3: Receive Data Output Timing Table

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{DEL1}	WCLK to RXOUT[31:0], RXTYP[1:0], RXWA, ACK/ RCLK, RXOK, TXOK, OOS delay	0.0		4.5	ns
T_{DEL1}	WCLK to RFM, REN, RTM/TCLK delay	0.7		7.0	ns
T_{DEL2}	WSIN to RXOUT[31:0], RXTYP[1:0], RXOK, TXOK, OOS delay	2.0		9.0	ns
T_{DEL2}	WSIN to RFM, REN, RTM delay	2.5		11.5	ns
T_{DEL2}	WSIN to RXWA, ACK/RCLK	1.5		7.5	ns
T_{SKEW}	Output data skew with respect to WCLK			1.5	ns
T_{DEL}	WCLK to TCLK delay	0.5		5.5	ns
T_{SKEW}	WCLK to WCLK skew using parallel transceivers			3.0	ns

Table 4: Misc. Timing Parameters

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{LT}	CMU and CRU lock time			100	us
T_{WS}	Word synchronization time			30	us
T_{CS}	Cell synchronization time per transceiver			(# words in cell)^2	WCLKs
T_{PM}	Data latency in packet mode with zero serial trace delay			8	WCLKs
T_{CM}	Data latency in cell mode with zero serial trace delay			12	WCLKs
T_{DM}	Data latency in direct mode with zero serial trace delay			6	WCLKs
T_{CRQ}	CRQ to REN delay time with zero serial trace delay			8	WCLKs
T_{REFCLK}	Reference (word) clock period		16		ns
F_{REFCLK}	Reference clock frequency stability			50	ppm
J_{REFCLK}	Reference clock input jitter			7	ps RMS

DC Characteristics

Table 5: LVDS and TTL Inputs and Outputs

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	I_{OH} = -6.0 mA
V_{OL}	Output LOW voltage (TTL)	—	—	0.4	V	I_{OL} = +6.0 mA
V_{OCM}	O/P Common Mode Range (LVDS)	1.2	—	2.1	V	At Min ΔV_{OUT}
ΔV_{OUT}	Differential Output Voltage (LVDS)	400	—	1000	mV	100Ω across input
V_{ICM}	I/P Common Mode Range (LVDS)	0.8	—	2.5	V	At Min ΔV_{IN}
ΔV_{IN}	Differential Input Voltage (LVDS)	200	—	1600	mV	—
V_{IH}	Input HIGH voltage (TTL)	2.0	—	V_{DD}+1.0	V	—
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	—	500	µA	V_{IN} =2.4V
I_{IL}	Input LOW current (TTL)	- 50	—	—	µA	V_{IN} = 0.4V

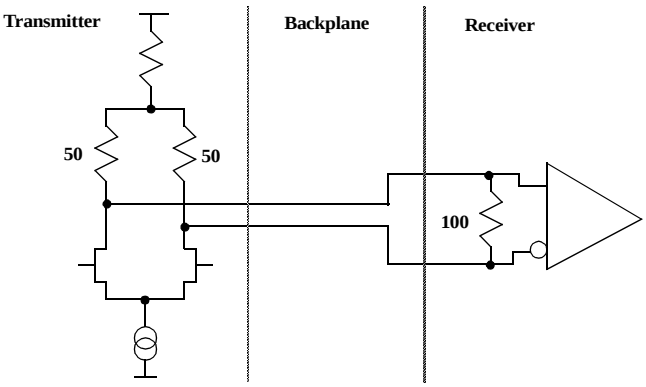
Hot Swap

The LVDS input and output buffers are subject to hot swap events while being connected and disconnected from the passive backplane. If the input is powered down but still receiving a signal from an output, the input must tolerate extra input current and power. If the input is powered up but has no input connection, it will go to a valid logic state. The table below lists the LVDS I/O parameters that relate to hot swap condition.

Table 6: Hot Swap LVDS I/O Parameters

Parameters	Description	Value	Units	Conditions
I_{CO}	LVDS maximum current delivered per output pin	10	mA	Normal Operation
I_{CI}	LVDS maximum current allowed per input pin	40	mA	V_{DD} = 0V
P_{CI}	LVDS maximum added power per output pin	60	mW	V_{DD} = 0V
V_{CDL}	LVDS input default logic state	LOW	—	Input Open

Figure 19: LVDS Input and Output Buffer Designs



Power Dissipation

Table 7: Power Supply Currents

Parameter	*Description*	*(Max)*	*Units*
I_{DD}	Power supply current from V_{DD} and V_{DDA} (V_{DD}, V_{DDA} = +3.3V + 5%)	1587	mA
I_{DDA}	Power supply current from V_{DDA} (V_{DDA} = +3.3V + 5%)	200	mA
P_D	Power dissipation (V_{DD}, V_{DDA} = +3.3V + 5%)	5.5	W

Absolute Maximum Ratings(1)

Power Supply Voltage (V_{DD}) Potential to GND ..... -0.5V to +4V
DC Input Voltage (LVDS inputs) ..... -0.5V to V_{DD} + 1.0V
DC Input Voltage (TTL inputs) ..... -0.5V to 5.5V
DC Output Voltage (TTL outputs) ..... -0.5V to V_{DD} + 1.0V
Output Current (TTL outputs) ..... +/-50mA
Output Current (LVDS outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C

NOTE: (1) Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{DD}, V_{DDA}) ..... +3.3V ±5 %
Extended Commercial Operating Temperature Range(1) (T) ..... 0°C to 85°C

NOTE: (1) Lower limit of specification is ambient temperature and upper limit is case temperature.

Package Pin Description

Signal	*Pin*
VSS	A01
REFCLK	A02
TXIN[3]	A03
TXIN[1]	A04
WSIN	A05
WSOUT	A06
VDD	A07
RXOUT[30]	A08
RXOUT[29]	A09
VDD	A10
RXOUT[24]	A11
RTR	A12
ABORT	A13
MODE[0]	A14
BYPASS	A15
VSS	A16
VDD	B01
VSCTE	B02
LOOPBACK	B03
TXIN[2]	B04
TXIN[0]	B05
RXWA	B06
VSS	B07
RXTYP[0]	B08
RXOUT[27]	B09
VSS	B10
RXOUT[23]	B11
RXEN	B12
RESET	B13
MODE[1]	B14
DLYEN/CCKIN	B15
VDD	B16
VDD	C01
RXSEL	C02
NC	C03
NC	C04
VSS	C05

Signal	*Pin*
VSS	C06
ACK/RCLK	C07
RXOUT[31]	C08
RXOUT[28]	C09
RXOUT[25]	C10
VSS	C11
VSS	C12
NC	C13
NC	C14
RESYNEN	C15
VDD	C16
VSS	D01
VDD	D02
VSS	D03
VDD	D04
VSS	D05
VDD	D06
RXTYP[1]	D07
VDD	D08
VSS	D09
RXOUT[26]	D10
VDD	D11
VSS	D12
VDD	D13
VSS	D14
VDD	D15
VSS	D16
RXSB-	E01
RXSB+	E02
VDD	E03
VDD	E04
VDD	E13
VSS	E14
RXOUT[22]	E15
RXOUT[21]	E16
RXSA-	F01
RXSA+	F02

Signal	*Pin*
VSS	F03
NC	F04
RXOUT[20]	F13
RXOUT[19]	F14
RXOUT[18]	F15
RXOUT[17]	F16
VSS	G01
VSS	G02
SCRAM	G03
VDD	G04
VDD	G13
RXOUT[14]	G14
RXOUT[15]	G15
RXOUT[16]	G16
TXSA-	H01
TXSA+	H02
VSS	H03
VDDA	H04
VSS	H13
RXOUT[13]	H14
RXOUT[12]	H15
RXOUT[11]	H16
TXSB+	J01
TXSB-	J02
LTIME	J03
VSSA	J04
VDD	J13
RXOUT[8]	J14
RXOUT[9]	J15
RXOUT[10]	J16
FACLPBK	K01
CELLSYN	K02
TESTEN	K03
VDD	K04
VSS	K13
RXOUT[7]	K14
RXOUT[6]	K15

Signal	*Pin*
RXOUT[5]	K16
TXIN[4]	L01
TXIN[5]	L02
$\overline{\text{RXOK}}$	L03
$\overline{\text{TXOK}}$	L04
RXOUT[1]	L13
RXOUT[2]	L14
RXOUT[3]	L15
RXOUT[4]	L16
OOS	M01
ALIVE	M02
VSS	M03
VDD	M04
VDD	M13
VSS	M14
RXOUT[0]	M15
WCLK	M16
VSS	N01
VDD	N02
VSS	N03
VDD	N04
VSS	N05
VDD	N06
TXIN[18]	N07
VDD	N08
VDD	N09
RTM/TCLK	N10
VDD	N11
VSS	N12
VDD	N13
VSS	N14
VDD	N15
VSS	N16
VDD	P01
TXIN[6]	P02
NC	P03
NC	P04

© ***VITESSE*** *SEMICONDUCTOR CORPORATION* • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

Signal	*Pin*
VSS	P05
VDD	P06
TXIN[17]	P07
TXIN[20]	P08
TXTYP[0]	P09
RFM	P10
VSS	P11
VSS	P12
NC	P13
NC	P14
TXIN[31]	P15

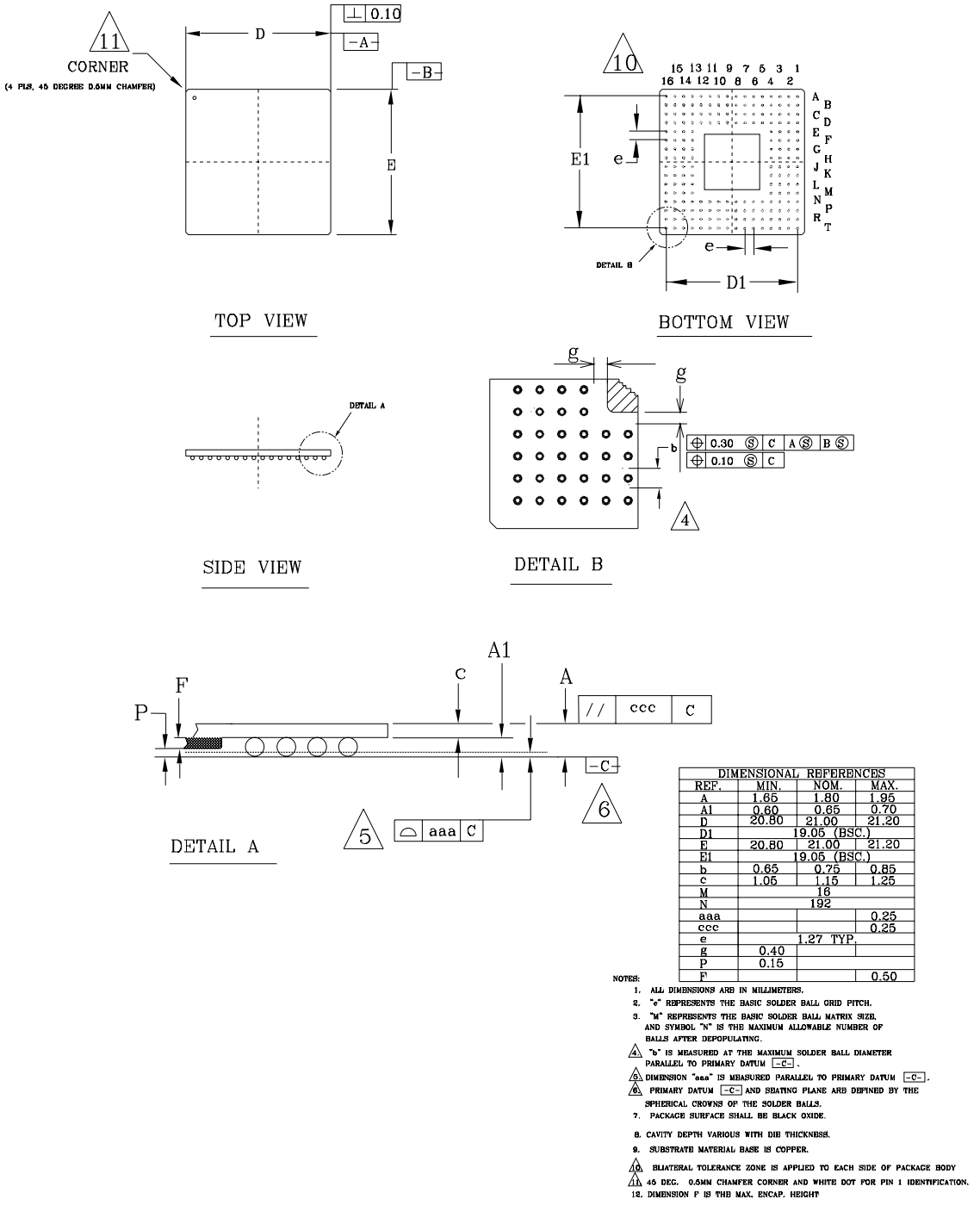
Signal	*Pin*
VDD	P16
VDD	R01
TXIN[7]	R02
TXIN[9]	R03
TXIN[11]	R04
TXIN[13]	R05
TXIN[15]	R06
VSS	R07
TXIN[19]	R08
TXTYP[1]	R09
VSS	R10

Signal	*Pin*
TXIN[22]	R11
TXIN[24]	R12
TXIN[26]	R13
TXIN[28]	R14
TXIN[30]	R15
VDD	R16
VSS	T01
TXIN[8]	T02
TXIN[10]	T03
TXIN[12]	T04
TXIN[14]	T05

Signal	*Pin*
TXIN[16]	T06
VDD	T07
TXIN[21]	T08
TXEN	T09
VDD	T10
REN	T11
TXIN[23]	T12
TXIN[25]	T13
TXIN[27]	T14
TXIN[29]	T15
VSS	T16

Package Information

192 BGA Package



DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	1.65	1.80	1.95
A1	0.60	0.65	0.70
D	20.80	21.00	21.20
D1		19.05 (BSC.)	
E	20.80	21.00	21.20
E1		19.05 (BSC.)	
b	0.65	0.75	0.85
c	1.05	1.15	1.25
M		16	
N		192	
aaa			0.25
ccc			0.25
e		1.27 TYP.	
g	0.40		
P	0.15		
F			0.50

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "M" REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE, AND SYMBOL "N" IS THE MAXIMUM ALLOWABLE NUMBER OF BALLS AFTER DEPOPULATING.
4. "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM -C-.
5. DIMENSION "aaa" IS MEASURED PARALLEL TO PRIMARY DATUM -C-.
6. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE SHALL BE BLACK OXIDE.
8. CAVITY DEPTH VARIOUS WITH DIE THICKNESS.
9. SUBSTRATE MATERIAL BASE IS COPPER.
10. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF PACKAGE BODY
11. 45 DEG. 0.6MM CHAMFER CORNER AND WHITE DOT FOR PIN 1 IDENTIFICATION.
12. DIMENSION F IS THE MAX. ENCAP. HEIGHT

Package Thermal Characteristics

The VSC870 is packaged in a thermally-enhanced 21mm 192TBGA with an embedded heat sink. The heat sink surface configurations are shown in the package drawings. With natural convection, the junction-to-case thermal resistance is estimated to be 1.49°C/W. The approximate air flow versus thermal resistance relationship is shown in Table 8. Refer to the application note AN-36 for thermal management and selection of heat sinks.

Table 8: Theta Junction-to-Ambient versus Air Velocity

Air Velocity (LFPM)	*Junction-to-Ambient Thermal Resistance (°C/W)*	
	Low Conductivity Two Layer Board	*High Conductivity Four Layer Board*
0	35.0	25.0
100	30.0	22.0
200	26.0	20.0
400	22.0	17.5
600	20.0	16.5

Ordering Information

The order number for this product is formed by a combination of the device number and package type.

VSC870 xx

Device Type
High Performance Serial Backplane Transceiver

Package
TX: 192 BGA
Extended Commerical Temperature: 0°C ambient to +85°C case

© ***VITESSE*** *SEMICONDUCTOR CORPORATION* • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com