Datasheet

VSC834

2.5Gb/s 17x17 Crosspoint Switch with Input Signal Activity (ISA) Monitoring

Features

- 17 Input by 17 Output Crosspoint Switch
- 2.5Gb/s NRZ Data Bandwidth
- 42 Gb/s Aggregate Bandwidth
- TTL Compatible µP Interface
- Differential PECL Data Inputs
- On-chip 50Ω Input Terminations
- 50Ω Source Terminated PECL Output Drivers
- Single 3.3V Supply
- 9W Maximum Power Dissipation
- High Performance 256 Pin BGA Package

General Description

The VSC834 is a monolithic 17x17 asynchronous crosspoint switch designed to carry broadband data streams at up to 2.5Gb/s. The non-blocking switch core is programmed through a parallel microprocessor interface that allows random access programming of each output port. A high degree of signal integrity is maintained through the chip through fully differential signal paths.

The crosspoint function is based on a multiplexer tree architecture. Each data output is driven by a 17:1 multiplexer tree that can be programmed to one and only one of its 17 inputs, and each data input can be programmed to multiple outputs. The signal path is unregistered, so no clock is required for the data inputs. The signal path is asynchronous, so there are no restrictions on the phase, frequency, or signal pattern at each input. Each input channel has an activity monitor function that can be used to identify loss of activity (LOA). An interrupt pin is provided to signal LOA, after which an external controller can query the chip to determine the channel(s) on which the fault occurred.

Each output driver is a fully differential switched current driver with on-die back-terminations for maximum signal integrity. Data inputs are terminated on die through 50Ω resistors connected to V_{TERM}.

The parallel interface uses TTL levels, and provides address, data, and control pins that are compatible with a microprocessor-style interface. The control port provides access to all chip functions, including LOA, and programming. Program buffering is provided to allow multiple program assignments to be queued and issued simultaneously via a single configure command.

VSC834 Block Diagram

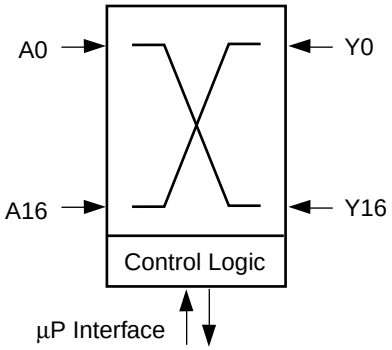
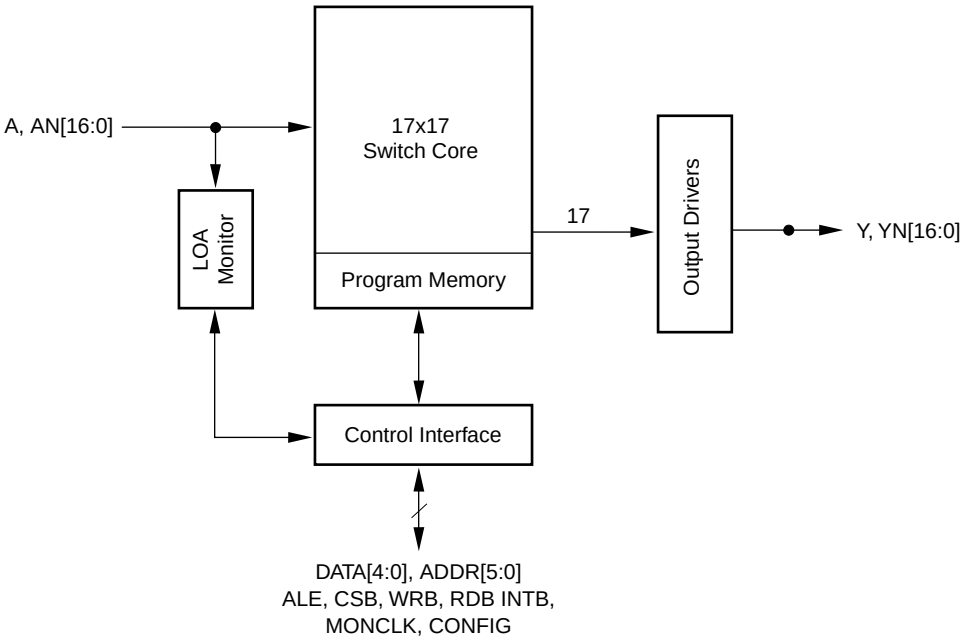


Figure 1: Detailed Block Diagram:



Functional Description

Data Paths

All input data must be differential and biased to PECL levels. On-chip terminations are provided, with a nominal impedance of 50Ω. All input termination resistors are tied to V_{TERM}.

Data outputs are provided through differential current switches with on-chip terminations that produce a PECL level output swing. The drive level of the output circuit is designed to produce standard PECL levels when terminated in 50Ω to 2.0V. Other termination voltages are possible, such as to V_{CC} or 1.3V, but the voltage level of the output swing will be shifted from its nominal value. The common-mode voltage of the output swing can be adjusted using the VCOM pin. The adjustment range is not calibrated, but typically allows for about ±200mV of adjustment in the output common-mode voltage.

Output channels can be powered off in pairs if fewer than 17 outputs are required. By connecting the VEE pin associated with a given pair of outputs to V_{CC}, the output pairs will pull to V_{CC} and chip power will be reduced by roughly 200mW.

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Programming Interface

The switch core is programmed through a parallel interface circuit that allows random reads or writes to the program memory array. The program memory array is buffered to allow multiple programming instructions to be loaded simultaneously with the CONFIG pin. Parallel programing can be clocked at up to a 50MHz rate.

The program data is composed of two parts: output address and input address. The output address, denoted by ADDR[5:0], specifies which output channel is to be programmed. The input address, denoted by DATA[4:0], specifies which input port the switch slice should connect to. The format of the program data is simple binary, where the binary value maps directly to the switch slice position and/or input port number. For example: ADDR[5:0] (000100) / DATA[4:0] (00110) would direct output channel Y4 to connect to input channel A6. The programming state may be verified (read back) by applying the address of the desired output and asserting RDB. The programming state is unknown at power-on. Additional address space is provided for access to the monitor registers (See Table 2). The microprocessor interface consists of the following signals. Levels are TTL (see Table 6).

Table 1: Signal Table

Pin	*I/O*	*Description*
D[5:0]	B	Bidirectional data bus to transfer data to/from internal program registers
A[5:0]	I	Address bus to select internal program registers for read-write operations
ALE	I	Address Latch Enable: for use with multiplexed address/data buses. Latches the address bus internally when low.
CSB	I	Chip Select (Active Low): assert this pin whenever the part is being read or programmed.
WRB	I	Write (Active Low): program data will be transferred to the first level internal registers on the rising edge of this signal (when CSB is also low).
RDB	I	Read (Active Low): program data from the internal program or monitor registers will be read out on the data bus when this signal goes low (with CSB also low).
INTB	O	Interrupt (Active Low): this signal is asserted when an LOA condition is found
CONFIG	I	Configure (Active High): assert this signal to transfer queued program information from the first-level internal registers to the second-level registers, making the programming take effect. This signal may be tied high to leave the second-level registers transparent so all programming will take effect immediately. CSB must be active (low) when CONFIG is asserted. CONFIG may be tied to a high-order bit of the address bus
MONCLK	I	Monitor states are transferred to monitor registers on the rising edge of this signal. MONCLK is not expected to exceed 3MHz.

Loss of Activity (LOA) Monitoring

The LOA function consists of an activity monitor on each input channel, connected directly to the pads. The state of a monitor (whether or not it has been toggled by an input transition) can be observed by applying the address (See Table 2) of the monitor register corresponding to the signal of interest and asserting RDB. Each monitor register is four bits in length, covering the state of four inputs or outputs. There is one extra one-bit monitor for each of the 17^{th} input and 17^{th} output. The state of each monitor is transferred to the register periodically on the rising edge of MONCLK, whereupon the activity monitor is clered until more activity is detected.

If any change in a monitor state occurs after sampling by MONCLK, an interrupt will be signalled by asserting INTB, and the user must identify the offending channel by reading the monitor states. The interrupt will be cleared when the corresponding activity monitor is read, but the monitor state will not be changed. If multiple monitors have triggered the interrupt, it will persist until all the corresponding monitors have been read.

The LOA circuitry requires a minimum signal level of 30-150 mV peak-peak to recognize an input as active. This is required to distinguish noise on an unconnected signal (where both inputs float to the termination voltage) from activity on a live signal. A minimum of two transitions defines activity. The threshold signal level can be adjusted with the VHYS pin, which can set the threshold from zero to the maximum allowed input swing. The VHYS pin will self-bias to a nomial value that will be appropriate for most applications (30-150mV p-p input level). Although uncalibrated for nominal level, gain and linearity, the VHYS pin can be externally set to adjust the threshold level over the entire range of the input signal, from zero to the maximum level allowed at the input.

Table 2: Memory Map

Address	*Access*	*Description*
00h	R/W	Output Y0's programmed input channel (write and then assert CONFIG to program)
01h	R/W	Output Y1's programmed input channel
...	...	...
10h	R/W	Output Y16's programmed input channel
11h	R/W	Internal output Y17's programmed input channel
...	...	...
20h	R/W	Internal output Y32's programmed input channel
21h	R/O	Rx Activity monitor for inputs A0, A1,A2,A3 (Logic '1'=No activity)
22h	R/O	Rx Activity monitor for inputs A4, A5,A6,A7
23h	R/O	Rx Activity monitor for inputs A8, A9,A10,A11
24h	R/O	Rx Activity monitor for inputs A12, A13,A14,A15
25h	R/O	Rx Activity monitor for input A16

AC Characteristics

Table 3: Data Path

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
F_{RATE}	Data rate	-	-	2.5	Gb/s
T_{ISKW}	Input channel delay skew (1)	-	300	-	ps
T_{OSKW}	Output channel delay skew (2)	-	300	-	ps
t_R, t_F	High-speed input rise/fall times, 20% to 80% (3)	-	-	150	ps
t_R, t_F	High-speed output rise/fall times, 20% to 80%	-	-	150	ps
t_{jP}	Output data eye jitter, peak-peak, 2^{23} PRBS (4)	-	-	100	ps

Note: Unless otherwise stated, all specifications are guaranteed but not tested.
Note 1: Skew between any two input channels to a given output.
Note 2: Skew between any two output channels from the same input channel.
Note 3: Required for high-speed output rise/fall spec at F_{RATE}=2.5 Gbits/s. For lower rate signals, use 0.375/F_{RATE}
Note 4: Broadband jitter added to a jitter-free signal; jitter is primarily in the form of ISI for random data

Figure 2: Interrupt Timing (Change in Monitor State Registers)

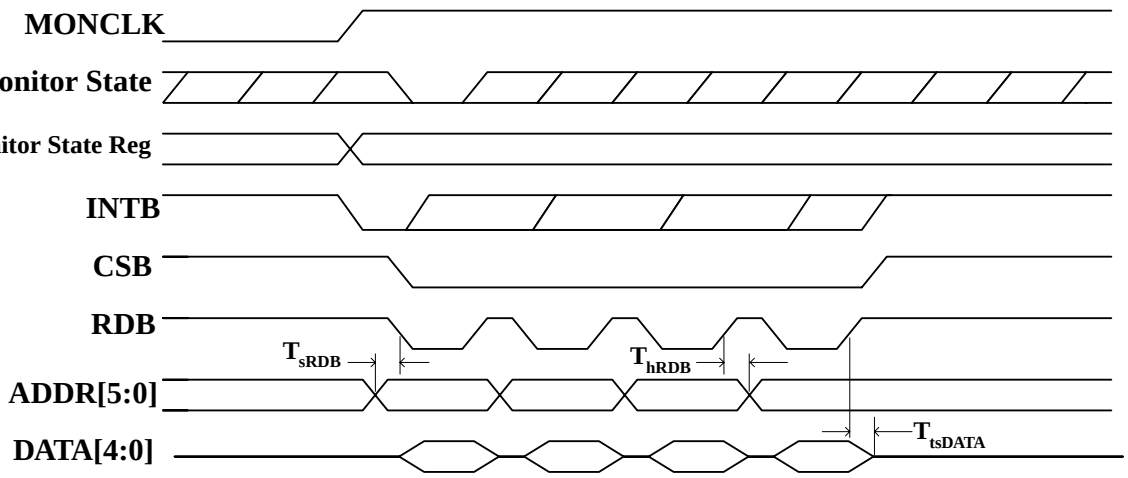

Figure 3: Interrupt Timing (No Change in Monitor State Registers)

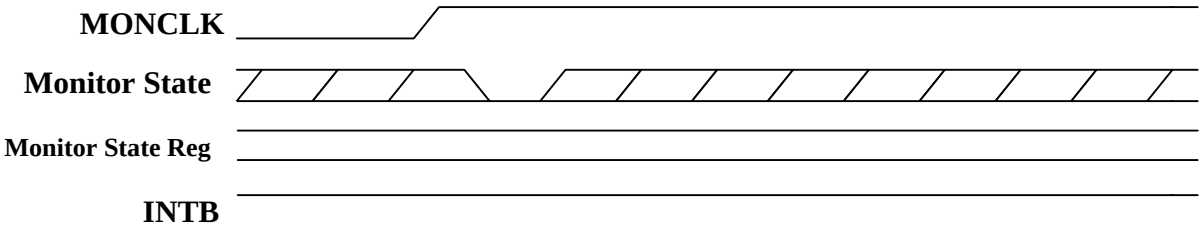

Figure 4: Program Timing

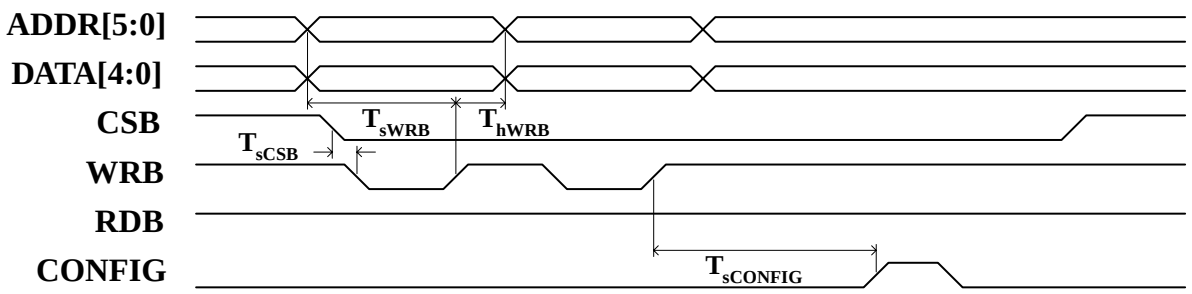

Table 4: Programing Port Interface Timing

Parameter	*Description*	*Min*	*Max*	*Units*
T_{config}	Switch configuration delay	-	6	ns
T_{pdADDR}	Data read propagation delay from ADDR	-	30	ns
T_{pdRDB}	Data read propagation delay from RDB (1)	-	7	ns
T_{pdint}	Interrupt propagation delay from MONCLK (2)	-	50	ns
$T_{pdstate}$	MONCLK to internal state register change delay (2)	-	6	ns
T_{sRDB}	ADDR to RDB setup time	5	-	ns
T_{hRDB}	RDB to ADDR hold time	3	-	ns
T_{sWRB}	WRB setup time (for either ADDR or DATA)	5	-	ns
T_{hWRB}	WRB hold time (for either ADDR or DATA)	3	-	ns
$T_{sCONFIG}$	WRB to CONFIG setup time	1	-	ns
T_{sCSB}	CSB setup time (to either WRB or RDB)	0	-	ns
$T_{pwCONFIG}$	CONFIG pulse width (high)	10	-	ns
T_{pwWRB}	WRB pulse width (low and high)	10	-	ns
T_{pwRDB}	RDB pulse width (low and high)	10	-	ns
T_{tsDATA}	DATA tri-state delay (from either RDB or CSB) (2)	-	10	ns
T_{sALE}	ALE setup time (for multiplexed ADDR/DATA bus)	5	-	ns

Note 1: Measured from falling edge.
Note 2: Measured from rising edge.

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DC Characteristics *(All Characteristics Are Over The Specified Operating Conditions)*

Table 5: Power

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{CC}	V_{CC} supply current			2600	mA	
P_T	Total chip power (V_{CC} = 3.45V and +85ºC case)			9	W	
I_{TERM-V}	V_{TERM} supply current with V_{TERM} =V_{CC}-1.3V			~0	mA	
I_{TERM-E}	V_{TERM} supply current with V_{TERM} =V_{CC}-2.0V			-600	mA	

Note: I_{CC} Specified with outputs terminated with 50Ω to +2.0V and Chip V_{TERM}=+2.0V.

Table 6: Control Port Input Levels

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{VCOM}	VCOM bias voltage (L and R)		2.0		V	V_{CC}=3.3V
V_{VHYS}	VHYS bias voltage		1.65		V	V_{CC}=3.3V
V_{IH}	Input HIGH voltage (TTL)	2.0	—	3.5	V	—
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	—	500	µA	V_{IN} = 2.4V
I_{IL}	Input LOW current (TTL)	—	—	-500	µA	V_{IN} = 0.5V
I_{OZ}	Tristate output current (TTL)	-100	—	100	µA	V_{OUT} = 0.4V-2.4V

Table 7: Data Input Levels (Differential PECL)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{ID}	Input differential voltage	200	—	1000	mV	—
V_{ICM}	Input common-mode voltage	1.8	—	2.2	V	V_{CC}=3.3V

Table 8: Data Output Levels (Differential PECL)

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OD}	Output differential voltage	600	—	1000	mV	Note 1
V_{OCM}	Output common-mode voltage	1.8	—	2.2	V	Note 1

NOTE: (1) Nominal PECL mode, V_{CC}=V_{CCP}=3.3V, V_{EE}=0, terminated 50Ω to +2.0V.

Absolute Maximum Ratings

Power Supply Voltage (V_{CC}) Potential to GND ..... -0.5 V to +4.0 V
TTL Input Voltage Applied ..... -0.5 V to V_{CC} +0.5 V
ECL Input Voltage Applied ..... -0.5 V to V_{CC} +0.5 V
Output Current (I_{OUT}) ..... 50 mA
Input Current (I_{IN}) ..... ±50 mA
V_{TERM} Current (I_{TERM}) ..... ±800 mA
Case Temperature Under Bias (T_C) ..... -55°C to + 125°C
Storage Temperature (T_{STG}) ..... -65°C to + 150°C

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Operating Conditions

Supply voltage (V_{EE}) ..... 0 V
Supply voltage (V_{CC}) ..... +3.3V ±5%
Supply voltage (V_{CCP}) ..... +3.3V ±5%
Termination voltage (V_{TERM}) ..... V_{CC} -1.3V
Case Temperature Operating Range (T) ..... 0°C to 85°C
Junction Temperature Operating Range (T_J) ..... 0°C to 110°C

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC834 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1000V.

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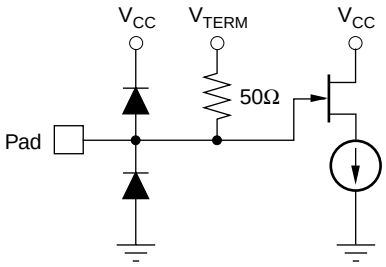
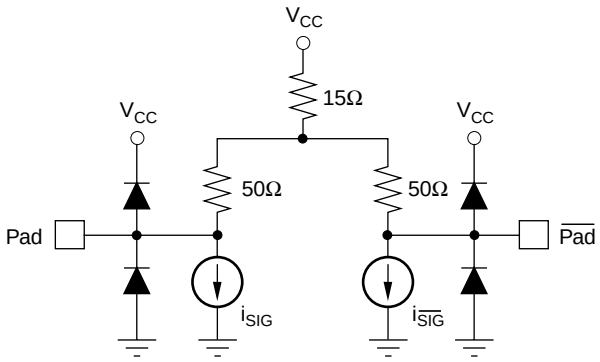
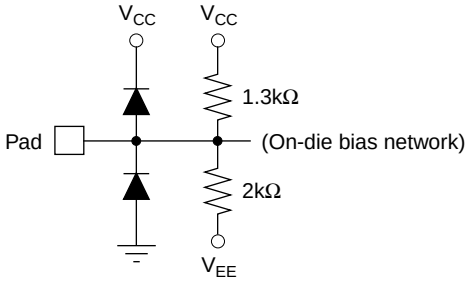
I/O Equivalent Circuits



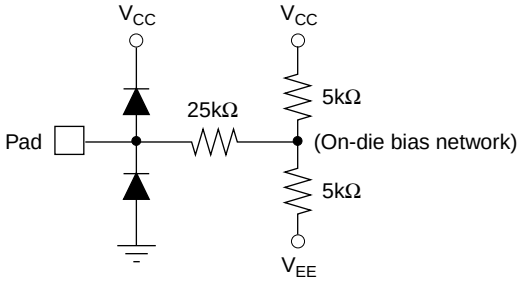
PECL Input Equivalent Circuit



PECL Output Equivalent Circuit



V_{COM} (L or R) Input
Equivalent Circuit



V_{HYS} (C or L) Input
Equivalent Circuit

Package Pin Descriptions

The VSC834 is packaged in a 27x27mm 256 pin ball grid array package. The 256 BGA package is thermally enhanced and carries the high-speed signals over controlled impedance lines from the solder ball to the circuit die. The following sections describe the pinout and mechanical details of the VSC834.

Figure 5: Functional Pinout Floorplan

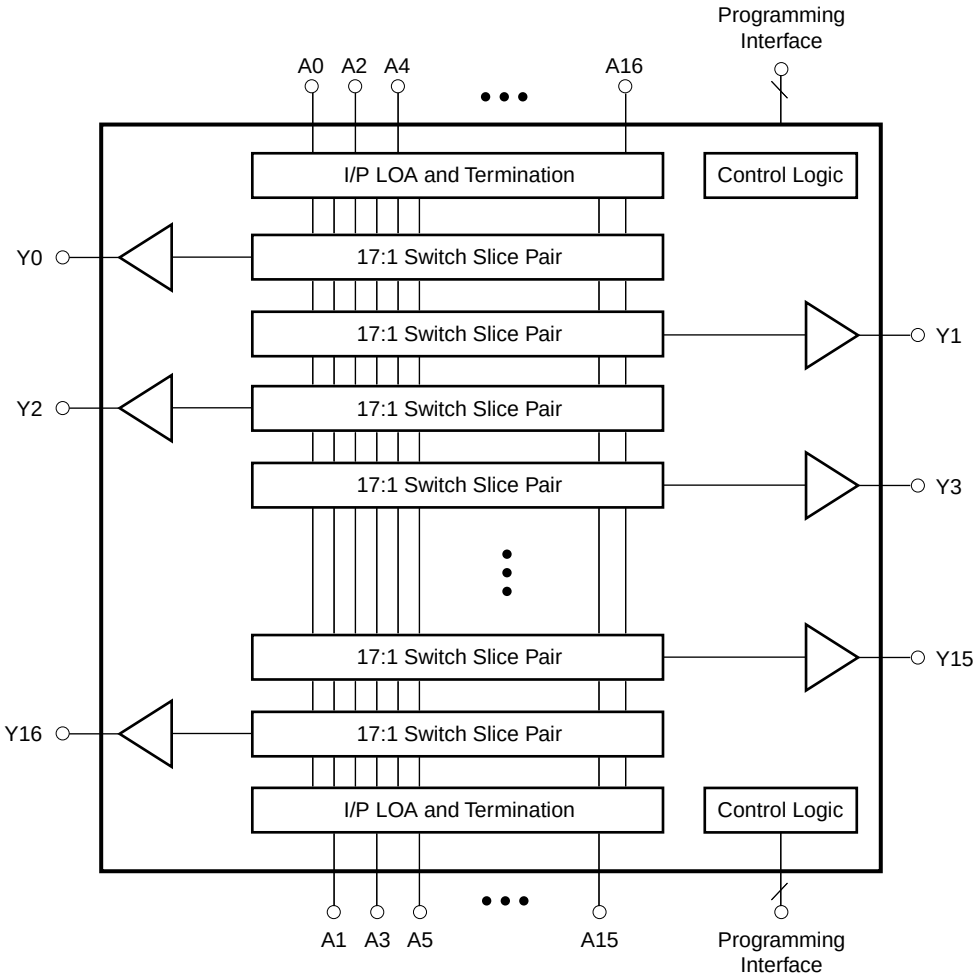


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Figure 6: Pinout Diagram

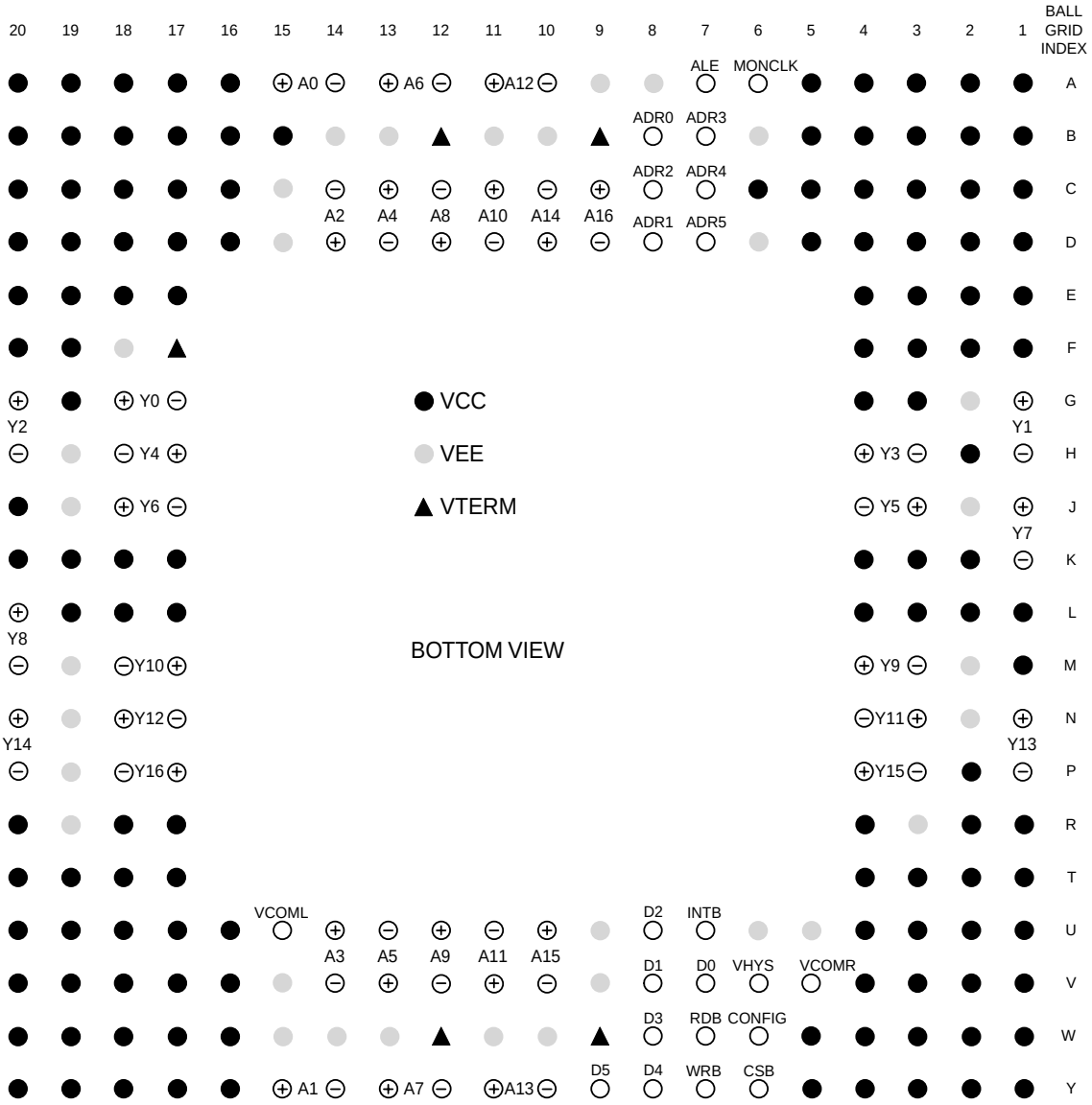

Table 9: Pin Identification

Signal Name	*Pin*	*Function*	*Level*
	High Speed Data Inputs		
A0, NA0	A15, A14	Data Input	PECL
A1, NA1	Y15, Y14	Data Input	PECL
A2, NA2	D14, C14	Data Input	PECL
A3, NA3	U14, V14	Data Input	PECL
A4, NA4	C13, D13	Data Input	PECL
A5, NA5	V13, U13	Data Input	PECL
A6, NA6	A13, A12	Data Input	PECL
A7, NA7	Y13, Y12	Data Input	PECL
A8, NA8	D12, C12	Data Input	PECL
A9, NA9	U12, V12	Data Input	PECL
A10, NA10	C11, D11	Data Input	PECL
A11, NA11	V11, U11	Data Input	PECL
A12, NA12	A11, A10	Data Input	PECL
A13, NA13	Y11, Y10	Data Input	PECL
A14, NA14	D10, C10	Data Input	PECL
A15, NA15	U10, V10	Data Input	PECL
A16, NA16	C9, D9	Data Input	PECL
	High Speed Data Outputs		
Y0, YN0	G18, G17	Data Output	PECL
Y1, YN1	G1, H1	Data Output	PECL
Y2, YN2	G20, H20	Data Output	PECL
Y3, YN3	H4, H3	Data Output	PECL
Y4, YN4	H17, H18	Data Output	PECL
Y5, YN5	J3, J4	Data Output	PECL
Y6, YN6	J18, J17	Data Output	PECL
Y7, YN7	J1, K1	Data Output	PECL
Y8, YN8	L20, M20	Data Output	PECL
Y9, YN9	M4, M3	Data Output	PECL
Y10, YN10	M17, M18	Data Output	PECL
Y11, YN11	N3, N4	Data Output	PECL
Y12, YN12	N18, N17	Data Output	PECL
Y13, YN13	N1, P1	Data Output	PECL
Y14, YN14	N20, P20	Data Output	PECL
Y15, YN15	P4, P3	Data Output	PECL

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Table 9: Pin Identification

Signal Name	*Pin*	*Function*	*Level*
Y16, YN16	P17, P18	Data Output	PECL
Programming Port			
ADR0	B8	Program data address	TTL
ADR1	D8	Program data address	TTL
ADR2	C8	Program data address	TTL
ADR3	B7	Program data address	TTL
ADR4	C7	Program data address	TTL
ADR5	D7	Program data address	TTL
D0	V7	Program data	TTL
D1	V8	Program data	TTL
D2	U8	Program data	TTL
D3	W8	Program data	TTL
D4	Y8	Program data	TTL
D5	Y9	Program data	TTL
ALE	A7	Address latch enable (active high)	TTL
INTB	U7	Interrupt (active low)	TTL
RDB	W7	Read enable (active low)	TTL
WRB	Y7	Write enable (active low)	TTL
CONFIG	W6	Configuration strobe (active high)	TTL
CSB	Y6	Chip select (active low)	TTL
MONCLK	A6	Loss of activity monitor clock (active high)	TTL
Power Supplies			
VCC	A1, A2, A3, A4, A5, A16, A17, A18, A19, A20, B1, B2, B3, B4, B5, B15, B16, B17, B18, B19, B20, C1, C2, C3, C4, C5, C6, C16, C17, C18, C19, C20, D1, D2, D3, D4, D5, D16, D17, D18, D19, D20, E1, E2, E3, E4, E17, E18, E19, E20, F1, F2, F3, F4, F19, F20, G3, G4, G19, H2, J20, K2, K3, K4, K17, K18, K19, K20, L1, L2, L3, L4, L17, L18, L19, M1, P2, R1, R2, R4, R17, R18, R20, T1, T2, T3, T4, T17, T18, T19, T20, U1, U2, U3, U4, U16, U17, U18, U19, U20, V1, V2, V3, V4, V16, V17, V18, V19, V20, W1, W2, W3, W4, W5, W16, W17, W18, W19, W20, Y1, Y2, Y3, Y4, Y5, Y16, Y17, Y18, Y19, Y20	Power	+3.3V

Table 9: Pin Identification

Signal Name	***Pin***	***Function***	***Level***
VEE	A8, A9, B6, B10, B11, B13, B14, C15, D6, D15, F18, M19, R3, U5, U6, U9, V9, V15, W10, W11, W13, W14, W15	Power	GND
VEE	H19	Power for output channels 0, 2	GND
VEE	G2	Power for output channels 1, 3	GND
VEE	J19	Power for output channels 4, 6	GND
VEE	J2	Power for output channels 5, 7	GND
VEE	N19	Power for output channels 8, 10	GND
VEE	M2	Power for output channels 9, 11	GND
VEE	P19	Power for output channels 12, 14	GND
VEE	N2	Power for output channels 13, 15	GND
VEE	R19	Power for output channel 16	GND
VTERM	B9, B12, F17, W9, W12	Termination power	+2.0V
Miscellaneous			
VCOML	U15	Slicing level for Y0 - YN16 (even)	ANALOG
VCOMR	V5	Slicing level for Y1 - YN15 (odd)	ANALOG
VHYS	V6	Loss of activity hysterisis threshold	ANALOG

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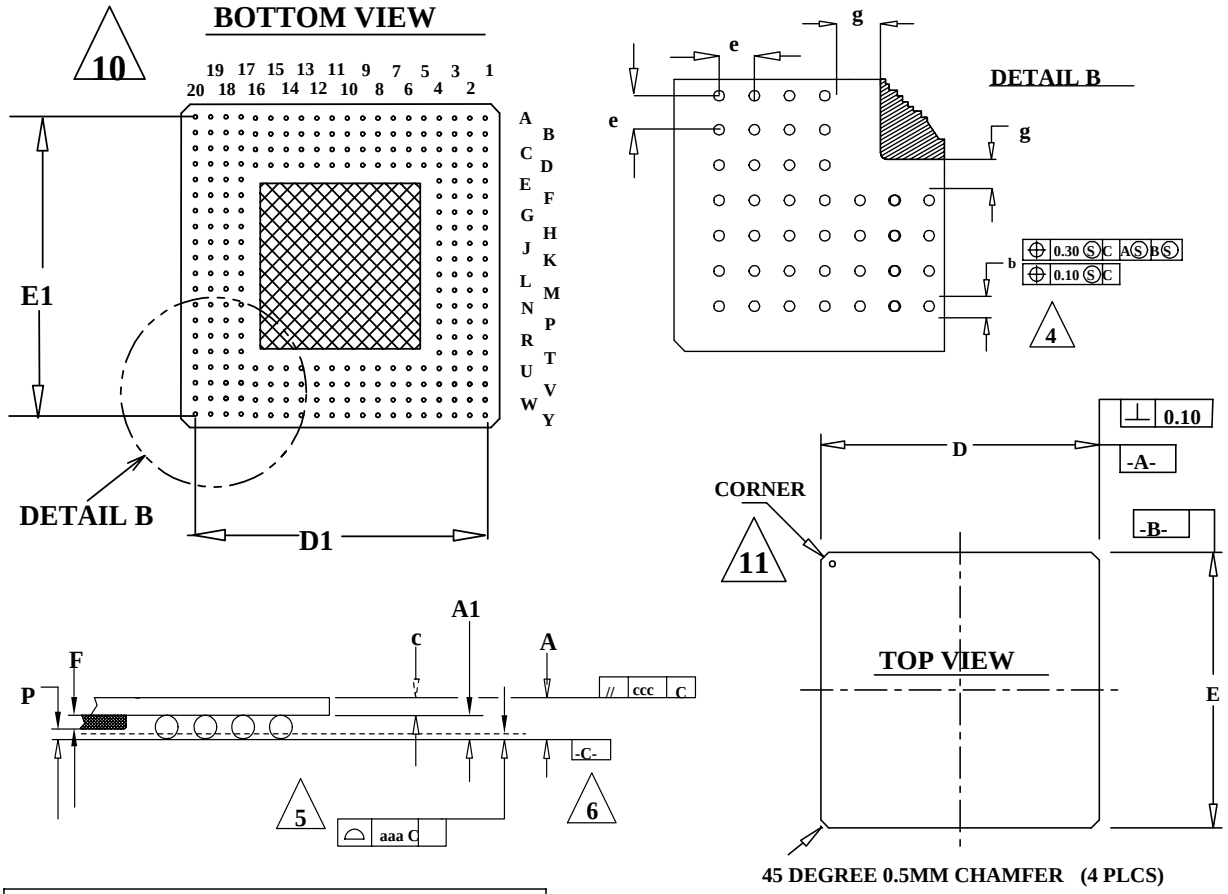
Package Information

27mm 256 BGA Package Drawing



45 DEGREE 0.5MM CHAMFER (4 PLCS)

DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	1.65	1.80	1.95
A1	0.60	0.65	0.70
D	26.80	27.00	27.20
D1		24.13 (BSC.)	
E	26.80	27.00	27.20
E1		24.13 (BSC.)	
b	0.65	0.75	0.85
c	1.05	1.15	1.25
M		20	
N		256	
aaa			0.25
ccc			0.25
e		1.27 TYP.	
P	0.15		
g	0.40		
F			0.50

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "M" REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE, AND SYMBOL "N" IS THE MAXIMUM ALLOWABLE NUMBER OF BALLS AFTER DEPOPULATING.
4. "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM -C- .
5. DIMENSION "aaa" IS MEASURED PARALLEL TO PRIMARY DATUM -C- .
6. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. PACKAGE SURFACE SHALL BE BLACK OXIDE.
8. CAVITY DEPTH VARIOUS WITH DIE THICKNESS
9. SUBSTRATE MATERIAL BASE IS COPPER.
10. BILATERAL TOLENANCE ZONE IS APPLIED TO EACH SIDE OF PACKAGE BODY
11. 45 DEG 0.5 mm CHAMFER CORNER AND WHITE DOT FOR PIN 1 IDENTIFICATION.
12. DIMENSION F IS THE MAX. ENCAP. HEIGHT

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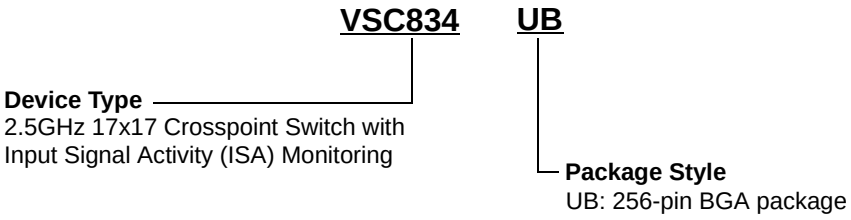
Internet: www.vitesse.com

Ordering Information

The order number for this product is formed by a combination of the device number, and package type.



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