Preliminary Datasheet

VSC8131

2.488 Gbit/sec
32:1 SONET/SDH Mux with Clock Generator

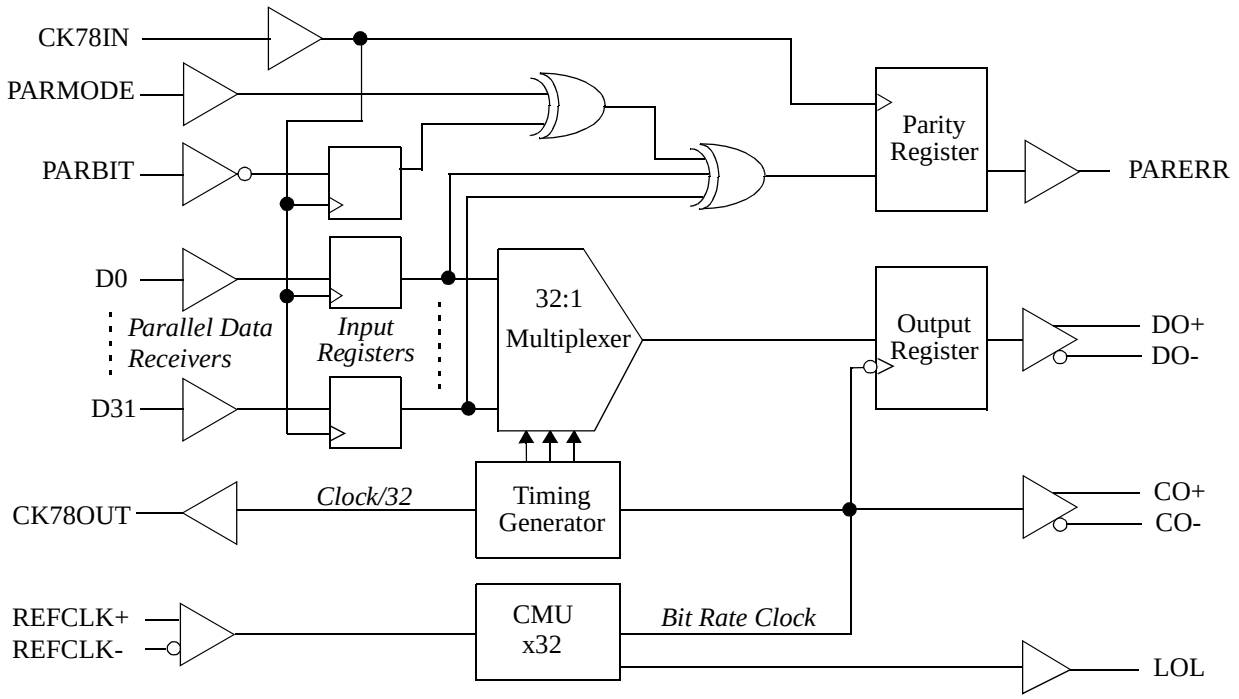
Features

- 2.488Gb/s 32:1 Mux with Clock Generator
- SONET STS-48/SDH STM-16
- LVPECL Differential High Speed Serial Data and Clock Outputs
- 32 TTL Parallel Data Inputs with Odd/Even Parity Check
- 128 Pin, 14x20x2 mm Enhanced-PQFP
- Single 3.3V Supply
- 2.15W Max Power Dissipation

General Description

The VSC8131 multiplexes 32 TTL compatible 77.76Mb/s Parallel Data Inputs (D0-D31) into a single LVPECL 2.488 Gb/s serial output (DO±) for use in SONET STS-48/SDH STM-16 systems. An integrated Clock Multiplier Unit (CMU) generates a LVPECL 2.488 GHz clock signal (CO±) from an externally supplied LVPECL compliant 77.76MHz reference clock (REFCLK±) which is used to retime the transmitted serialized data. A Divide-by-32 TTL clock output (CK78OUT) is used as a clock input (CK78IN) for timing of the parallel data inputs. Parity Checking (PARBIT) is performed on the incoming data with a selectable even or odd TTL parity mode input (PARMODE) and a TTL Parity Error (PARERR) output. A TTL Loss Of Lock (LOL) output indicator is used to report the loss of the REFCLK± or for conditions resulting in the CMU losing lock to incoming clock.

VSC8131 Block Diagram



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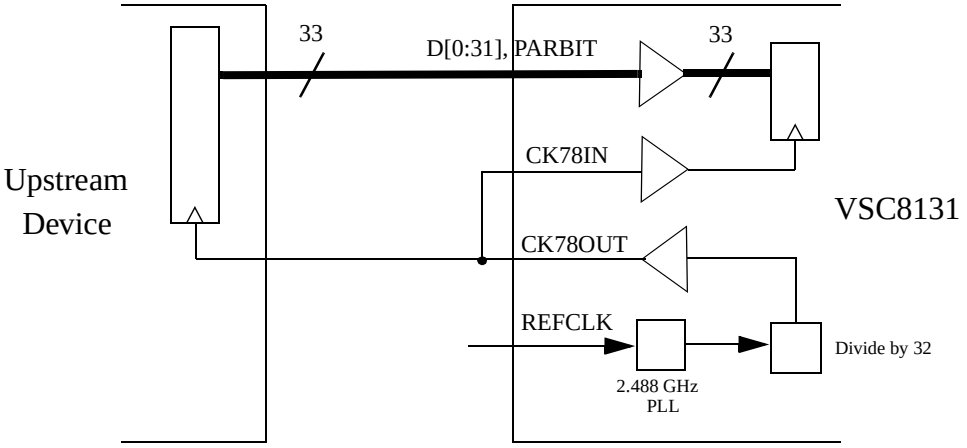
Functional Description

Low Speed Interface

The timing for the low speed parallel interface is based upon the CK78OUT output signal. The intent is to have the device upstream from the VSC8131 use the CK78OUT clock signal as the timing source for its final output stage latch. CK78IN is to be driven by CK78OUT, refer to Figure 1. This reduces the setup time of the VSC8131. The maximum propagation delay permitted from CK78OUT to CK78IN is specified by t_{CKPROP} in the AC Characteristics. The setup and hold time of the data inputs are specified with respect to the rising edge of CK78IN. D0-D31, CK78OUT, and CK78IN are TTL compatible inputs.

Figure 1: Low Speed System Interface



Parity

A parity check is performed between the parity bit input (PARBIT) and the 32 parallel data inputs (D0-D31). Even versus odd parity checking is selected with PARMODE. Set PARMODE low to test for odd parity. Set PARMODE high to test for even parity. The parity error output (PARERR) is set to a logic high when a parity error has occurred. The PARERR signal can be changed from an active high to active low signal by complementing the PARMODE input. PARERR is re-calculated each time new parallel data is clocked in. The newly calculated PARERR result is clocked out on the rising edge of CK78IN 2 cycles after the data is loaded. PARBIT, PARMODE, and PARERR conform to TTL output levels.

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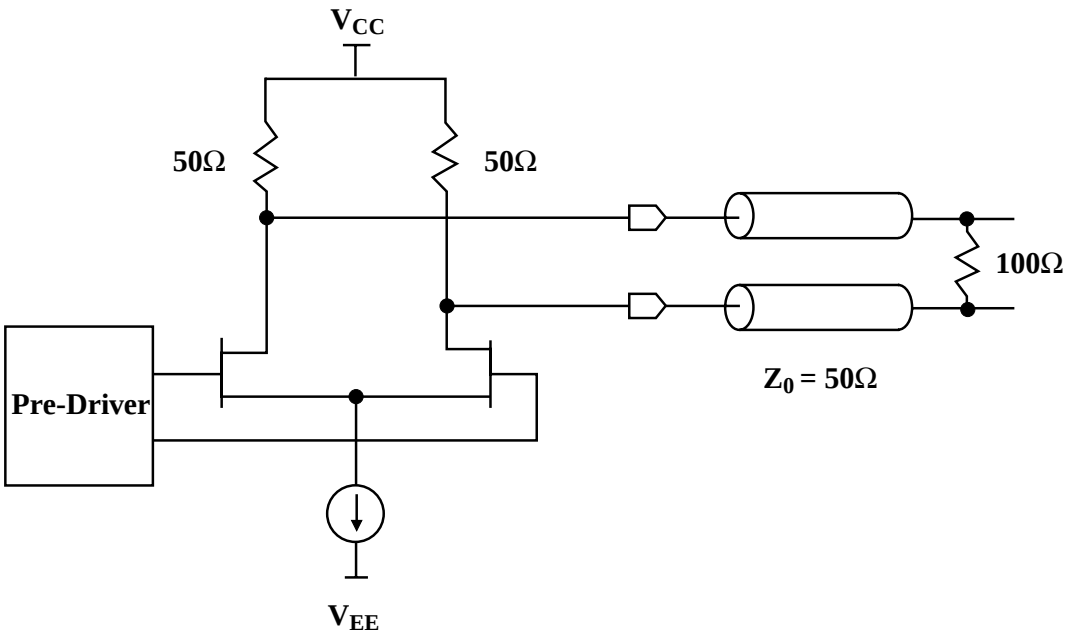
High Speed Data Output

The high speed data will be multiplexed in the sequence D0, D1 up to D31 with D0 being transmitted first. The high speed data output driver consists of a differential pair designed to drive a 50Ω transmission line. The transmission line should be terminated with a 100Ω resistor at the load between the true and complement outputs, refer to Figure 2. No connection to a termination voltage is required. The output driver is back terminated to 50Ω on-chip, providing snubbing of any reflections. If used single-ended, the high speed output driver must still be terminated differentially at the load with a 100Ω resistor between the true and complement output signals.

High Speed Clock Output

The high speed clock output driver consists of a differential pair designed to drive a 50Ω transmission line. The transmission line should be terminated with a 100Ω resistor at the load between the true and complement output, refer to Figure 2. No connection to a termination voltage is required. The output driver is back terminated to 50Ω on-chip, providing a snubbing of any reflections. If used single-ended, the high speed output driver must still be terminated differentially at the load with a 100Ω resistor between the true and complement output signals.

Figure 2: Termination for High Speed Clock and Data Output Drivers



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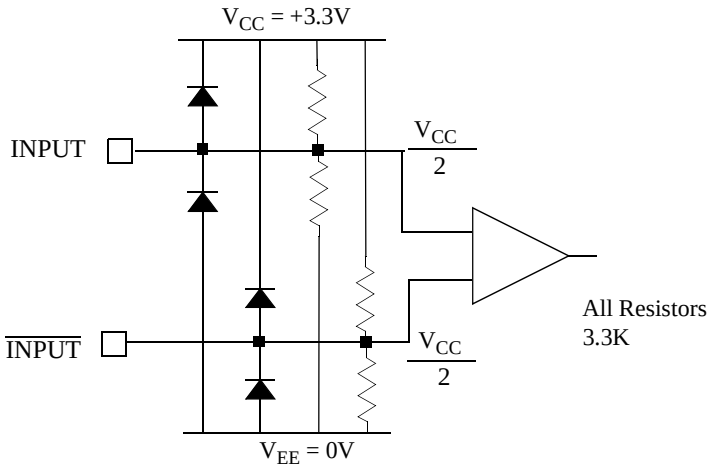
Clock Generator

An on-chip Phase Locked Loop (PLL) generates the 2.488 GHz transmit clock from the externally provided REFCLK input. The on-chip PLL uses a low phase noise reactance based Voltage Controlled Oscillator (VCO) with an on-chip loop filter. The loop bandwidth of the PLL is within the SONET specified limit of 2MHz. The REFCLK is 77.76MHz and should be of high quality. Noise on the REFCLK below the loop band width of the PLL will pass through the PLL and appear as jitter on the output. Preconditioning of the REFCLK signal with a VCXO may be required to avoid passing REFCLK noise with greater than 4ps RMS of jitter to the output. Such a condition would create an output from the VSC8131 which has the REFCLK noise in addition to the intrinsic jitter from the VSC8131 itself. REFCLK is a LVPECL level and is required to be a differential signal in order to meet the 4pS RMS jitter spec. The true and complement inputs of the differential PECL receiver are internally biased to VCC/2 so that the REFCLK signal can be AC coupled without using external bias resistors, refer to Figure 3. REFCLK can be DC coupled by simply over-driving the internal bias voltage.

Figure 3: REFCLK Internal Bias Configuration



Loss of Lock

The Loss Of Lock (LOL) output is used to indicate if the CMU is locked. A loss of lock condition is reported when the CMU does not lock to the REFCLK frequency or when the REFCLK input signal is not present. LOL is high when the CMU is locked. LOL is low when the REFCLK input signal is not present (input floating due to cut line or input stuck high or low). The LOL signal will appear as a pulse train of 1's and 0's when the REFCLK is present, but the CMU is not locked to the REFCLK's frequency. The frequency of the LOL pulse train can be anywhere from 500Hz to 50MHz.

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Supplies

This device is specified as a LVPECL device with a single +3.3V supply. Normal operation is to have V_{CC}=+3.3V and V_{EE}=ground. Should the user desire to use the device in an ECL environment with a negative 3.3V supply, then V_{CC} will be ground and V_{EE} will be -3.3V. If used with V_{EE} tied to -3.3V, the TTL I/O signals are still referenced to V_{EE}.

Decoupling of the power supplies is a critical element in maintaining the proper operation of the part. It is recommended that the V_{CC} power supply be decoupled using a 0.1µF and 0.01µF capacitor placed in parallel on each V_{CC} power supply pin as close to the package as possible. If room permits, a 0.001µF capacitor should also be placed in parallel with the 0.1µF and 0.01µF capacitors mentioned above. Recommended capacitors are low inductance ceramic SMT X7R devices. For the 0.1µF capacitor, a 0603 package should be used. The 0.01µF and 0.001µF capacitors can be either 0603 or 0403 packages.

Extra care needs to be taken when decoupling the analog power supply pins (labeled V_{CCANA}). In order to maintain the optimal jitter and loop bandwidth characteristics of the PLL contained in the VSC8131, the analog power supply pins should be filtered from the main power supply with a 10µH C-L-C pi filter. If preferred, a ferrite bead may be used to provide the isolation. The 0.1µF and 0.01µF decoupling capacitors are still required and must be connected to the supply pins between the device and the C-L-C pi filter (or ferrite bead).

For low frequency decoupling, 47µF tantalum low inductance SMT caps are sprinkled over the board's main +3.3V power supply and placed close to the C-L-C pi filter.

If the device is being used in an ECL environment with a negative 3.3V supply, then all references to decoupling V_{CC} must be changed to V_{EE}, and all references to decoupling +3.3V must be changed to -3.3V.

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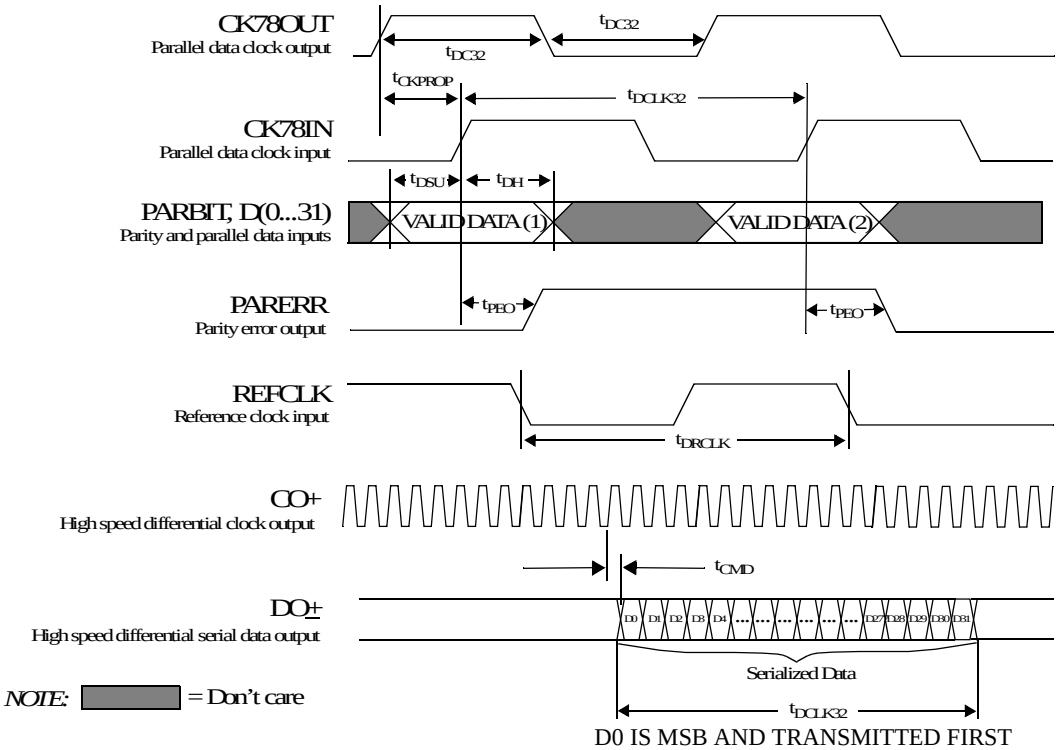
AC Characteristics

Table 1: VSC8131 Multiplexer AC Characteristics (*Over recommended operating conditions*)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
t_{DRCLK}	REFCLK period		12.8	-	ns
t_{DCLK32}	CK78IN period		12.8	-	ns
t_{DC32}	CK78OUT (CLK/32) duty cycle	40	-	60	%
t_{DCLOL}	LOL Duty Cycle (When CMU is not locked)	40	-	60	%
t_{DSU}	D(0-31) and PARBIT set-up time (wrt CK78IN rising edge)	1.0	-	-	ns
t_{DH}	D(0-31) and PARBIT hold time (wrt CK78IN rising edge)	1.0	-	-	ns
t_{PEO}	Parity error output timing; rising edge of CK78IN to PARERR	1.9		6.0	ns
t_{CKPROP}	Allowable propagation delay for connecting CK78OUT to CK78IN	0		3.0	ns
t_{CMD}	High speed clock output (CO±) timing; falling edge of CO+ to muxed data output (DO±)	100		270	ps
t_r, t_f	REFCLK rise and fall times (10%-90%)	-	-	1.5	ns
t_r, t_f	D(0.31) rise and fall times (10%-90%)	-	-	2.0	ns
t_r, t_f	CK78OUT, LOL and PARERR rise and fall times (10%-90%)	-	-	4.0	ns
t_r, t_f	DO± rise and fall times (20%-80%)	-	150	170	ps
t_r, t_f	CO± rise and fall times (20%-80%)	-	150	170	ps

Figure 4: VSC8131 Multiplexer Waveforms



D0 IS MSB AND TRANSMITTED FIRST

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DC Characteristics

Table 2: VSC8131 Multiplexer DC Characteristics (*Over recommended operating conditions*)

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
$V_{OH(DO)}$	Output HIGH voltage (DO)	V_{CC}-0.050	—	V_{CC}	V	50 Ohm Termination to V_{CC}
$V_{OL(DO)}$	Output LOW voltage (DO)	V_{CC}-1.20	—	V_{CC}-0.60	V	50 Ohm Termination to V_{CC}
$\Delta V_{OD(DO)}$	Output differential voltage (DO)	550	850	1200	mV	100 Ohm Termination between DO$\pm$ at Load
$V_{CM(DO)}$	Output common mode voltage	2.10	-	3.00	V	100 Ohm Termination between DO$\pm$ at Load
$V_{OH(CO)}$	Output HIGH voltage (CO)	V_{CC}-0.050	—	V_{CC}	V	50 Ohm Termination to V_{CC}
$V_{OL(CO)}$	Output LOW voltage (CO)	V_{CC}-1.20	—	V_{CC}-0.60	V	50 Ohm Termination to V_{CC}
$\Delta V_{OD(CO)}$	Output differential voltage (CO)	500	850	1200	mV	100 Ohm Termination between CO$\pm$ at Load
$V_{CM(CO)}$	Output common mode voltage	2.10	-	3.00	V	100 Ohm Termination between CO$\pm$ at Load
R_O	Back Termination Impedance (DO, CO)	40		60	Ohm	Guaranteed, not tested
V_{IH}	Input HIGH voltage (LVPECL)	1.5	-	V_{CC}-1.0v	V	
V_{IL}	Input LOW voltage (LVPECL)	0	-	-	V	
ΔV_{IN}	Differential Input voltage (LVPECL)	400		1600	mV	
V_{ICM}	Input Common Mode Range (LVPECL)	1.5-$\Delta V_{IN/2}$		VCC-1.0-$\Delta V_{IN/2}$	V	
V_{OH}	Output HIGH voltage (TTL)	2.4			V	I_{OH}=-4.0 mA
V_{OL}	Output LOW voltage (TTL)			0.5	V	I_{OL}=+4.0 mA
V_{IH}	Input HIGH voltage (TTL)	2.0		5.5	V	
V_{IL}	Input LOW voltage (TTL)	0.0		0.8	V	
I_{IH}	Input HIGH Current (TTL)			500	uA	V_{IN}=2.4V
I_{IL}	Input LOW Current (TTL)			-500	uA	V_{IN}=0.5V
V_{CC}	Supply voltage	3.14	—	3.47	V	3.3V$\pm$ 5%
P_D	Power dissipation	—	1.7	2.15	W	Outputs open, V_{CC} = V_{CC} max
I_{CC}	Supply Current	—	495	620	mA	Outputs open, V_{CC} = V_{CC} max

Clock Multiplier Unit

Table 3: VSC8131 CMU Performance

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_J	Output Clock and Data Jitter	—	4	ps.	RMS, tested to SONET specification with 2ps RMS jitter on REFCLK
LBW	PLL Loop Bandwidth		2.0	MHz	-3dB point of jitter transfer curve
$Peak_J$	Jitter Peaking		0.1	dB	REFCLK to DO
	Tuning Range	-100	+100	ppm	

Absolute Maximum Ratings (1)

Power Supply Voltage, (V_{CC}) ..... -0.5V to +3.8V
DC Input Voltage (Differential inputs) ..... -0.5V to V_{CC} +0.5V
DC Input Voltage (TTL inputs) ..... -0.5V to +5.5V
DC Output Voltage (TTL Outputs) ..... -0.5V to V_{CC} + 0.5V
Output Current (TTL Outputs) ..... +/-50mA
Output Current (Differential Outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55^{o} to $+125^{o}$C

Recommended Operating Conditions

Power Supply Voltage, (V_{CC}) ..... +3.3V±5%
Operating Temperature Range ..... 0^{o}C Ambient to $+85^{o}$C Case Temperature

Notes:
(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC8131 is rated to 1500V based on the human body model.

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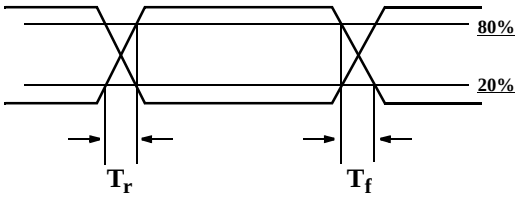
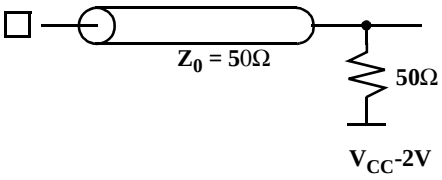
Figure 5: Parametric Measurement Information

TTL Rise and Fall Time



Parametric Test Load Circuit

Serial Output Load



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Package Pin Description

Table 4: Package Pin Identification

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
NC	1	-	-	Leave Unconnected
TEST	2	I	GND	
TEST	3	I	GND	
VCC	4	PWR	+3.3V	
VEE	5	PWR	GND	
VEE	6	PWR	GND	
VEE	7	PWR	GND	
VCC	8	PWR	+3.3V	
CO+	9	O	LVPECL	2.488 GHz Clock, true
CO-	10	O	LVPECL	2.488 GHz Clock, compliment
VCC	11	PWR	+3.3V	
VCC	12	PWR	+3.3V	
NC	13	-	-	Leave Unconnected
NC	14	-	-	Leave Unconnected
VEE	15	PWR	GND	
VEE	16	PWR	GND	
VEE	17	PWR	GND	
VCC	18	PWR	+3.3V	
DO+	19	O	LVPECL	Serialized Data, true
DO-	20	O	LVPECL	Serialized Data, compliment
VCC	21	PWR	+3.3V	
NC	22	-	-	Leave Unconnected
VCC	23	PWR	+3.3V	
VCC	24	PWR	+3.3V	
VCC	25	PWR	+3.3V	
VEE	26	PWR	GND	
VEE	27	PWR	GND	
VEE	28	PWR	GND	
VEE	29	PWR	GND	
VEE	30	PWR	GND	
NC	31	-	-	Leave Unconnected
NC	32	-	-	Leave Unconnected
NC	33	-	-	Leave Unconnected
NC	34	-	-	Leave Unconnected
NC	35	-	-	Leave Unconnected
NC	36	-	-	Leave Unconnected

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Table 4: Package Pin Identification

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
NC	37	-	-	Leave Unconnected
NC	38	-	-	Leave Unconnected
VCC	39	PWR	+3.3V	
VEE	40	PWR	GND	
NC	41	-	-	Leave Unconnected
VEE	42	PWR	GND	
VCC	43	PWR	+3.3V	
NC	44	-	-	Leave Unconnected
NC	45	-	-	Leave Unconnected
NC	46	-	-	Leave Unconnected
NC	47	-	-	Leave Unconnected
NC	48	-	-	Leave Unconnected
LOL	49	O	TTL	CMU loss of lock
VCC	50	PWR	+3.3V	
VEE	51	PWR	GND	
PARERR	52	O	TTL	parity error
CK78OUT	53	O	TTL	divide-by-32 clock out
VCC	54	PWR	+3.3V	
CK78IN	55	I	TTL	divide-by-32 clock in
NC	56	-	-	Leave Unconnected
VEE	57	PWR	GND	
D31	58	I	TTL	parallel data (LSB)
D30	59	I	TTL	parallel data
VCC	60	PWR	+3.3V	
D29	61	I	TTL	parallel data
D28	62	I	TTL	parallel data
NC	63	-	-	Leave Unconnected
VCC	64	PWR	+3.3V	
NC	65	-	-	Leave Unconnected
VCC	66	PWR	+3.3V	
D27	67	I	TTL	parallel data
D26	68	I	TTL	parallel data
VEE	69	PWR	GND	
D25	70	I	TTL	parallel data
D24	71	I	TTL	parallel data
VCC	72	PWR	+3.3V	
D23	73	I	TTL	parallel data

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Table 4: Package Pin Identification

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
D22	74	I	TTL	parallel data
VCC	75	PWR	+3.3V	
D21	76	I	TTL	parallel data
D20	77	I	TTL	parallel data
VEE	78	PWR	GND	
D19	79	I	TTL	parallel data
D18	80	I	TTL	parallel data
VCC	81	PWR	+3.3V	
D17	82	I	TTL	parallel data
D16	83	I	TTL	parallel data
VCC	84	PWR	+3.3V	
D15	85	I	TTL	parallel data
D14	86	I	TTL	parallel data
VEE	87	PWR	GND	
D13	88	I	TTL	parallel data
D12	89	I	TTL	parallel data
VCC	90	PWR	+3.3V	
D11	91	I	TTL	parallel data
D10	92	I	TTL	parallel data
VCC	93	PWR	+3.3V	
D9	94	I	TTL	parallel data
D8	95	I	TTL	parallel data
VEE	96	PWR	GND	
D7	97	I	TTL	parallel data
D6	98	I	TTL	parallel data
VCC	99	PWR	+3.3V	
D5	100	I	TTL	parallel data
D4	101	I	TTL	parallel data
VCC	102	PWR	+3.3V	
VCC	103	PWR	+3.3V	
NC	104	-	-	Leave Unconnected
D3	105	I	TTL	parallel data
D2	106	I	TTL	parallel data
VCC	107	PWR	+3.3V	
D1	108	I	TTL	parallel data
D0	109	I	TTL	parallel data (MSB)
VEE	110	PWR	GND	

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Table 4: Package Pin Identification

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
PARBIT	111	I	TTL	parity bit
PARMODE	112	I	TTL	parity mode select (even vs. odd)
VCC	113	PWR	+3.3V	
TEST	114	I	GND	
NC	115	-	-	Leave Unconnected
REFCLK+	116	I	LVPECL	CMU reference clock, true
REFCLK-	117	I	LVPECL	CMU reference clock, compliment
VCC	118	PWR	+3.3V	
VEE	119	PWR	GND	
TEST	120	O	-	Leave Unconnected
TEST	121	O	-	Leave Unconnected
VEE_ANA	122	PWR	GND	Analog Power for CMU
VCC_ANA	123	PWR	+3.3V	Analog Power for CMU
NC	124	-	-	Leave Unconnected
NC	125	-	-	Leave Unconnected
VEE	126	PWR	GND	
VEE	127	PWR	GND	
VCC	128	PWR	+3.3V	

NC = No Connection. ***These pins must be left floating*** *- do not connect to a supply potential. Connecting any of these pins to a power supply rail may cause improper operation or failure of the device; or in extreme cases, may cause permanent damage to the device.*

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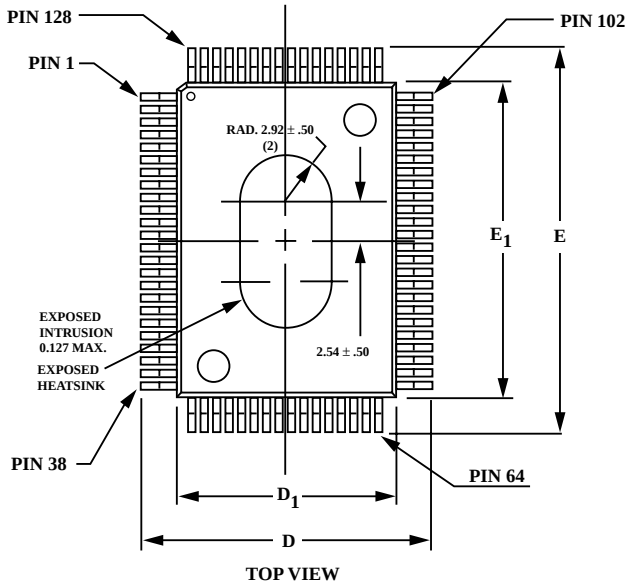
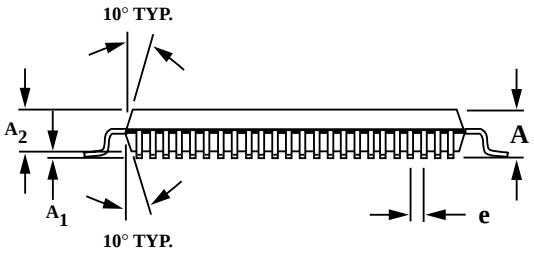
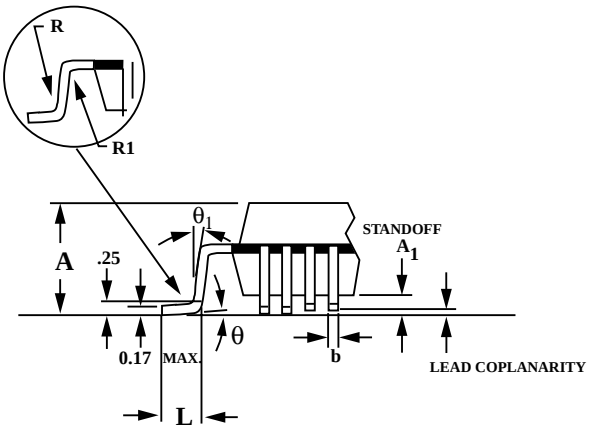
Package Information

Figure 6: 128 PQFP Package Drawing



Key	*mm*	*Tolerance*
A	2.35	MAX
A1	0.25	MAX
A2	2.00	+.10
D	17.20	±.20
D1	14.00	±.10
E	23.20	±.20
E1	20.00	±.10
L	.88	+.15/-.10
e	.50	BASIC
b	.22	±.05
θ	0°-7°	
R	.30	TYP
R1	.20	TYP





Notes: 1) Drawing is not to scale
2) All dimensions in mm
3) Package represented is also used for the 64, 80, & 100 PQFP packages. Pin count drawn does not reflect the 128 Package.

NOTES:

Package #: 101-322-5
Issue #: 2

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Package Thermal Considerations

This package has been enhanced with a copper heat slug to provide a low thermal resistance path from the die to the exposed surface of the heat spreader. The thermal resistance is shown in the following table

Table 5: Thermal Resistance

Symbol	*Description*	*°C/W*
θ_{jc}	Thermal resistance from junction to case.	2.2
θ_{ja}	Thermal resistance from junction to ambient with no airflow, including conduction through the leads.	25.6

Thermal Resistance with Airflow

Shown in the table below is the thermal resistance with airflow. This thermal resistance value reflects all the thermal paths including through the leads in an environment where the leads are exposed. The temperature difference between the ambient airflow temperature and the case temperature should be the worst case power of the device multiplied by the thermal resistance.

Table 6: Thermal Resistance with Airflow

Airflow	θ_{ca} (°C/W)
100 lfpm	19.8
200 lfpm	16.7
400 lfpm	14.6
600 lfpm	13.0

Maximum Ambient Temperature without Heatsink

The worst case ambient temperature without use of a heatsink is given by the equation:

$$T_{A(MAX)} = T_{C(MAX)} - P_{(MAX)}\theta_{CA}$$

where:

$T_{A(MAX)}$ Ambient Air temperature
$T_{C(MAX)}$ Case temperature (85°C for VSC8131)
$P_{(MAX)}$ Power (2.15W for VSC8131)
θ_{CA} Theta case to ambient at appropriate airflow

The results of this calculation are listed below:

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Table 7: Maximum Ambient Air Temperature without Heatsink

Airflow	Max Ambient Temp ^{0}C
none	33.2
100 lfpm	42.4
200 lfpm	49.1
400 lfpm	53.6
600 lfpm	57.1

Note that ambient air temperature varies throughout the system based on the positioning and magnitude of heat sources and the direction of air flow.

Notice

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Warning

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