Target Specification

VSC8124

2.488 Gb/s Quad Data Re-timer

Features

- Four Channel 2.488 Gb/s Data Recovery
- SONET Quality Jitter Tolerance
- Fastlock Data Acquisition less than 200 Bit Times
- Loss of Signal Indicators
- Long Strings of Static Data Tolerated by the Clock Recovery Circuit without Loss of Signal
- First Order Clock Recovery Loop Minimizes Jitter Accumulation
- Differential on Chip Terminated Serial Data I/O
- Bypass for OC3, OC12 Data Rates
- 155.52 MHz Reference Clock Frequency
- 3.3V Supply Operation
- 14 x 14mm, 100 Pin Thermally Enhanced TQFP Package

General Description

The VSC8124 is a four channel, 2.5 Gb/s data re-timer for cleaning up data downstream of optical links or cross point switches. Serial data at the 2.5 Gb/s rate is independently re-timed on four channels, and driven differentially by CML drivers. The re-timing function on each channel can be individually bypassed for lower rate signals or test purposes. The VSC8124 provides four independent loss of signal indicators in the event of loss of synchronous data transitions.

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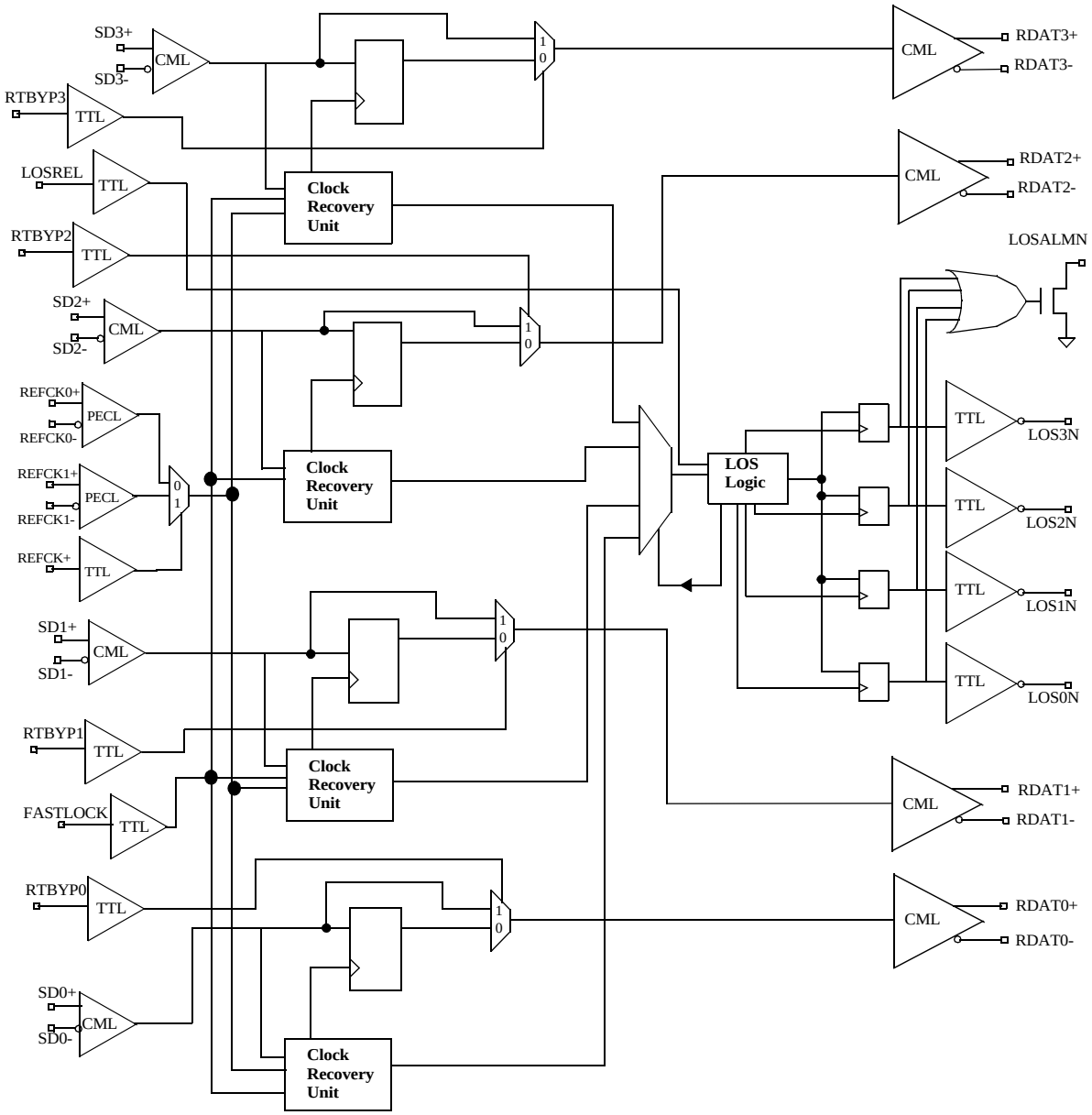
VSC8124 Block Diagram



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Functional Description

Reference Clock

A clean reference clock should be provided to meet jitter specifications. An arbitrary discontinuity in reference clock phase can be tolerated without data error at slightly reduced jitter tolerance. (See Table 1) Phase changes must not occur more often than every 20 µs. Serial data transition density must average ≥ 0.5 for that period. Two reference clock input ports are provided. The REFSEL pin selects the active port. When REFSEL is not driven, it floats low, selecting REFCK0. Changing REFSEL implies a phase change.

Clock Recovery

The incoming serial data on each channel is presented to a clock recovery and data re-timing circuit. For each channel, a phase detector and low pass filter force a local clock to track the average phase of the incoming serial data. The low pass filter is first order to prevent jitter peaking in cascaded devices.

Figure 1: Serial Input Data Eye Diagram

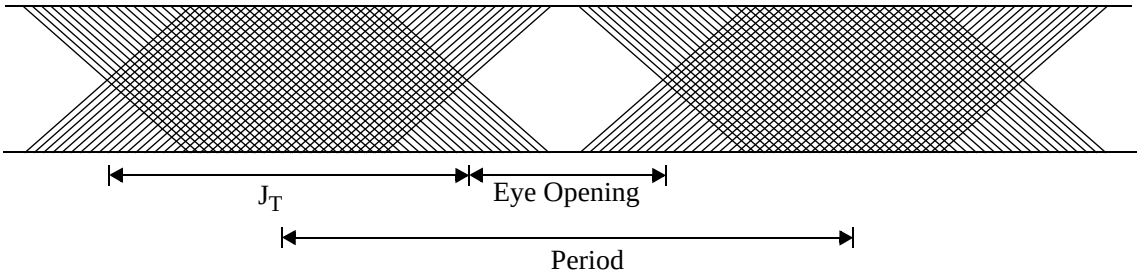

Table 1: Serial Input Data Specification

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
J_T	Jitter tolerance	220	-	-	ps	Normal Operation
J_T	Jitter tolerance	150	170	-	ps	Fast Lock Mode
J_T	Jitter tolerance	190	210	-	ps	Within 20µs after REFCLK phase change
Period		-	401.88	-	ps	

NOTE: 1) Jitter tolerance is measured at worst case power supply and temperature, using 155.52 MHz clean reference clock (REFCK to meet 2.0 ps RMS jitter at less than 10 Mhz in bandwidth), and 600mV swing differential PRBS data with150ps maximum rise time.

2) Jitter tolerance and re-timed data jitter are degraded in FASTLOCK mode.

3) Reference clock frequency tolerance: $\Delta f <= 100$ ppm

4) Jitter tolerance specifications do not apply in re-timer bypass mode.

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Figure 2: Re-timed Serial Output Data Eye Diagram

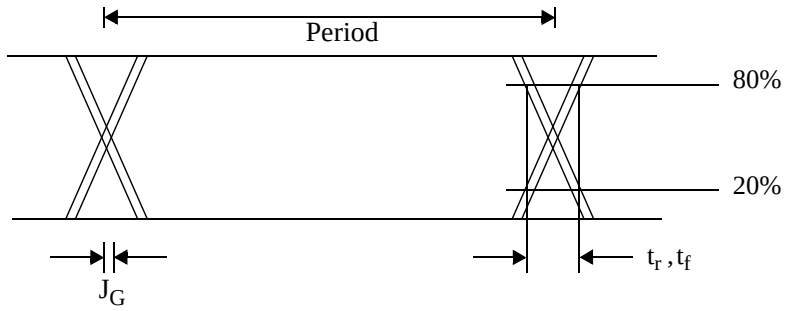

Table 2: Serial Output Data Specification

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
J_G	Jitter generation	-	-	12ps rms		Normal Operation
J_G	Jitter generation	-	-	15 ps rms		Fast Lock Mode
J_G	Jitter generation	-	-	14ps rms		Within 40 µs after REFCK phase change
t_r, t_f	Rise time, fall time	-	-	140	ps	20 to 80%

NOTES: 1) Jitter generation is measured at worst case power supply and temperature using 155.52 MHz clean reference clock and clean serial data.

2) Jitter generation and rise, fall time specifications do not apply in re-timer bypass mode.

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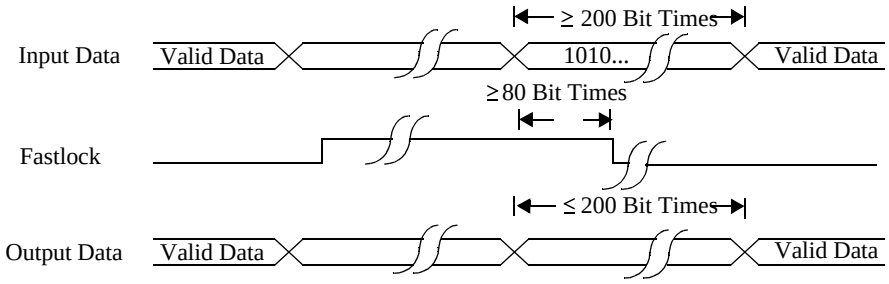
Figure 3: Fastlock Timing Diagram



Fast Lock

The VSC8124 supports a fastlock clock recovery mode which enables the clock recovery unit to lock the retiming clock to the incoming data within 80 bit periods of initiation. As a requirement for the operation of the fastlock function, the driving system must send a 0101 bit pattern while the fastlock pin is at a high logic level. The FASTLOCK function is active simultaneously on all four data channels The fastlock pin has a TTL input receiver meeting the specifications contained in Table 7. Note that jitter tolerance and re-timed data jitter are degraded in FASTLOCK mode.

Loss of Signal

The loss of signal (LOS) circuitry is shared among four serial data channels, sampling the signal condition on each channel sequentially. There is a loss of signal latch and active low indicator pin (LOS[0:3]N) for each channel. In addition, there is an alarm pin (LOSALMN) which indicates the OR of the latched states of the four channel indicators. The alarm pin uses an open drain output, so the alarm pins from multiple parts can be wired together. A weak external pull resistor (approximately 1k Ohm) must be provided to utilize the wired NOR alarm function. To facilitate system troubleshooting, the LOS latches can only be cleared by the active high LOSCLR input.

The loss of signal clear (LOSCLR) input will cause all four loss of signal indicators LOS[0:3]N and the loss of signal alarm (LOSALM) to be cleared. The LOSCLR input is asynchronous. It must be held active for at least two reference clock cycles. A channel found to be missing after the error latch has been cleared, will again set its error latch and the LOSALMN.

The LOS circuit examines a selected clock recovery channel for expected data transition activity. Expected data activity includes pseudo-random data at a baud rate 16 times the reference clock frequency, and data including at least 8500 consecutive bits of a 101010... pattern. The detector will allow the OC-48 framing pattern to pass without triggering LOS. The LOS detector is disabled when FASTLOCK mode is active.

To assist diagnostic procedures, the effect of individual loss of signal indicators in the loss of signal alarm can be masked. This is controlled by the MASK[0:3] pins. Each of those pins, when pulled high, disables the effect of its respective channel on the loss of signal alarm (LOSALM). If all MASK pins are pulled high, the LOSALM signal will not pull down. The loss of signal indicators for individual channels are not affected by the MASK pins.

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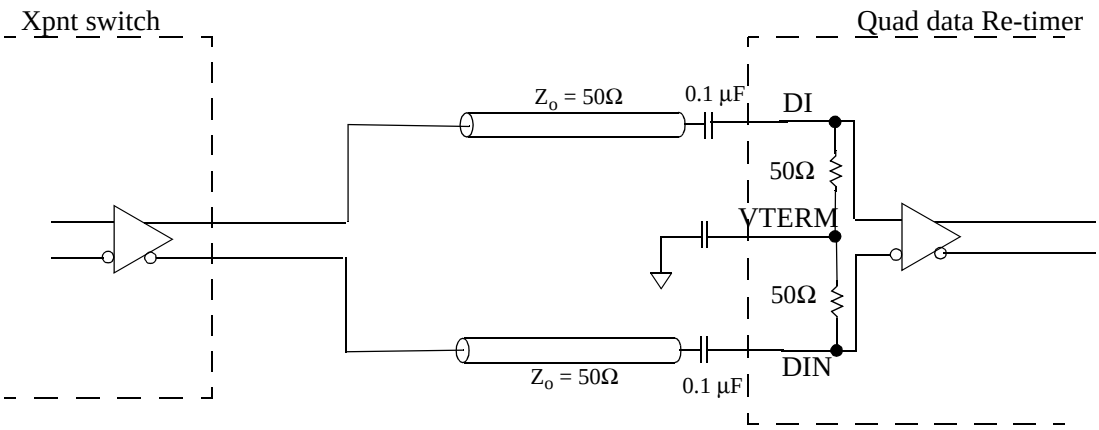
Re-timer Bypass

The serial data re-timer can be individually bypassed for data channels. This allows asynchronous data signals to pass through the part. The bypass function is controlled by the RTBYP[0:3] pins.

High Speed Interfaces

Figure 4: High Speed Data Input Termination- AC Coupled



Notes:

1)It is recommended that VTERM pins from multiple inputs NOT be tied together, unless driven from a low impedance supply.

2) The high speed data receivers have self biased inputs.

3) For unused serial data receivers, it is recommended to tie one side low by connecting a 1k Ohm resistor to V_{ee} and letting the other side float.

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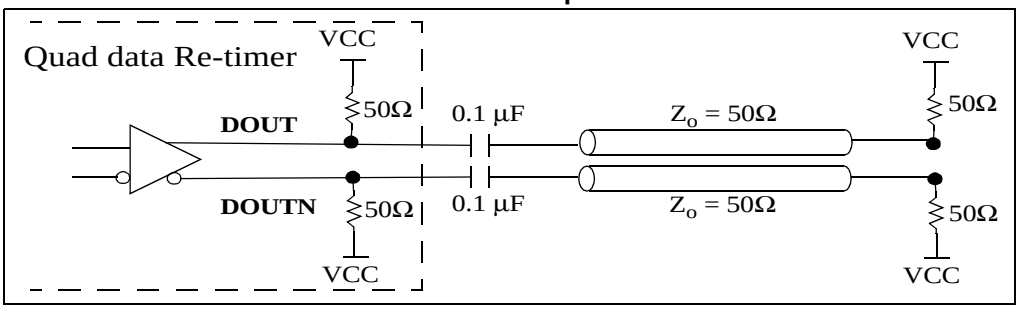
Figure 5: High Speed Data Output Termination - AC Coupled

AC Coupled



DC Coupled

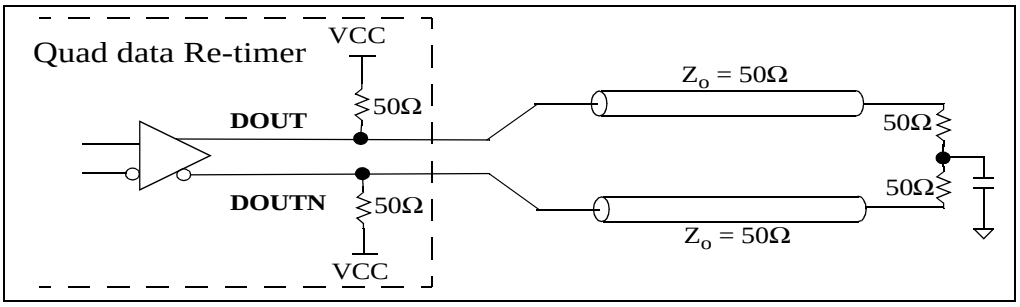
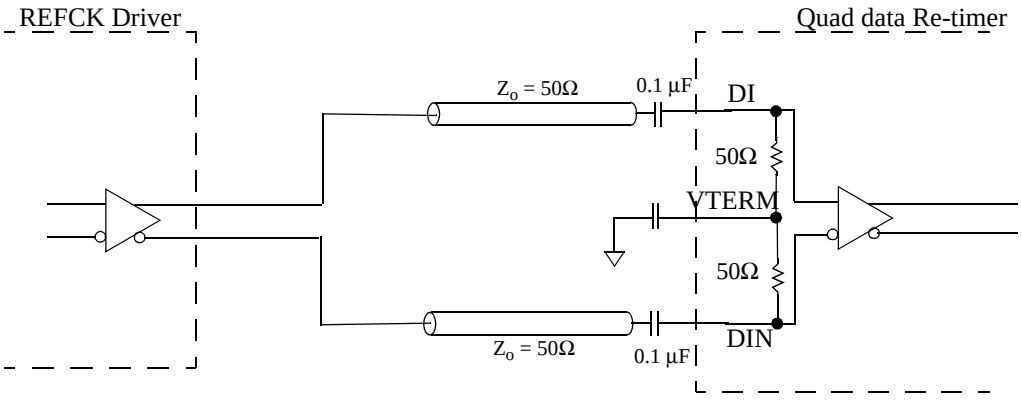


Figure 6: REFCK Input Termination - AC Coupled



Notes:

1) It is recommended that the VTERM pins from multiple inputs NOT be tied together, unless driven from a low impedance supply.

2) The reference clock receivers have self-biased inputs.

3) For unused reference clock receivers, it is recommended to tie one side low by connecting a 1k Ohm resistor to V_{ee}, and letting the other side float.

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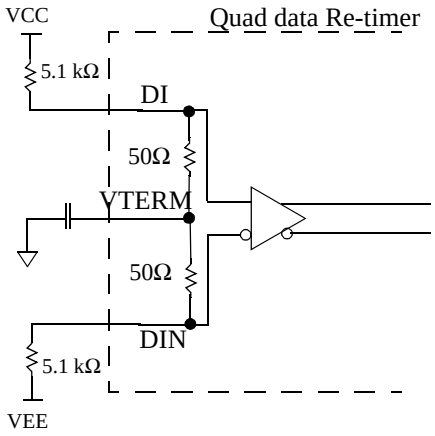
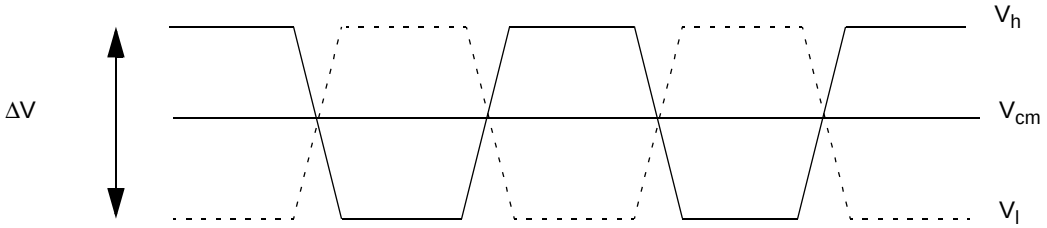
Figure 7: Unused High Speed and REFCK Input Termination.



High Speed Specifications

Figure 8: Definition of I/O Levels



NOTE: Diagram applies to all I/O swing specifications

Table 3: High Speed Driver Specification

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
$\Delta V=(V_h - V_l)$	Single ended peak-to-peak	600	-	1000	mV	Terminated as in Fig. 5 (DC Coupled)
V_{CM}	Output common mode	1.8V	-	2.2	V	Terminated as in Fig.5 (DC Coupled)
Z_{OUT}	Ouput impedance	40	50	60	Ω	Measured Single-ended

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Table 4: AC Coupled High Speed Receiver Specifications

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
$\Delta V=V_h-V_l$	Input swing(1)	200	-	1200	mV	
Z_{in}	Differential input impedance	80	-	120	Ω	

NOTE: 1) See Figure 8

Table 5: DC Coupled High Speed Receiver Specifications

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{cm}	Input common mode	-	0.43VCC	-	V	
V_{ih}	Input high level	VEE+0.9	-	VCC-1.0	V	
V_{il}	Input low level	VEE	-	VCC-1.2	V	
$\Delta V=V_h-V_l$	Input swing	200	-	1200	mV	

Table 6: REFCK Receiver Specifications

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
$\Delta V=V_h-V_l$	Input swing(1)	400	-	1300	mV	
V_{cm}	Input common mode	1.27	-	1.49	V	
Z_{in}	Differential input impedance	80	-	120	Ω	

NOTE: 1) See Figure 8

Table 7: TTL Input (internal pull-down) Receiver Specifications

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{ih}	Input high level	2000	-	-	mV	
V_{il}	Input low level	-	-	800	mV	
I_{ilh}	Input leakage current high	-	-	1	mA	V_{in} = 3.3V
I_{ill}	Input leakage current low	-	-	1	mA	V_{in} = 0V

Table 8: TTL Output Driver Specifications

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{oh}	Output high level	2400	-	-	mV	
V_{ol}	Output low level	-	-	400	mV	

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Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
t_r	Rise Time	-	-	5	ns	10 to 90% 10pF load
t_f	Fall Time	-	-	5	ns	10 to 90% 10pF load
I_{olh}	Output leakage current high	-	-	2	mA	V_{out} = 2.0V, tri-state enabled
I_{oll}	Output leakage current low	-	-	4	mA	V_{out} = 0.8V, tri-state enabled
t_{oez}	Tristate enabled to high Z	-	-	10	ns	

Table 9: Power Supply Specifications

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
Power supply voltage		3.15	3.30	3.46	V	
Power dissipation		-	2.7	3.25	W	

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Absolute Maximum Ratings

Power Supply Voltage, (V_{CC}) .....-0.5 V to +4.0 V
DC Input Voltage (Differential inputs) .....-0.5 V to V_{CC} + 0.5V
DC Input Voltage (TTL inputs)..... -0.5 V to V_{CC} + 0.5 V
DC Output Voltage (TTL outputs .....-0.5 V to V_{CC} + 0.5V
Output Current (TTL outputs).....+/- 50mA
Output Current (Differential outputs).....+/- 50mA
Case Temperature Under Bias.....-55^{o} to + 100^{o}C

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltages (V_{CC})..... +3.3V ±5 %

Operating Case Temperature Range (T)..... 0^{o} to 85^{o}C

Notes: (1) Customer may require cooled/heatsink environment to meet thermal requirements of 100TQFP.
(2) Contact factory for package thermal performance information.
(3) θ_{JC} = 6^{o}C/W

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC8124 is rated to the following ESD voltages based on the human body model:

1. High speed pins are rated ≥ 200V
2. All other pins are rated at or above 1500V.

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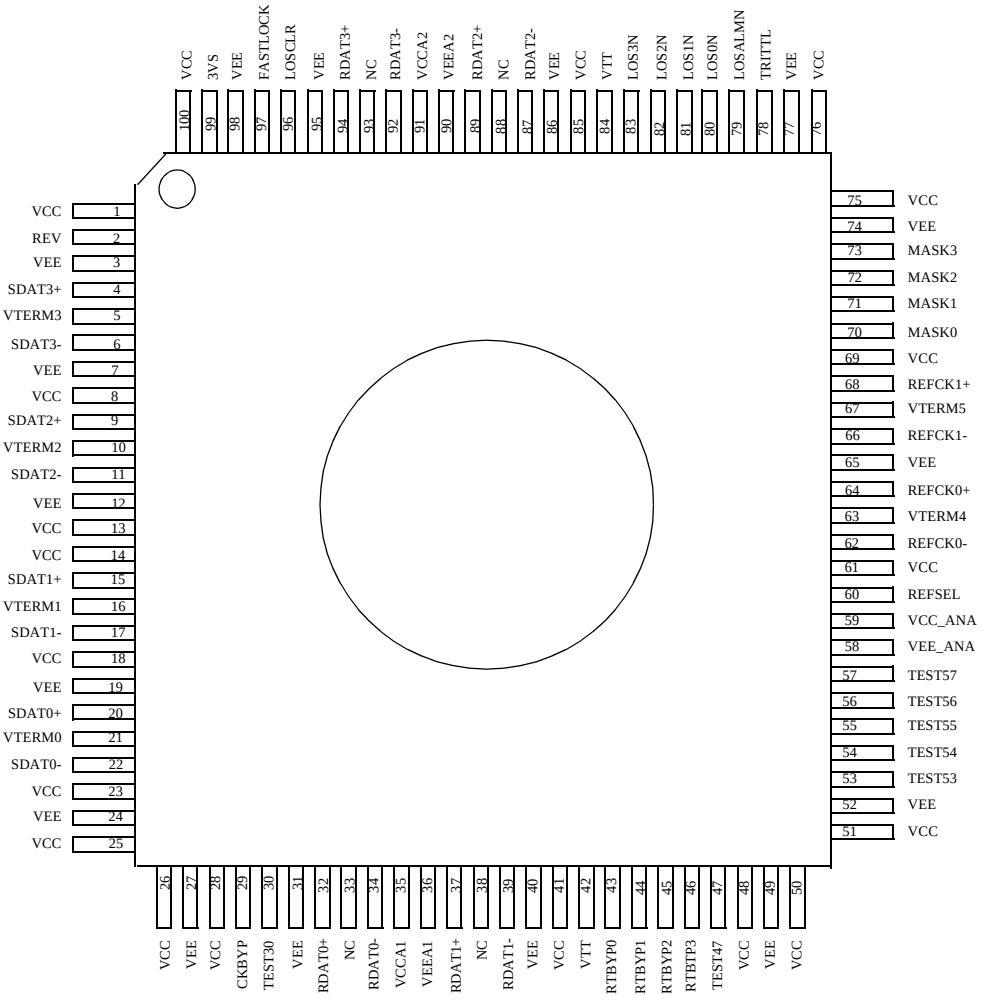
Package Pin Descriptions

Figure 9: Package Pin Diagram

VSC8124
2.488 Gb/s Re-timer



Drawing is heat sink up
Cavity Down Package
100 Pin TQFP
14x14x1.4 mm
BODY + 2.0mm footprint

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Table 10: Package Pin Identification

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
VCC	1	PWR	+3.3V	
REV	2	O	ANALOG	Do not connect
VEE	3	PWR	GND	
SDAT3+	4	I	CML	High speed data input
VTERM3 [1]	5	PWR	VTERM	
SDAT3-	6	I	CML	High speed data input
VEE	7	PWR	GND	
VCC	8	PWR	+3.3V	
SDAT2+	9	I	CML	High speed data input
VTERM2 [1]	10	PWR	VTERM	
SDAT2-	11	I	CML	High speed data input
VEE	12	PWR	GND	
VCC	13	PWR	+3.3V	
VCC	14	PWR	+3.3V	
SDAT1+	15	I	CML	High speed data input
VTERM1 [1]	16	PWR	VTERM	
SDAT1-	17	I	CML	High speed data input
VCC	18	PWR	+3.3V	
VEE	19	PWR	GND	
SDAT0+	20	I	CML	High speed data input
VTERM0 [1]	21	PWR	VTERM	
SDAT0-	22	I	CML	High speed data input
VCC	23	PWR	+3.3V	
VEE	24	PWR	GND	
VCC	25	PWR	+3.3V	
VCC	26	PWR	+3.3V	
VEE	27	PWR	GND	
VCC	28	PWR	+3.3V	
TEST29	29	I	TTL	Do not connect
TEST30	30	I	TTL	Do not connect
VEE	31	PWR	GND	
RDAT0+	32	O	CML	Retimed data output
NC	33	-	NC	
RDAT0-	34	O	CML	Retimed data output
VCCA1 [2]	35	PWR	+3.3V	
VEEA1 [2]	36	PWR	GND	
RDAT1+	37	O	CML	Retimed data output

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Table 10: Package Pin Identification

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
NC	38	-	NC	
RDAT1-	39	O	CML	Retimed data output
VEE	40	PWR	GND	
VCC	41	PWR	+3.3V	
VTT	42	PWR	+1.3V	Do not connect
RTBYP0	43	I	TTL	Re-timer bypass
RTBYP1	44	I	TTL	Re-timer bypass
RTBYP2	45	I	TTL	Re-timer bypass
RTBYP3	46	I	TTL	Re-timer bypass
TEST47	47	I	TTL	Do not connect
VCC	48	PWR	+3.3V	
VEE	49	PWR	GND	
VCC	50	PWR	+3.3V	
VCC	51	PWR	+3.3V	
VEE	52	PWR	GND	
TEST53	53	I	-	Do not connect
TEST54	54	I	-	Do not connect
TEST55	55	I	-	Do not connect
TEST56	56	I	-	Do not connect
TEST57	57	I	-	Do not connect
VEE_ANA	58	PWR	GND	
VCC_ANA	59	PWR	+3.3V	
REFSEL	60	I	TTL	Reference clock select
VCC	61	PWR	+3.3V	
REFCK0-	62	I	LVPECL	155 MHz ref. clock
VTERM4 [1]	63	PWR	VTERM	
REFCK0+	64	I	LVPECL	155 MHz ref. clock
VEE	65	PWR	GND	
REFCK1-	66	I	LVPECL	Alternate ref. clock

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Table 10: Package Pin Identification

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
VTERM5 [1]	67	PWR	VTERM	
REFCK1+	68	I	LVPECL	Alternate ref. clock
VCC	69	PWR	+3.3V	
MASK0	70	I	TTL	LOS mask enable
MASK1	71	I	TTL	LOS mask enable
MASK2	72	I	TTL	LOS mask enable
MASK3	73	I	TTL	LOS mask enable
VEE	74	PWR	GND	
VCC	75	PWR	+3.3V	
VCC	76	PWR	+3.3V	
VEE	77	PWR	GND	
TRITTL	78	I	TTL	Tri-state enable
LOSALMN	79	O	Open Drain	Loss of signal alarm
LOS0N	80	O	TTL	Loss of signal indicator
LOS1N	81	O	TTL	Loss of signal indicator
LOS2N	82	O	TTL	Loss of signal indicator
LOS3N	83	O	TTL	Loss of signal indicator
VTT	84	PWR	+1.3V	Do not connect
VCC	85	PWR	+3.3V	
VEE	86	PWR	GND	
RDAT2-	87	O	CML	Retimed data output
NC	88	-	NC	
RDAT2+	89	O	CML	Retimed data output
VEEA2 [2]	90	PWR	GND	
VCCA2 [2]	91	PWR	+3.3V	
RDAT3-	92	O	CML	Retimed data output
NC	93	-	NC	
RDAT3+	94	O	CML	Retimed data output
VEE	95	PWR	GND	
LOSCLR	96	I	TTL	LOS clear
FASTLOCK	97	I	TTL	Fast lock enable
VEE	98	PWR	GND	
3VS	99	PWR	-	Do not connect
VCC	100	PWR	+3.3V	

[1] All pins indicated with superscript (1), while having different names, use the same voltage, but are isolated in the part for noise immunity.

[2] All pins indicated with superscript (2), while having different names, use the same voltage, but are isolated in the part for noise immunity.

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Table 11: Power Supply Pin Summary

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
VCC	1,8,13,14,18,23, 25,26,28,41,48,50, 51,62,70,75,76,85, 100	PWR	+3.3V	
VEE	3,7,12,19,24,27, 31,40,49,52,65, 74,77,86,95,98	PWR	GND	
VTT	42,84	PWR	+1.3V	
VCCA1	35	PWR	+3.3V	dirty VCC for RDAT[0:1]
VCCA2	91	PWR	+3.3V	dirty VCC for RDAT[2:3]
VEEA1	36	PWR	GND	dirty VEE for RDAT[0:1]
VEEA2	90	PWR	GND	dirty VEE for RDAT[2:3]
VCC_ANA	59	PWR	+3.3V	clean VCC for VCO/CMU
VEE_ANA	58	PWR	GND	clean VEE for VCO/CMU
VTERM[0:5]	5,10,16,21,64,68, 72	PWR	VCC/2	

All supplies which reference the same voltage may be connected to the same power supply plane. The VCCANA and VEEANA are noise sensitive supplies, while the VCCA1, VCCA2, VEEA1 and VEEA2 are noise generating supplies. Appropriate power supply noise suppression should be applied to optimize the performance of the device.

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Typical Application

This table lists the suggested connections for non-data path pins for a typical 2.5 Gb/s application which does not use the fast locking, channel re-timer bypassing, or loss of signal alarm masking. Users of those features should take care to understand the functions before connecting to the control pins.

Table 12: Recommended Pin Usage

Pin Number	*Pin Name*	*Recommended Hook-up*
2	REV	Do not connect
29	CKBYP	Do not connect
30	TEST30	Do not connect
42	VTT	Internally generated power supply; Do not connect
43	RTBYP0	Re-timer bypass; Do not connect
44	RTBYP1	Re-timer bypass; Do not connect
45	RTBYP2	Re-timer bypass; Do not connect
46	RTBYP3	Re-timer bypass; Do not connect
47	TEST47	Do not connect
53	TEST53	Do not connect
54	TEST54	Do not connect
55	TEST55	Do not connect
56	TEST56	Do not connect
57	TEST57	Do not connect
60	REFSEL	Reference clock select; to use REFCK0, do not connect
62	REFCK0-	Reference clock 0-; Connect your reference clock true here
64	REFCK0+	Reference clock 0+; Connect your reference clock complement here
66	REFCK1-	Reference clock 1-; 1k Ohm to Vee
68	REFCK1+	Reference clock 1+; Do not connect
70	MASK0	Mask alarm; Do not connect
71	MASK1	Mask alarm; Do not connect
72	MASK2	Mask alarm; Do not connect
73	MASK3	Mask alarm; Do not connect
78	TRITTL	Tri-state TTL outputs; Do not connect
79	LOSALMN	Loss of signal alarm; if used, 1k Ohm to Vcc otherwise do not connect
80	LOS0N	Loss of signal channel 0; connect to CMOS input
81	LOS1N	Loss of signal channel 0; connect to CMOS input
82	LOS2N	Loss of signal channel 0; connect to CMOS input
83	LOS3N	Loss of signal channel 0; connect to CMOS input
84	VTT	Internally generated power supply; Do not connect
96	LOSCLR	Loss of signal clear; CMOS input (3.3V max.)
97	FASTLOCK	Enable fast lock; Do not connect
99	3VS	Power supply sense; Vcc or do not connect

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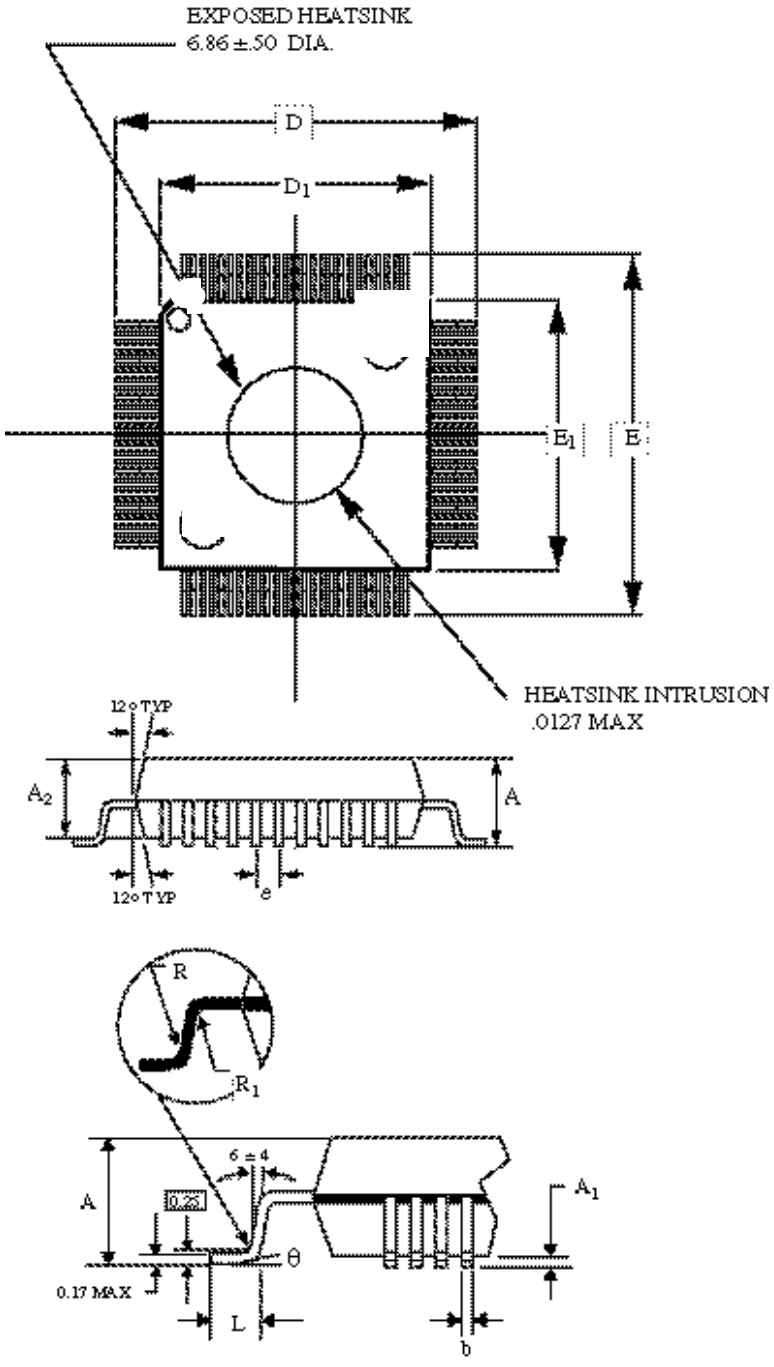
Package Information

100 TQFP Package Drawings



Key	*mm*	*Tolerance*
A	1.6	MAX
A1	0.15	MAX
A2	1.4	±.05
D	16.00	±.20
D1	14.00	±.05
E	16.00	±.20
E1	14.00	±.05
L	.60	+.15/-.10
e	.50	BASIC
b	.22	±.05
q	0°-7°	
R	.20	TYP
R1	.20	TYP

NOTES:
(1) Drawings not to scale.
(2) All units in millimeters unless otherwise noted

Package #: 101-318-3
Issue #: 1

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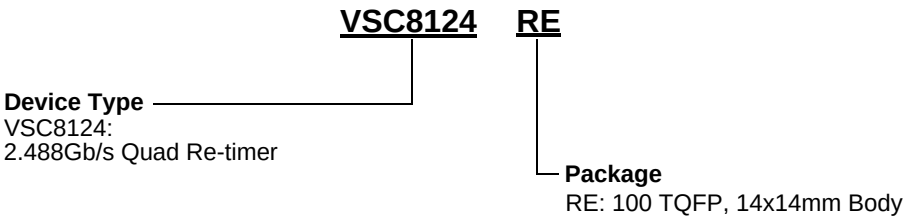
Ordering Information

The order number for this product is formed by a combination of the device number, and package type.



Notice

This document contains information about a proposed product during its design phase of development and is subject to change without notice at any time. All features and specifications are design goals only. Please contact Vitesse Semiconductor to obtain the latest product status and most recent versions of this specification.

Warning

Vitesse Semiconductor Corporation's products are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent is prohibited.

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