reliminary Datasheet

SC8164

2.488 Gbit/sec to 2.7Gbit/sec
1:16 SONET/SDH Demux

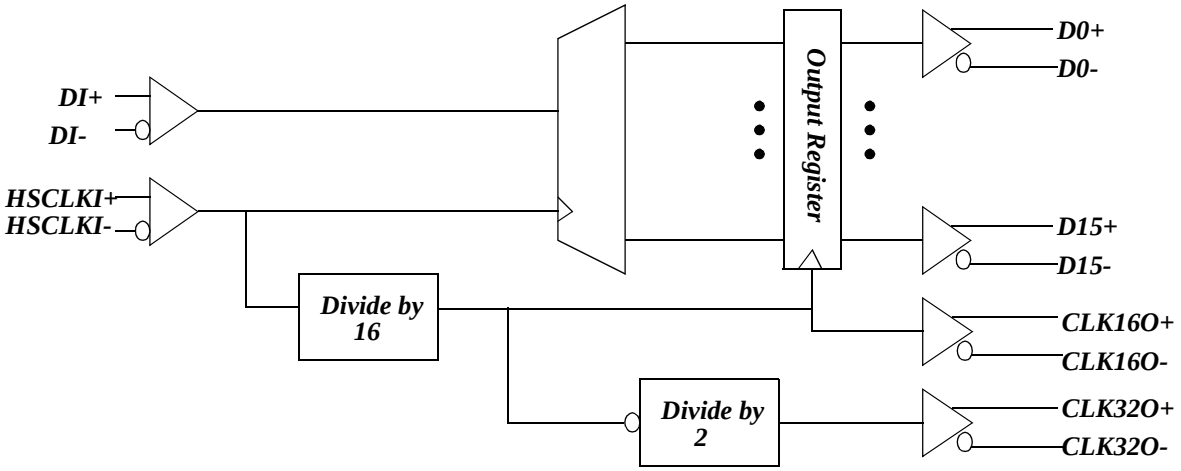
Features

- 2.488Gb/s 1:16 Demultiplexer
- Targeted for SONET OC-48 / SDH STM-16 Applications
- Supports FEC rates up to 2.7Gb/s
- Differential LVPECL Low Speed Interface
- Single +3.3V Supply
- 128 Pin 14x20mm PQFP Package

General Description

The VSC8164 is a 1:16 demultiplexer for use in SONET/SDH systems operating at a standard 2.488Gb/s data rate or forward error correction (FEC) data rate up to 2.7Gb/s. The device operates using a single 3.3V power supply, and is packaged in a thermally enhanced plastic package. The thermal performance of the 128PQFP allows the use of the VSC8164 without a heat sink under most thermal conditions.

VSC8164 Block Diagram



Functional Description

Low Speed Interface

The demultiplexed serial stream is made available by a 16 bit differential LVPECL interface D[15:0] with accompanying differential LVPECL divide by 16 clock CLK16O± and divide by 32 clock CLK32O±. The low speed LVPECL output drivers are designed to drive a 50Ω transmission line. The transmission line can be DC terminated with a split end termination scheme (see Figure 1), or DC terminated by 50Ω to V_{CC}-2V on each line (see Figure 2). At any time, the equivalent split-end termination technique can be substituted for the traditional 50Ω to V_{CC}-2V on each line. AC coupling can be achieved by a number of methods. Figure 3 illustrates an AC coupling method for the occasion when the downstream device provides the bias point for AC coupling. If the downstream device were to have internal termination, the line to line 100Ω resistor may not be necessary. The divide by 32 output can be used to provide a reference clock for the clock multiplication unit on the VSC8163.

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Figure 1: Split-end DC Termination of Low Speed LVPECL CLK16O, CLK32O, D[15:0] Outputs

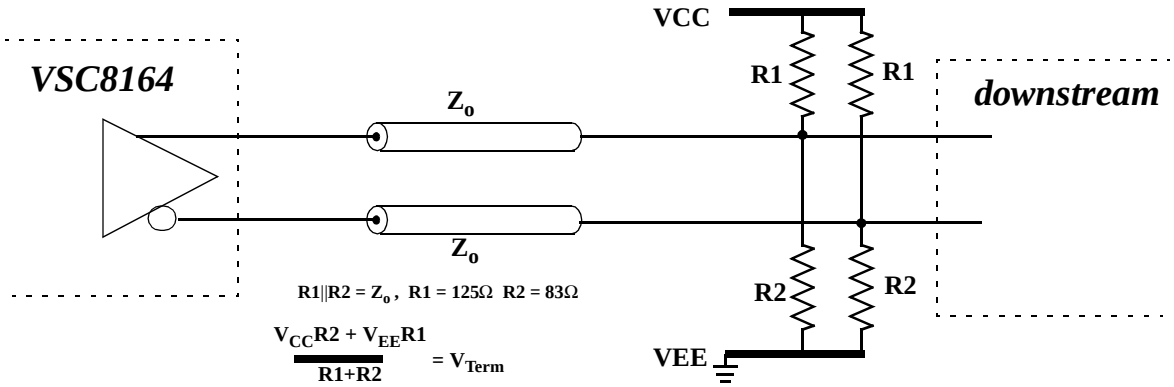


Figure 2: Traditional DC Termination of Low Speed LVPECL CLK16O, CLK32O, D[15:0] Outputs

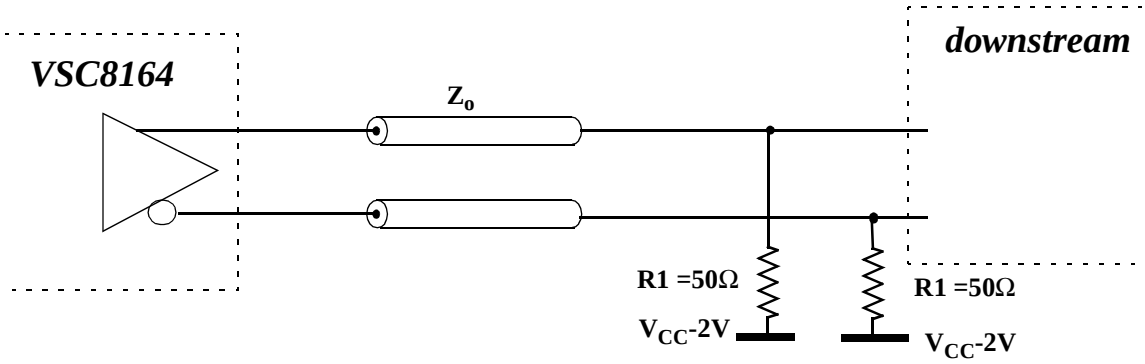
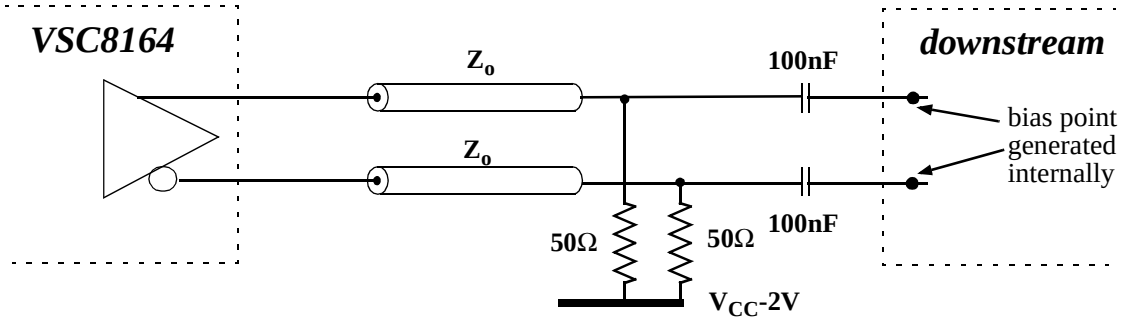


Figure 3: AC Termination of Low Speed LVPECL CLK16O, CLK32O, D[15:0] Outputs



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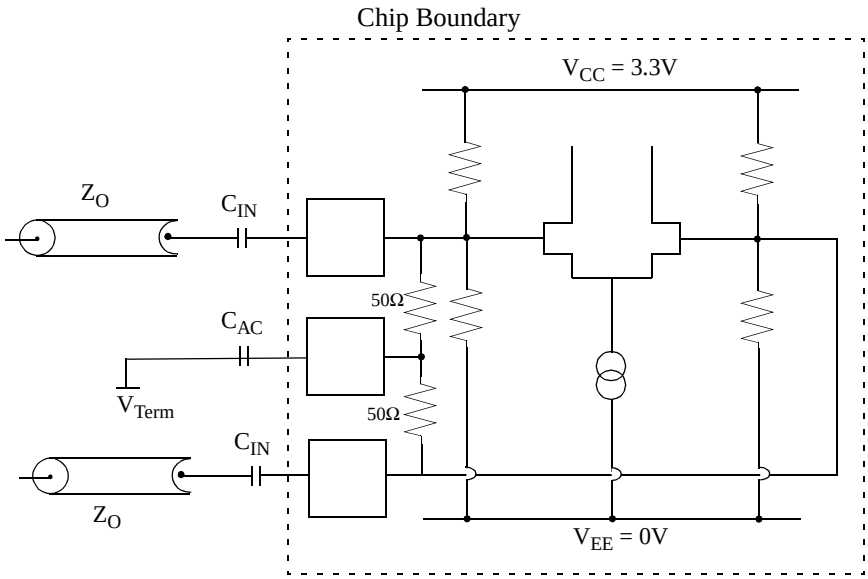
High Speed Interface

The incoming 2.488Gb/s data (up to 2.7Gb/s for FEC applications) and input clock are received by high speed inputs DI and HSCLKI. The data and clock inputs are internally terminated by a center-tapped resistor network. For differential input DC coupling, the network is terminated to the appropriate termination voltage V_{Term} (pins HSDREF, HSCLKREF) providing a 50Ω to V_{Term} termination for both true and complement inputs. For differential input AC coupling, the network is terminated to V_{Term} via a blocking capacitor.

In most situations these inputs will have high transition density and little DC offset. However, in cases where this does not hold, direct DC connection is possible. All serial data and clock inputs have the same circuit topology, as shown in Figure 4. The reference voltage is created by a resistor divider as shown. If the input signal is driven differentially and DC-coupled to the part, the mid-point of the input signal swing should be centered about this reference voltage and not exceed the maximum allowable amplitude (ΔV_{CMI}, ΔV_{IHSDC}). For single-ended, DC-coupling operations, it is recommended that the user provides an external reference voltage which has better temperature and power supply noise rejection than the on-chip resistor divider. The external reference should have a nominal value equivalent to the common mode switch point of the DC coupled signal, and can be connected to either side of the differential gate.

Figure 4: High Speed Serial Clock and Data Inputs



C_{IN} TYP = 100 nF

C_{AC} TYP = 100 nF

Supplies

This device is specified as a LVPECL device with a single positive 3.3V supply. Should the user desire to use the device in a ECL environment with a negative 3.3V supply, then VCC will be ground and VEE will be -3.3V.

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Decoupling of the power supplies is a critical element in maintaining the proper operation of the part. It is recommended that the V_{CC} power supply be decoupled using a 0.1µF and 0.01µF capacitor placed in parallel on each V_{CC} power supply pin as close to the package as possible. If room permits, a 0.001µF capacitor should also be placed in parallel with the 0.1µF and 0.01µF capacitors mentioned above. Recommended capacitors are low inductance ceramic SMT X7R devices. For the 0.1µF capacitor, a 0603 package should be used. The 0.01µF and 0.001µF capacitors can be either 0603 or 0402 packages.

For low frequency decoupling, 47µF tantalum low inductance SMT caps should be sprinkled over the board's main +3.3V power supply and placed close to the C-L-C pi filter.

If the device is being used in an ECL environment with a -3.3V supply, then all references to decoupling V_{CC} must be changed to V_{EE}, and all references to decoupling 3.3V must be changed to -3.3V.

AC Characteristics

Figure 5: AC Timing Waveforms

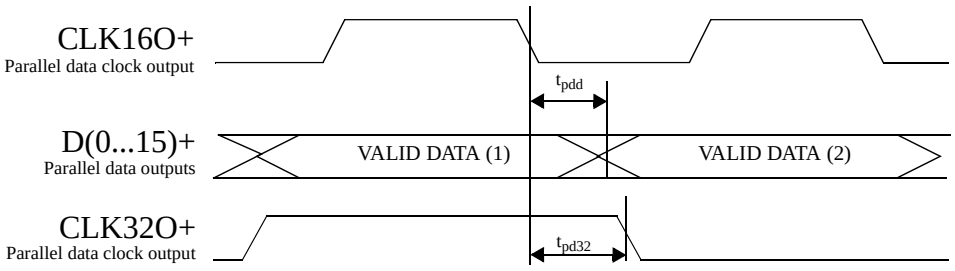

Figure 6: High Speed Input Timing

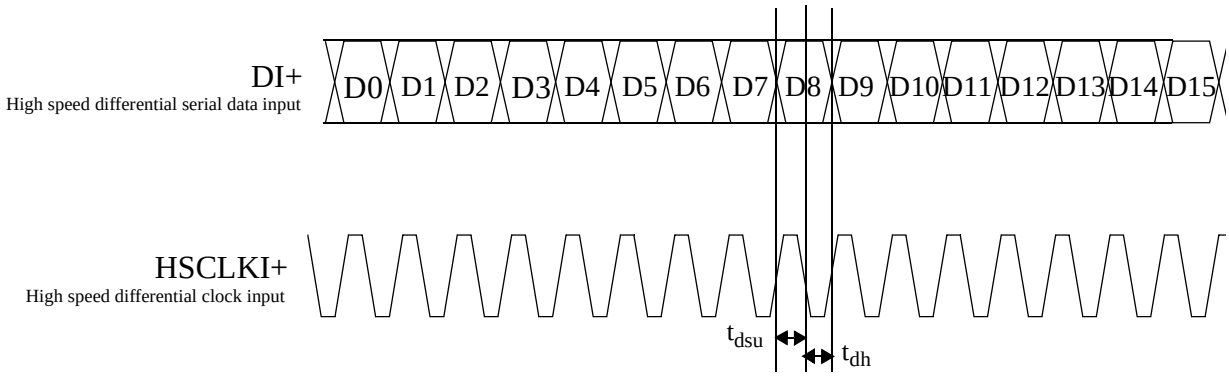

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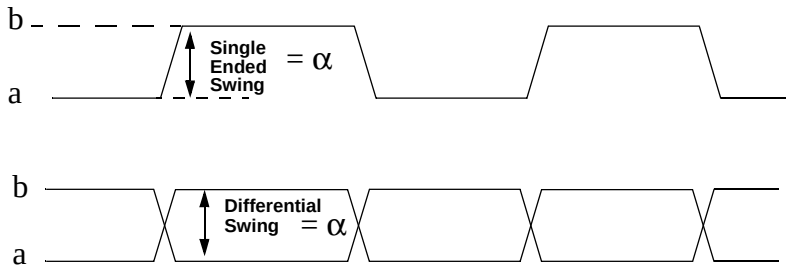
Figure 7: Differential and Single Ended Input and Output Voltage Measurement



* Differential swing (α) is specified as | b - a | (or | a - b |), as is the single ended swing. Differential swing is specified as equal in magnitude to single ended swing.

Table 1: AC Characteristics

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
t_{pdd}	Data valid from falling edge of CLK16O+	0	800	ps.	
t_{pd32}	CLK32O transition from falling edge of CLK16O+	0	1.0	ns.	
t_{DR}, t_{DF}	D[15:0]+/- rise and fall times	—	400	ps	20% to 80% into 50 Ohm load. See Figure 7
t_{CLKR}, t_{CLKF}	CLK16O+/- rise and fall times	—	250	ps	20% to 80% into 50 Ohm load. See Figure 7
$CLK16O_D$	CLK16O+/- duty cycle distortion	45	55	% of clock cycle	High speed clock input at 2.488GHz
t_{dsu}	DI+ setup time with respect to falling edge of HSCLKI+	100	—	ps	
t_{dh}	DI+ hold time with respect to falling edge of HSCLKI+	75	—	ps	
$HSCLKI_D$	HSCLKI+/- duty cycle distortion	40	60	% of clock cycle	

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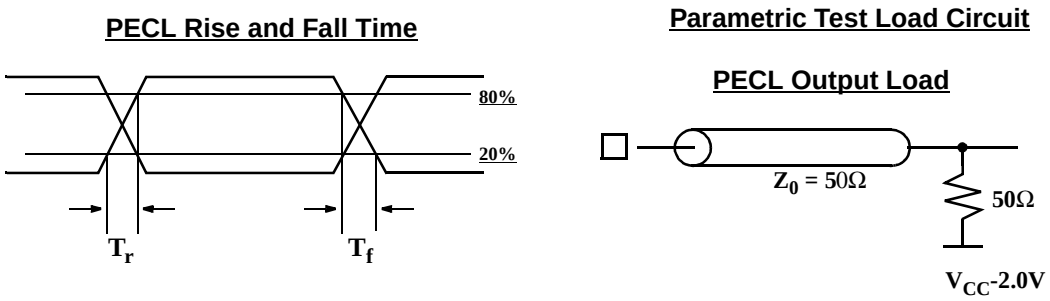
Table 2: DC Characteristics *(Over recommended operating conditions)*.

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	PECL output high voltage	V_{CC}-1.02	—	V_{CC}-0.70	V	50Ω Termination to V_{CC} - 2.0V, See Figure 7
V_{OL}	PECL output low voltage	V_{CC}-2.00	—	V_{CC}-1.62	V	50Ω Termination to V_{CC} - 2.0V, See Figure 7
$\Delta V_{OLVPECL}$	Low speed output voltage differential peak-to-peak swing.	400	—	1300	mV	AC Coupled
ΔV_{IHSAC}	Serial input differential voltage AC coupled	200	—	—	mV	AC Coupled, internally biased to $(V_{CC}+V_{EE})/2$
ΔV_{IHSDC}	Serial input differential voltage DC coupled	200	—	—	mV	DC coupled
ΔV_{CMI}	Serial input common mode voltage	V_{CC}-1.5		V_{CC}-0.5	V	
V_{CC}	Supply voltage	3.14	—	3.47	V	3.3V± 5%
P_D	Power dissipation	—	.75	1.1	W	Outputs open, V_{CC} = 3.45V
I_{DD}	Supply Current	—	220	320	mA	Outputs open, V_{CC} = 3.45V

Figure 8: Parametric Measurement Information



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Absolute Maximum Ratings (1)

Power Supply Voltage, (V_{CC}) ..... -0.5V to +3.8V
DC Input Voltage (Differential inputs) ..... -0.5V to V_{cc}+0.5V
Output Current (Differential Outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55^{o} to +125^{o}C
Storage Temperature ..... -65^{o}C to +150^{o}C
Maximum Input ESD (Human Body Model) 1500V

Recommended Operating Conditions

Power Supply Voltage, (V_{CC}) ..... +3.3V$\pm$5%
Operating Temperature Range ..... 0^{o}C Ambient to +85^{o}C Case Temperature

Notes:
(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC8164 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500V.

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Package Pin Descriptions

Table 3: Pin Identification

Pin	Name	I/O	Level	Description
1	NC	-	-	No connect, leave unconnected
2	NC	-	-	No connect, leave unconnected
3	NC	-	-	No connect, leave unconnected
4	NC	-	-	No connect, leave unconnected
5	NC	-	-	No connect, leave unconnected
6	NC	-	-	No connect, leave unconnected
7	NC	-	-	No connect, leave unconnected
8	NC	-	-	No connect, leave unconnected
9	NC	-	-	No connect, leave unconnected
10	HSDREF	I	voltage	High speed data input termination voltage reference
11	NC	-	-	No connect, leave unconnected
12	VEE	-	GND typ	Negative power supply pins
13	D+	I	HS	High jspeed data input, true
14	D-	I	HS	High speed data input, complement
15	VCC	-	+3.3V typ	Positive power supply pins
16	VEE	-	GND typ	Negative power supply pins
17	VEE	-	GND typ	Negative power supply pins
18	VCC	-	+3.3V typ	Positive power supply pins
19	HSCLK-	I	HS	High speed clock input, complement
20	HSCLK+	I	HS	High speed clock input, true
21	VCC	-	+3.3V typ	Positive power supply pins
22	HSCLKREF	I	voltage	High speed clock input termination voltage reference
23	NC	-	-	No connect, leave unconnected
24	NC	-	-	No connect, leave unconnected
25	NC	-	-	No connect, leave unconnected
26	NC	-	-	No connect, leave unconnected
27	NC	-	-	No connect, leave unconnected
28	NC	-	-	No connect, leave unconnected
29	NC	-	-	No connect, leave unconnected
30	NC	-	-	No connect, leave unconnected
31	NC	-	-	No connect, leave unconnected
32	NC	-	-	No connect, leave unconnected
33	NC	-	-	No connect, leave unconnected

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Pin	Name	I/O	Level	Description
34	NC	-	-	No connect, leave unconnected
35	NC	-	-	No connect, leave unconnected
36	NC	-	-	No connect, leave unconnected
37	NC	-	-	No connect, leave unconnected
38	NC	-	-	No connect, leave unconnected
39	NC	-	-	No connect, leave unconnected
40	NC	-	-	No connect, leave unconnected
41	NC	-	-	No connect, leave unconnected
42	NC	-	-	No connect, leave unconnected
43	NC	-	-	No connect, leave unconnected
44	NC	-	-	No connect, leave unconnected
45	NC	-	-	No connect, leave unconnected
46	NC	-	-	No connect, leave unconnected
47	NC	-	-	No connect, leave unconnected
48	NC	-	-	No connect, leave unconnected
49	NC	-	-	No connect, leave unconnected
50	NC	-	-	No connect, leave unconnected
51	NC	-	-	No connect, leave unconnected
52	NC	-	-	No connect, leave unconnected
53	NC	-	-	No connect, leave unconnected
54	VCC	-	+3.3V typ	Positive power supply pins
55	NC	-	-	No connect, leave unconnected
56	NC	-	-	No connect, leave unconnected
57	VEE	-	GND typ	Negative power supply pins
58	D15+	O	LVPECL	Low speed differential parallel data
59	D15-	O	LVPECL	Low speed differential parallel data
60	VCC	-	+3.3V typ	Positive power supply pins
61	D14+	O	LVPECL	Low speed differential parallel data
62	D14-	O	LVPECL	Low speed differential parallel data
63	NC	-	-	No connect, leave unconnected
64	VCC	-	+3.3V typ	Positive power supply pins
65	NC	-	-	No connect, leave unconnected
66	VCC	-	+3.3V typ	Positive power supply pins
67	D13+	O	LVPECL	Low speed differential parallel data
68	D13-	O	LVPECL	Low speed differential parallel data
69	VEE	-	GND typ	Negative power supply pins

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Pin	*Name*	*I/O*	*Level*	*Description*
70	D12+	O	LVPECL	Low speed differential parallel data
71	D12-	O	LVPECL	Low speed differential parallel data
72	VCC	-	+3.3V typ	Positive power supply pins
73	D11+	O	LVPECL	Low speed differential parallel data
74	D11-	O	LVPECL	Low speed differential parallel data
75	VCC	-	+3.3V typ	Positive power supply pins
76	D10+	O	LVPECL	Low speed differential parallel data
77	D10-	O	LVPECL	Low speed differential parallel data
78	VEE	-	GND typ	Negative power supply pins
79	D9+	O	LVPECL	Low speed differential parallel data
80	D9-	O	LVPECL	Low speed differential parallel data
81	VCC	-	+3.3V typ	Positive power supply pins
82	D8+	O	LVPECL	Low speed differential parallel data
83	D8-	O	LVPECL	Low speed differential parallel data
84	VCC	-	+3.3V typ	Positive power supply pins
85	D7+	O	LVPECL	Low speed differential parallel data
86	D7-	O	LVPECL	Low speed differential parallel data
87	VEE	-	GND typ	Negative power supply pins
88	D6+	O	LVPECL	Low speed differential parallel data
89	D6-	O	LVPECL	Low speed differential parallel data
90	VCC	-	+3.3V typ	Positive power supply pins
91	D5+	O	LVPECL	Low speed differential parallel data
92	D5-	O	LVPECL	Low speed differential parallel data
93	VCC	-	+3.3V typ	Positive power supply pins
94	D4+	O	LVPECL	Low speed differential parallel data
95	D4-	O	LVPECL	Low speed differential parallel data
96	VEE	-	GND typ	Negative power supply pins
97	D3+	O	LVPECL	Low speed differential parallel data
98	D3-	O	LVPECL	Low speed differential parallel data
99	VCC	-	+3.3V typ	Positive power supply pins
100	D2+	O	LVPECL	Low speed differential parallel data
101	D2-	O	LVPECL	Low speed differential parallel data
102	VCC	-	+3.3V typ	Positive power supply pins
103	VCC	-	+3.3V typ	Positive power supply pins
104	NC	-	-	No connect, leave unconnected
105	D1+	O	LVPECL	Low speed differential parallel data

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Pin	*Name*	*I/O*	*Level*	*Description*
106	D1-	O	LVPECL	Low speed differential parallel data
107	VCC	-	+3.3V typ	Positive power supply pins
108	D0+	O	LVPECL	Low speed differential parallel data
109	D0-	O	LVPECL	Low speed differential parallel data
110	VEE	-	GND typ	Negative power supply pins
111	CLK16O-	O	LVPECL	Parallel clock output, complement
112	CLK16O+	O	LVPECL	Parallel clock output, true
113	VCC	-	+3.3V typ	Positive power supply pins
114	CLK32O-	O	LVPECL	Divided parallel clock output, complement
115	CLK32O+	O	LVPECL	Divided parallel clock output, true
116	NC	-	-	No connect, leave unconnected
117	NC	-	-	No connect, leave unconnected
118	NC	-	-	No connect, leave unconnected
119	NC	-	-	No connect, leave unconnected
120	NC	-	-	No connect, leave unconnected
121	NC	-	-	No connect, leave unconnected
122	NC	-	-	No connect, leave unconnected
123	NC	-	-	No connect, leave unconnected
124	NC	-	-	No connect, leave unconnected
125	NC	-	-	No connect, leave unconnected
126	NC	-	-	No connect, leave unconnected
127	NC	-	-	No connect, leave unconnected
128	NC	-	-	No connect, leave unconnected

Note: No connect (NC) pins must be left unconnected, or floating. Connecting any of these pins to either the positive or negative power supply rails may cause improper operation or failure of the device; or in extreme cases, cause permanent damage to the device.

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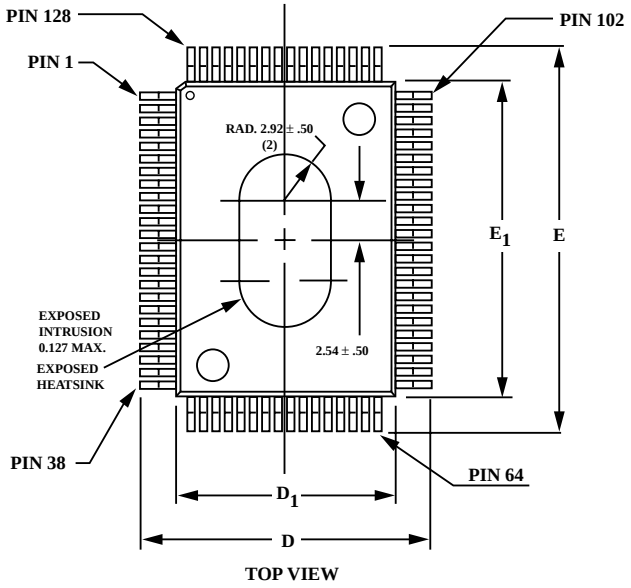
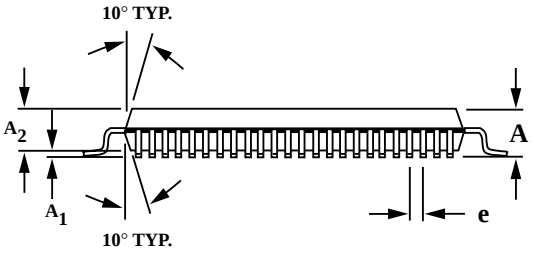
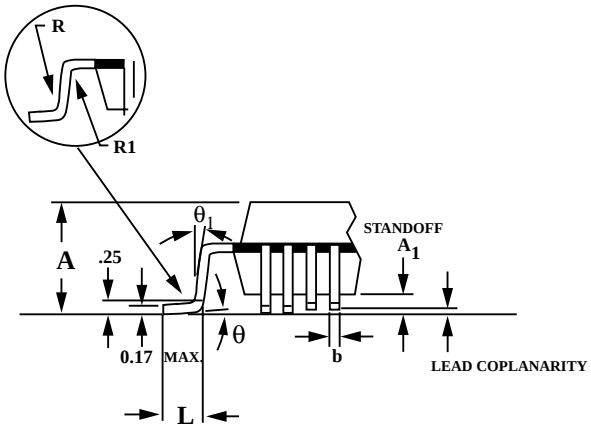
Package Information

128 PQFP Package Drawings



Key	*mm*	*Tolerance*
A	2.35	MAX
A1	0.25	MAX
A2	2.00	+.10
D	17.20	±.20
D1	14.00	±.10
E	23.20	±.20
E1	20.00	±.10
L	.88	+.15/-.10
e	.50	BASIC
b	.22	±.05
θ	0°-7°	
R	.30	TYP
R1	.20	TYP





Notes: 1) Drawing is not to scale
2) All dimensions in mm
3) Package represented is also used for the 64, 80, & 100 PQFP packages. Pin count drawn does not reflect the 128 Package.

NOTES:

Package #: 101-322-5
Issue #: 2

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Package Thermal Considerations

This package has been enhanced with a copper heat slug to provide a low thermal resistance path from the die to the exposed surface of the heat spreader. The thermal resistance is shown in the following table

Table 4: Thermal Resistance

Symbol	*Description*	*°C/W*
θ_{jc}	Thermal resistance from junction to case.	1.34
θ_{ca}	Thermal resistance from case to ambient with no airflow, including conduction through the leads.	25.0

Thermal Resistance with Airflow

Shown in the table below is the thermal resistance with airflow. This thermal resistance value reflects all the thermal paths including through the leads in an environment where the leads are exposed. The temperature difference between the ambient airflow temperature and the case temperature should be the worst case power of the device multiplied by the thermal resistance.

Table 5: Thermal Resistance with Airflow

Airflow	θ_{ca} (°C/W)
100 lfpm	21
200 lfpm	18
400 lfpm	16
600 lfpm	14.5

Maximum Ambient Temperature without Heatsink

The worst case ambient temperature without use of a heatsink is given by the equation:

$$T_{A(MAX)} = T_{C(MAX)} - P_{(MAX)}\theta_{CA}$$

where:

θ_{CA} Theta case to ambient at appropriate airflow
$T_{A(MAX)}$ Ambient Air temperature
$T_{C(MAX)}$ Case temperature (85°C for VSC8164)
$P_{(MAX)}$ Power (1.1 W for VSC8164)

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The results of this calculation are listed below:

Table 6: Maximum Ambient Air Temperature without Heatsink

Airflow	Max Ambient Temp ^{0}C
none	58
100 lfpm	62
200 lfpm	65
400 lfpm	67
600 lfpm	69

Note that ambient air temperature varies throughout the system based on the positioning and magnitude of heat sources and the direction of air flow.

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Ordering Information

The order number for this product is formed by a combination of the device number, and package type.

VSC8164 **QR**

Device Type
VSC8164:
2.488Gb/s to 2.7Gb/s
1:16 SONET/SDH Demux

Package
QR: 128PQFP, 14X20mm Body

Notice

This document contains information about a new product in the preproduction phase of development. The information contained in this document is based on initial product characterization. Vitesse reserves the right to alter specifications, features, capabilities, functions, manufacturing release dates, and even general availability of the product at any time. The reader is cautioned to confirm that this datasheet is current prior to using it for design.

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