April 2004

LMX2515
PLLatinum™ Frequency Synthesizer System with Integrated VCO

General Description

LMX2515 is a highly integrated, high performance, low power frequency synthesizer system optimized for Japan PDC mobile handsets. Using a proprietary digital phase locked loop technique, LMX2515 generates very stable, low noise local oscillator signals for up and down conversion in wireless communications devices.

LMX2515 includes a voltage controlled oscillator (VCO), a loop filter, and a fractional-N RF PLL based on a delta sigma modulator. In concert these blocks form a closed loop RF synthesizer system. The LMX2515LQ0701 supports the Japan PDC800 band and the LMX2515LQ1321 supports Japan PDC1500 band.

Serial data is transferred to the device via a three-wire MICROWIRE interface (DATA, LE, CLK).

Operating supply voltage ranges from 2.5 V to 3.3 V. LMX2515 features low current consumption.

LMX2515 is available in a 28-pin leadless leadframe package (LLP).

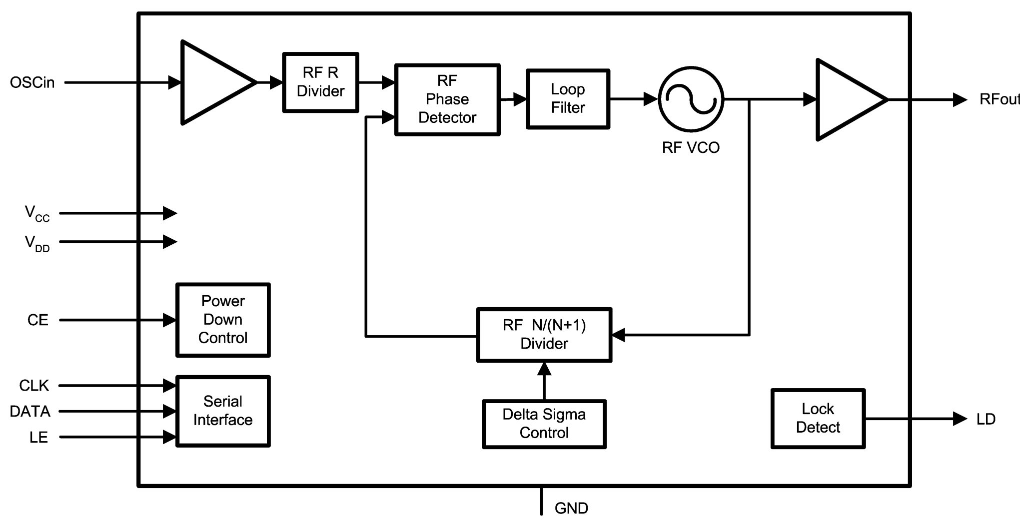
Features

- Small size
  5.0 mm X 5.0 mm X 0.75 mm 28-Pin LLP Package
- RF Synthesizer System
  Integrated RF VCO
  Integrated Loop Filter
  Low Spurious, Low Phase Noise Fractional-N RF PLL
  Based on 10-Bit Delta Sigma Modulator
  Frequency Resolution Down to 20 kHz
- Supports Various Reference Frequencies
  12.6/14.4/25.2/26.0 MHz
- Fast Lock Time: 300 µs
- Low Current Consumption
- 2.5 V to 3.3 V operation
- Digital Filtered Lock Detect Output
- Hardware and Software Power Down Control

Applications

- Japan PDC systems at 800 MHz frequency band.
- Japan PDC systems at 1500 MHz frequency band.

Functional Block Diagram



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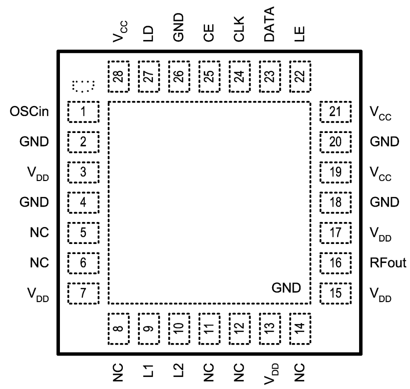
Connection Diagrams

28-Pin 5x5 LLP (LQ) Package (LMX2515LQ0701 - Top View)



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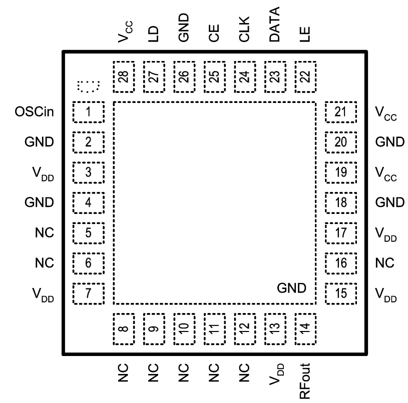
28-Pin 5x5 LLP (LQ) Package (LMX2515LQ1321 - Top View)



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Pin Descriptions

Pin Number LMX2515LQ0701	Pin Number LMX2515LQ1321	Name	I/O	Description
1	1	OSCin	I	Reference frequency input
2	2	GND	—	Ground for digital circuitry
3	3	V_{DD}	—	Supply voltage for analog circuitry
4	4	GND	—	Ground for analog circuitry
5	5	NC	—	Do not connect to any node on the printed circuit board.
6	6	NC	—	Do not connect to any node on the printed circuit board.
7	7	V_{DD}	—	Supply voltage for RF analog circuitry
8	8	NC	—	Do not connect to any node on the printed circuit board.
9		L1	—	RF VCO tank pin. An external inductor is required between pins L1 and L2 to set the resonant frequency of LMX2515LQ0701 RF VCO.
	9	NC	—	Do not connect to any node on the printed circuit board.
10		L2	—	RF VCO tank pin. An external inductor is required between pins L1 and L2 to set the resonant frequency of LMX2515LQ0701 RF VCO.
	10	NC	—	Do not connect to any node on the printed circuit board.
11	11	NC	—	Do not connect to any node on the printed circuit board.
12	12	NC	—	Do not connect to any node on the printed circuit board.
13	13	V_{DD}	—	Supply voltage for RF analog circuitry
14		NC	—	Do not connect to any node on the printed circuit board.
	14	RFout	O	RF VCO output for LMX2515LQ1321
15	15	V_{DD}	—	Supply voltage for RF analog circuitry
16		RFout	O	RF VCO output for LMX2515LQ0701
	16	NC	—	Do not connect to any node on the printed circuit board.
17	17	V_{DD}	—	Supply voltage for analog circuitry
18	18	GND	—	Ground for digital circuitry
19	19	V_{CC}	—	Supply voltage for digital circuitry
20	20	GND	—	Ground for digital circuitry
21	21	V_{CC}	—	Supply voltage for digital circuitry
22	22	LE	I	MICROWIRE Latch Enable
23	23	DATA	I	MICROWIRE Data

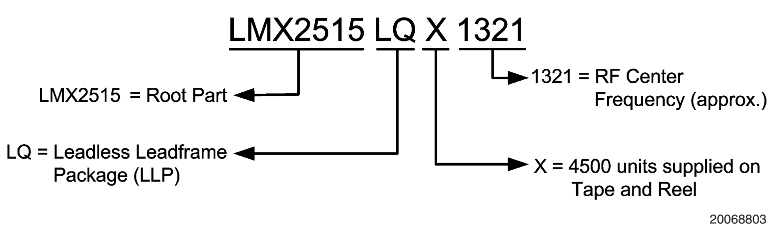
Pin Descriptions (Continued)

Pin Number LMX2515LQ0701	Pin Number LMX2515LQ1321	Name	I/O	Description
24	24	CLK	I	MICROWIRE Clock
25	25	CE	I	Chip enable control pin
26	26	GND	—	Ground for digital circuitry
27	27	LD	O	Lock detect pin
28	28	V_{CC}	—	Supply voltage for digital circuitry

Ordering Information

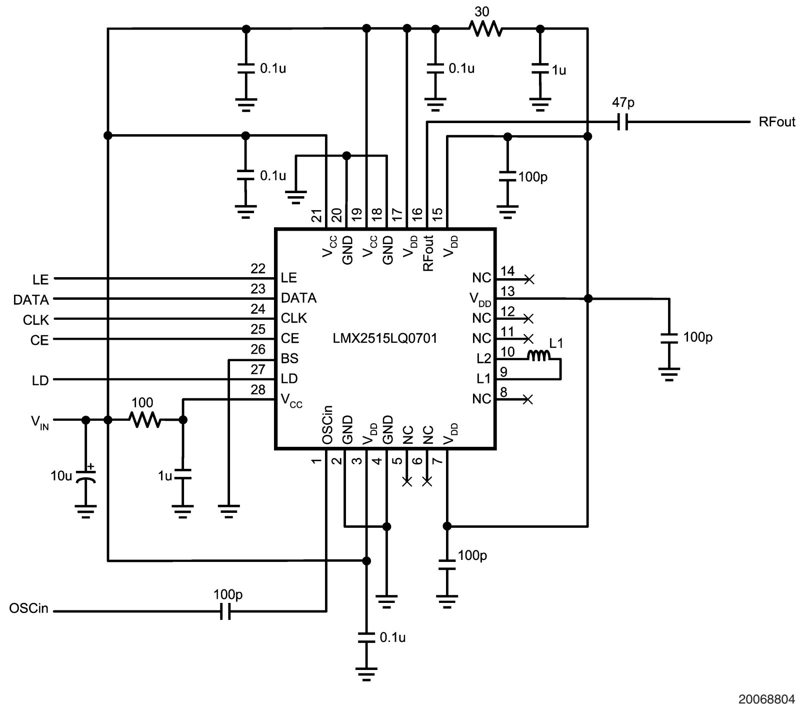
Order Part Number	RF Min. (MHz)	RF Max. (MHz)	RF Center (MHz)	Package Marking	Supplied As
LMX2515LQX0701	633.15	768	~0701	25150701	4500 units on tape and reel
LMX2515LQ0701	633.15	768	~0701	25150701	1000 units on tape and reel
LMX2515LQX1321	1270.22	1394.95	~1321	25151321	4500 units on tape and reel
LMX2515LQ1321	1270.22	1394.95	~1321	25151321	1000 units on tape and reel

Part Number Description

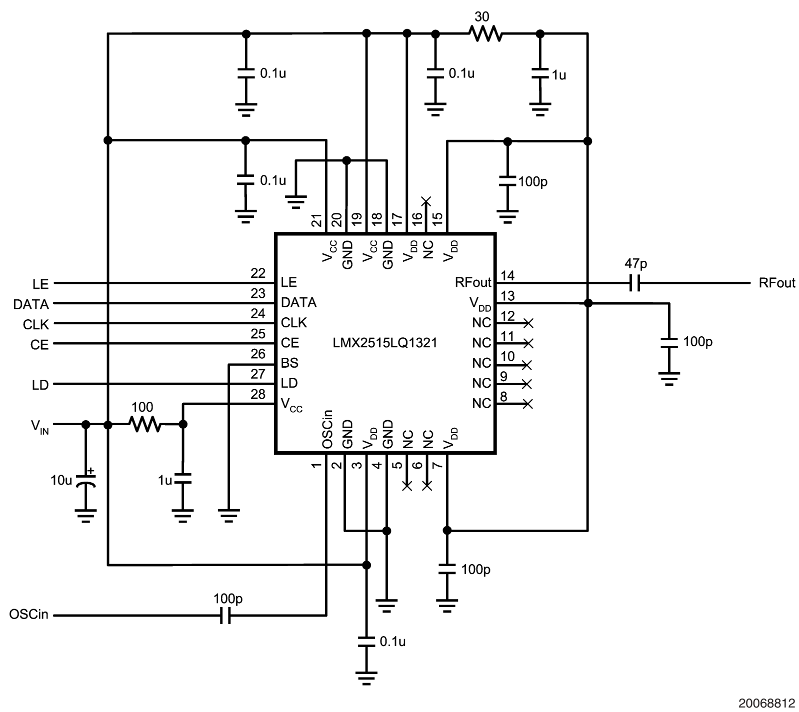


Typical Application Circuit

LMX2515LQ0701 Application Circuit (Note 1)



LMX2515LQ1321 Application Circuit (Note 2)



Note 1: Refer to LMX2515LQ0701 Tuning Range vs. External Inductance plot to aid in selecting the appropriate external inductance, PCB trace and L1, for the desired frequency range.

Note 2: No external inductance required.

Absolute Maximum Ratings (Notes 3, 4, 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Parameter	Symbol	Ratings	Units
Supply Voltage	V_{CC}, V_{DD}	-0.5 to 3.6	V
Voltage on any pin with GND	V_I	-0.3 to V_{CC}+0.3	V
		-0.3 to V_{DD}+0.3	V
Storage Temperature Range	T_{STG}	-65 to 150	˚C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Temperature	T_A	-30	25	85	˚C
Supply Voltage (to GND)	V_{CC}, V_{DD}	2.5		3.3	V

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, refer to the Electrical Characteristics section. The guaranteed specifications apply only for the conditions listed.

Note 4: This device is a high performance RF integrated circuit with an ESD rating < 2 kV and is ESD sensitive. Handling and assembly of this device should be done at ESD protected workstations.

Note 5: GND = 0 V.

Electrical Characteristics

(V_{IN} = 2.8 V, refer to Typical Application Circuit; Limits in standard typeface are for T_A = 25 ˚C; Limits in **boldface** type apply over the operating temperature range from -20 ˚C ≤ T_A ≤ 75 ˚C unless otherwise noted.)

Symbol	Parameter		Condition	Min	Typ	Max	Units
I_{CC} PARAMETERS							
I_{CC} + I_{DD}	Supply Current	LMX2515LQ0701	OB_CRL [1:0] = 11		11.5	13.0 **13.3**	mA
			OB_CRL [1:0] = 00		10.0	11.5 **11.8**	mA
		LMX2515LQ1321	OB_CRL [1:0] = 11		16.0	17.5 **17.8**	mA
			OB_CRL [1:0] = 00		14.2	15.6 **15.9**	mA
	Power Down Current		CE = LOW or RF_PD = 1			20	µA
REFERENCE OSCILLATOR PARAMETERS							
f_{OSCin}	Reference Oscillator Input Frequency (Note 6)		12.6/14.4/25.2/26.0 MHz are supported.	12.6	14.4	26.0	MHz
V_{OSCin}	Reference Oscillator Input Sensitivity				0.5	V_{CC}	Vp-p
RF VCO							
f_{RFout}	Frequency Range	LMX2515LQ0701		633.15		768	MHz
		LMX2515LQ1321		1270.22		1394.95	MHz
P_{RFout}	Output Power	LMX2515LQ0701	OB_CRL [1:0] = 11	**-6**	-3	**0**	dBm
			OB_CRL [1:0] = 10	**-9**	-6	**-3**	dBm
			OB_CRL [1:0] = 01	**-11**	-8	**-5**	dBm
			OB_CRL [1:0] = 00	**-15**	-12	**-9**	dBm
		LMX2515LQ1321	OB_CRL [1:0] = 11	**-5**	-2	**1**	dBm
			OB_CRL [1:0] = 10	**-7**	-4	**-1**	dBm
			OB_CRL [1:0] = 01	**-10**	-7	**-4**	dBm
			OB_CRL [1:0] = 00	**-13**	-10	**-7**	dBm
	Lock Time		Full frequency span in High Speed Mode.			**300** (Note 8)	µs
			Full frequency span in Normal Mode.			**500** (Note 8)	µs
						375 (Note 9)	µs
	RMS Phase Error				1.3		degrees

Electrical Characteristics (V_{IN} = 2.8 V, refer to Typical Application Circuit; Limits in standard typeface are for T_A = 25 ˚C; Limits in **boldface** type apply over the operating temperature range from -20 ˚C ≤ T_A ≤ 75 ˚C unless otherwise noted.) (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
RF VCO						
$L(f)_{RFout}$	Phase Noise in Normal Mode.	@ 25 kHz offset		-95	-93 **-91**	dBc/Hz
		@ 50 kHz offset		-106	-103 **-101**	dBc/Hz
		@ 100 kHz offset		-115	-113 **-111**	dBc/Hz
		@ 1 MHz offset			-135 **-133**	dBc/Hz
	2nd Harmonic Suppression				**-25**	dBc
	3rd Harmonic Suppression				**-20**	dBc
	Spurious Tones	@ ≤ 25 kHz offset			**-45**	dBc
		@ 25 kHz < offset ≤ 50 kHz			**-60**	dBc
		@ 50 kHz < offset ≤ 100 kHz			**-69**	dBc
		@ offset > 100 kHz			**-75**	dBc
DIGITAL INTERFACE (DATA, CLK, LE, LD, CE)						
V_{IH}	High-Level Input Voltage		0.8 V_{CC}		V_{CC}	V
			0.8 V_{DD}		V_{DD}	V
V_{IL}	Low-Level Input Voltage		-0.3		0.2 V_{CC}	V
			-0.3		0.2 V_{DD}	V
I_{IH}	High-Level Input Current		-10		10	µA
I_{IL}	Low-Level Input Current		-10		10	µA
	Input Capacitance			3		pF
	Rise/Fall Time			30		ns
V_{OH}	High-Level Output Voltage		V_{CC} - 0.4			V
			V_{DD} - 0.4			V
V_{OL}	Low-Level Output Voltage				0.4	V
	Output Capacitance				5	pF
MICROWIRE INTERFACE TIMING						
t_{CS}	Data to Clock Set Up Time		50			ns
t_{CH}	Data to Clock Hold Time		10			ns
t_{CWH}	Clock Pulse Width HIGH		50			ns
t_{CWL}	Clock Pulse Width LOW		50			ns
t_{ES}	Clock to Latch Enable Set Up Time		50			ns
t_{EW}	Latch Enable Pulse Width		50			ns

Note 6: The reference frequency must also be programmed using the OSC_FREQ control bit. For other reference frequencies, please contact National Semiconductor.

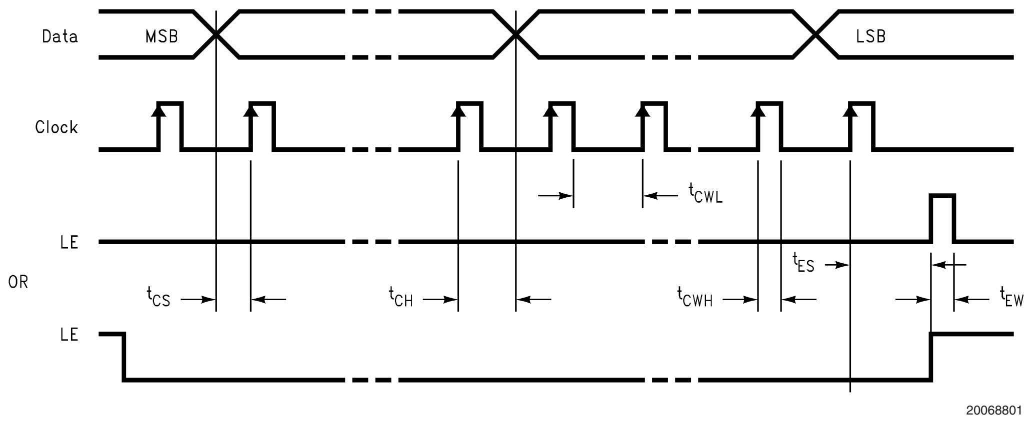
Note 7: For other frequency ranges, please contact National Semiconductor.

Note 8: Lock time is defined as the time difference between the beginning of the frequency transition and the point at which the frequency remains within +/-1 kHz of the final frequency.

Note 9: Lock time is defined as the time difference between the beginning of the frequency transition and the point at which the frequency remains within +/-3 kHz of the final frequency.

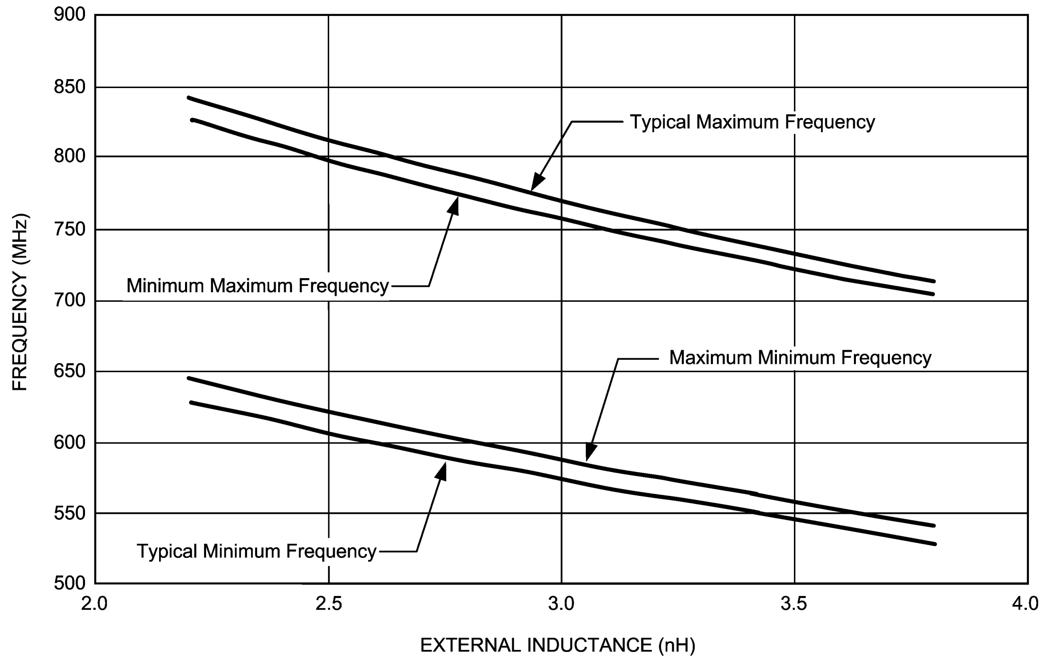
Note 10: All limits are guaranteed. All electrical characteristics having room temperature limits are tested during production with T_A = 25 ˚C or correlated using Statistical Quality Control (SQC) methods. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Microwire Interface Timing Diagram



Typical Performance Characteristics (Note 11)

LMX2515LQ0701 Tuning Range vs. External Inductance (Note 12)
V_{IN} = 2.8 V



Note 11: Typical performance characteristics do not guarantee specific performance limits. For guaranteed specifications, refer to the Electrical Characteristics section.

Note 12: The frequency range is defined as the difference between the highest frequency and the lowest frequency of a given unit. For a chosen external inductance, the typical frequency range equals the difference between the Typical Maximum Frequency and the Typical Minimum Frequency. Typical frequency range may be assumed on any unit with that chosen external inductance, even if the unit has worst case Maximum Frequency or worst case Minimum Frequency.

Functional Description

GENERAL

The LMX2515 is a highly integrated frequency synthesizer system for Japan PDC wireless communication systems. The LMX2515LQ0701 supports operation for 800 MHz band and the LMX2515LQ1321 supports operation for 1500 MHz band.

The LMX2515 includes all functional blocks for the RF PLL including RF VCO, frequency divider, PFD, and loop filter. Only external passive elements for the RF VCO tank (LMX2515LQ0701 only) and supply bypassing are required to complete the RF synthesizer.

The LMX2515 uses a patent pending Fractional-N synthesizer architecture based on a delta sigma modulator to support fine frequency resolution. Four of the most common reference frequencies for PDC applications, 12.6 MHz, 14.4 MHz, 25.2 MHz and 26.0 MHz, are supported. The unique feature of this architecture is its low spurious modulation effect.

The use of a fractional synthesizer based on delta sigma modulator allows for fast lock-up and system set-up times, which reduces system power consumption. The loop filter is included in the circuit to minimize the external noise coupling and reduce the form factor applicable to the board level application.

RF_PLL SECTION

Frequency Selection

The divide ratio can be calculated using the following equations:

f_{VCO} = {8 x RF_B + RF_A + (RF_FN / FD)} x (f_{OSC} / R) where (RF_A < RF_B) for LMX2515LQ1321

f_{VCO} = {4 x RF_B + RF_A + (RF_FN / FD)} x (f_{OSC} / R) where (RF_A < RF_B) for LMX2515LQ0701

f_{VCO}: Output frequency of voltage controlled oscillator (VCO)

RF_B: Preset divide ratio of binary 4-bit programmable counter (2 ≤ RF_B ≤ 15)

RF_A: Preset divide ratio of binary 3-bit swallow counter (0 ≤ RF_A ≤ 7 for LMX2515LQ1321 and 0 ≤ RF_A ≤ 3 for LMX2515LQ0701)

RF_FN: Preset numerator of binary 10-bit modulus counter (0 ≤ RF_FN < FD)

FD: Preset denominator for modulus counter (FD = f_{OSC}/(R X f_{CH}) where f_{CH} is the channel spacing)

f_{OSC}: Reference oscillation frequency

R: Internal reference oscillator frequency divider (1 for 12.6 MHz and 14.4 MHz, 2 for 25.2 MHz and 26.0 MHz)

The denominator, FD, in the above equation is dependent on the channel spacing and reference oscillator frequency. The channel spacing will change based on the Rx/Tx and RF_SEL bits. *Table 6* in the R0 Register section summarizes the values of FD.

VCO Frequency Tuning

The center frequency of the LMX2515 RF VCO is determined by the resonant frequency of the tank circuit, illustrated in *Figure 1*. With an internal fixed bonding-wire inductor and an external inductor, the center frequency of the VCO is given as follows:

$$f_{center} = \frac{1}{2\pi\sqrt{(L_{fixed} + L_{external}) \cdot C_{total}}}$$

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where C_{total} is the total capacitance of the VCO, including the parasitic capacitance and the nominal self-tuning capacitance. Note, for the LMX2515LQ0701, the external inductance consists of the PCB traces and lumped element inductor. The output frequency tuning range can be optimized for the specific application by selecting the appropriate external inductance. Refer to LMX2515LQ0701 Tuning Range vs. External Inductance plot to aid in selecting the appropriate external inductance. Care should be taken to ensure proper frequency coverage when choosing the tolerance of the lumped element inductor.

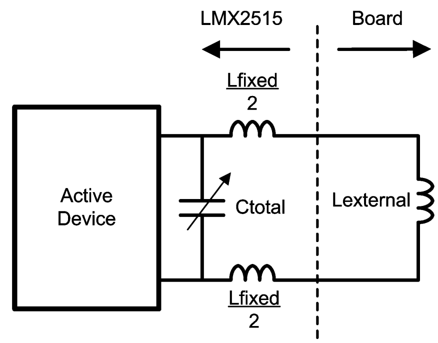

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FIGURE 1. External Inductor Connection

For the LMX2515LQ1321, the internal bonding-wires provide the necessary inductance to set the VCO center frequency and no external inductance is required.

In real implementation, the inductance of L_{fixed} and $L_{external}$ can vary from its nominal value. The LMX2515 utilizes a built-in tracking algorithm to compensate for variations up to ±15% and tunes the VCO to the required frequency. During the frequency acquisition period, the loop bandwidth is extended to achieve the frequency lock. After the frequency lock, the loop bandwidth of the PLL is set to the nominal value and the phase lock is achieved. The transition between the two operating modes is very smooth and extremely fast to meet the stringent PDC requirements for lock time and phase noise.

POWER DOWN MODE

The LMX2515 includes the power down mode to reduce the power consumption. The LMX2515 enters the power down mode either by taking the CE pin LOW or by setting the RF_PD bit in the R0 register. If the CE pin is set LOW, the circuit is powered down regardless of the register values. When the CE pin is HIGH, the RF_PD bit controls power to the RF circuitry. Data can be written to the registers even when the CE pin is set LOW. The following truth table summarizes the power down logic.

Functional Description (Continued)

TABLE 1. Power Down Modes

CE pin	RF_PD Bit	Mode
HIGH	0	Active
HIGH	1	Not Active
LOW	0	Not Active
LOW	1	Not Active

VCO SELECTION

The RF_SEL bit must be used to select the RF VCO output. When using the LMX2515LQ0701 the RF_SEL bit must be set to "0". When using the LMX2515LQ1321 the RF_SEL bit must be set to "1".

TABLE 2. VCO Selection

RF_SEL Bit	Mode
0	LMX2515LQ0701
1	LMX2515LQ1321

LOCK DETECT MODE

The LD output can be used to indicate the lock status of the PLL. Bit 6 in Register R1 determines the signal that appears on the LD pin. When the PLL is not locked, the LD pin remains LOW. After obtaining phase lock, the LD pin will have a logical HIGH level. The LD output is always low when the LD register bit is 0 and in power down mode.

TABLE 3. Lock Detect Modes

LD Bit	Mode
0	Disable (GND)
1	Enable

TABLE 4. Lock Detect Logic

RF-PLL Section	LD Output
Locked	HIGH
Not Locked	LOW

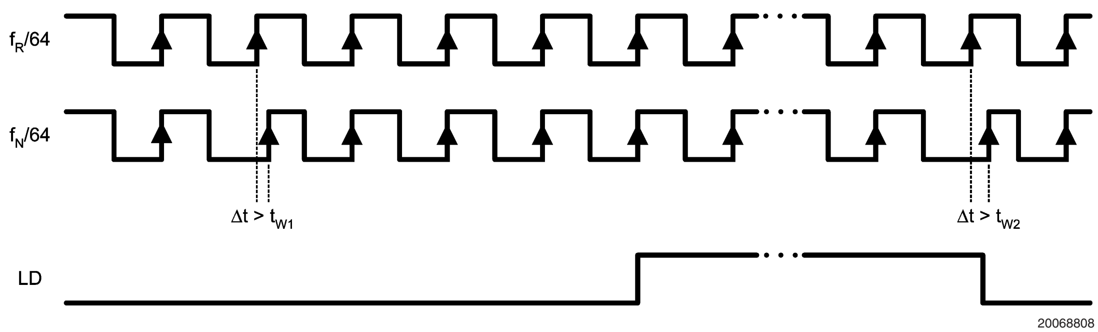


FIGURE 2. Lock Detect Timing Diagram Waveform (Notes 13, 14, 15, 16, 17)

Note 13: LD output becomes low when the phase error is larger than t_{W2}.

Note 14: LD output becomes high when the phase error is less than t_{W1} for four or more consecutive cycles.

Note 15: Phase Error is measured on leading edge. Only errors greater than t_{W1} and t_{W2} are labeled.

Note 16: t_{W1} is 5 ns for LMX2515LQ1321 and 10 ns for LMX2515LQ0701. t_{W2} is 10 ns for both devices.

Note 17: The lock detect comparison occurs with every 64^{th} cycle of f_R and f_N

Functional Description (Continued)

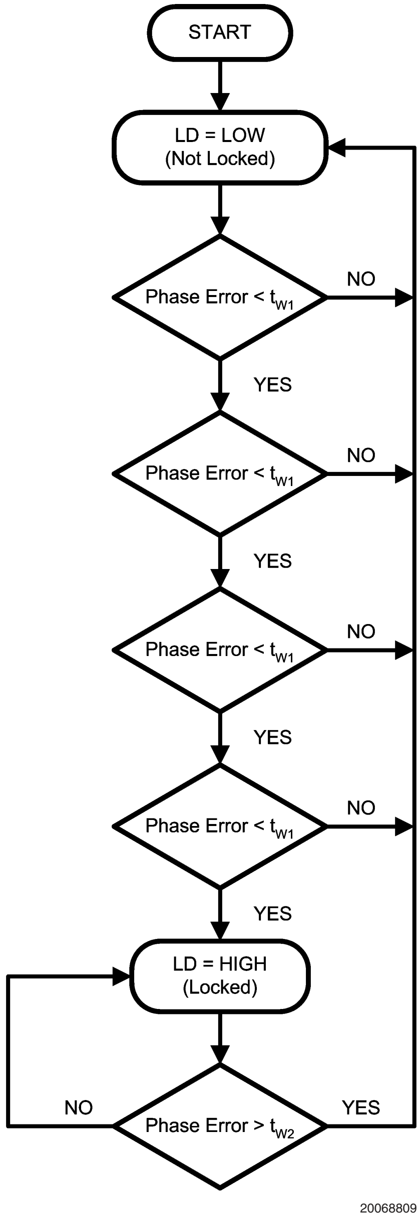


FIGURE 3. Lock Detect Flow Diagram

HIGH SPEED LOCK-UP MODE

Two frequency-locking modes are provided: a Normal mode and a High Speed mode for faster lock times. The HS bit in register R0 controls the locking mode.

TABLE 5. Lock-up Modes

HS Bit	Mode
0	Normal mode
1	High Speed mode

MICROWIRE INTERFACE

The programmable register set is accessed via the MICROWIRE serial interface. The interface is comprised of three signal pins: CLK, DATA, and LE (Latch Enable). Serial data is clocked into the 24-bit shift register on the rising edge of the clock. The last bits decode the internal control register address. When the latch enable (LE) transitions from LOW to HIGH, data stored in the shift registers is loaded into the corresponding control register. The data is loaded MSB first.

Programming Description

GENERAL PROGRAMMING INFORMATION

The serial interface has a 24-bit shift register to store the incoming data bits temporarily. The incoming data is first loaded into the shift register from MSB to LSB. The data is shifted at the rising edge of the clock signal. When the latch enable signal transitions from LOW to HIGH, the data stored in shift register is transferred to the proper register depending on the address bit setting. The selection of the particular register is determined by the control bits indicated in boldface text.

At initial start-up, the MICROWIRE loading requires three default words (registers R2, loaded first, to R0, loaded last). After the device has been initially programmed, the RF VCO frequency can be changed using a single register (R0).

The control register content map describes how the bits within each control register are allocated to the specific control functions.

COMPLETE REGISTER MAP

Register	**MSB**	**SHIFT REGISTER BIT LOCATION**																						**LSB**
	23	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R0 (Default)	RX/ TX	RF_ PD	HS	0	RF_ SEL	RF_B [3:0]				RF_A [2:0]			RF_FN [9:0]										**0**	**0**
R1 (Default)	SPI_ DEF	0	0	1	0	0	1	0	1	0	0	0	0	0	0	1	0	LD	OB_ CRL [1:0]		OSC_ FREQ [1:0]		**0**	**1**
R2 (Default)	1	1	0	0	1	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	**1**	**0**
R3	1	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	**0**	**1**	**1**
R4	0	0	0	0	0	0	1	1	1	0	1	0	0	0	1	1	0	0	1	0	**0**	**1**	**1**	**1**
R5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**1**	**1**	**1**	**1**

Note: R0 control register will be used when hot start frequency change.

Note: Boldface text represent address bits.

Programming Description (Continued)

R0 REGISTER

The R0 register address bits (R0 [1:0]) are “00”.

The Rx/Tx bit selects between receive and transmit modes and, in conjunction with the RF VCO selection bit (RF_SEL), the channel spacing to be synthesized.

The RF_PD bit selects the power down mode of the RF PLL and selected VCO.

The HS bit selects between normal and high speed locking mode.

The RF_SEL bit is set to "0" for the LMX2515LQ0701 and "1" for the LMX2515LQ1321.

The RF N counter consists of the 4-bit programmable counter (RF_B counter), the 3-bit swallow counter (RF_A counter) and the 10-bit delta sigma modulator (RF_FN counter). The equations for calculating the counter values are presented below.

R0 REGISTER

Register	MSB	SHIFT REGISTER BIT LOCATION																						LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																						Address Field	
R0 (Default)	RX/TX	RF_PD	HS	0	RF_SEL	RF_B [3:0]				RF_A [2:0]			RF_FN [9:0]										**0**	**0**

Name	Functions
RX/TX	**RX/TX Mode** 0 = Rx 1 = Tx
RF_PD	**Power Down of RF Synthesizer** 0 = RF synthesizer on (Active mode) 1 = RF synthesizer powered down
HS	**Locking Mode** 0 = Normal Mode 1 = High Speed Mode
RF_SEL	**RF VCO Selection** 0 = LMX2515LQ0701 1 = LMX2515LQ1321
RF_B [3:0]	**RF_B Counter** 4-bit programmable counter 0 ≤ RF_B ≤ 15 for both bands
RF_A [2:0]	**RF_A Counter** 3-bit swallow counter 0 ≤ RF_A ≤ 7 for LMX2515LQ1321 0 ≤ RF_A ≤ 3 for LMX2515LQ0701
RF_FN [9:0]	**RF_FN Counter** 10-bit modulus counter 0 ≤ RF_FN < FD See *Table 6* for FD values.

Counter Name	Symbol	Functions
Modulus Counter	RF_FN	**RF N Divider** N = 8 x RF_B + RF_A + RF_FN/FD (LMX2515LQ1321) N = 4 x RF_B + RF_A + RF_FN/FD (LMX2515LQ0701)
Programmable Counter	RF_B	
Swallow Counter	RF_A	

Programming Description (Continued)

Pulse Swallow Function

f_{VCO} = {8 x RF_B + RF_A + (RF_FN / FD)} x f_{OSC} / R where (RF_A < RF_B) for LMX2515LQ1321

f_{VCO} = {4 x RF_B + RF_A + (RF_FN / FD)} x f_{OSC} / R where (RF_A < RF_B) for LMX2515LQ0701

f_{VCO}: Output frequency of voltage controlled oscillator (VCO)

RF_B: Preset divide ratio of binary 4-bit programmable counter (2 ≤ RF_B ≤ 15)

RF_A: Preset divide ratio of binary 3-bit swallow counter (0 ≤ RF_A ≤ 7 for LMX2515LQ1321 and 0 ≤ RF_A ≤ 3 for LMX2515LQ0701)

RF_FN: Preset numerator of binary 10-bit modulus counter (0 ≤ RF_FN < FD)

FD: Preset denominator for modulus counter (FD = f_{OSC}/(R x f_{CH}) where f_{CH} is the channel spacing)

f_{OSC}: Reference oscillator frequency

R: Internal reference oscillator frequency divider

OSC_FREQ [1:0]	Reference Oscillator Frequency (MHz)	R Divider
00	12.6	1
01	14.4	1
10	25.2	2
11	26.0	2

The value of the denominator (FD) is depended on the channel spacing and reference oscillator frequency. *Table 6* summarizes the denominator values based on the settings of the Rx/Tx, RF_SEL, and OSC_FREQ [1:0] bits.

TABLE 6. Demonimator Values

Part Number	RF_SEL	Rx/Tx	OSC_FREQ [1:0]	Reference Oscillator Frequency (MHz)	R	f_{CH} (kHz)	Denominator (FD)
LMX2515LQ0701	0	0	00	12.6	1	25.0	504
	0	0	01	14.4	1	25.0	576
	0	0	10	25.2	2	25.0	504
	0	0	11	26.0	2	25.0	520
	0	1	00	12.6	1	20.0	630
	0	1	01	14.4	1	20.0	720
	0	1	10	25.2	2	20.0	630
	0	1	11	26.0	2	20.0	650
LMX2515LQ1321	1	0	00	12.6	1	25.0	504
	1	0	01	14.4	1	25.0	576
	1	0	10	25.2	2	25.0	504
	1	0	11	26.0	2	25.0	520
	1	1	00	12.6	1	22.22	567
	1	1	01	14.4	1	22.22	648
	1	1	10	25.2	2	22.22	567
	1	1	11	26.0	2	22.22	585

Programming Description (Continued)

R1 REGISTER

The R1 register address bits (R1 [1:0]) are “01”.

The SPI_DEF bit allows for the programming of words R3 to R5. Under most circumstances, the SPI_DEF bit should be set to "1".

The LD bit sets the function of the lock detect pin. Enabling the lock detect function provides a digital lock detect output of the active RF synthesizer at the LD pin.

The OB_CRL [1:0] bits determine the power level of the RF output buffer. The power level can be adjusted to best meet the system requirement.

The reference frequency selection bits, OSC_FREQ [1:0], are used to set the reference clock and R divider for use with one of the following reference frequencies: 12.6 MHz, 14.4 MHz, 25.2 MHz or 26.0 MHz. The LMX2515 uses the OSC_FREQ bits along with the RF_SEL and RX/TX bits to determine the correct divide ratios needed to meet the required channel spacing for the mode of operation selected. Refer to *Table 6* for a summary of denominator values.

R1 REGISTER

Register	MSB	SHIFT REGISTER BIT LOCATION																				LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																						Address Field	
R1 (Default)	SPI_ DEF	0	0	1	0	0	1	0	1	0	0	0	0	0	0	1	0	LD	OB_ CRL [1:0]		OSC_ FREQ [1:0]		**0**	**1**

Name	Functions
SPI_DEF	**Default Register Selection** 0 = OFF (Use values set in R0 to R5) 1 = ON (Use default values set in R0 to R2)
LD	**Lock Detect** 0 = Disable (GND) 1 = Enable
OB_CRL [1:0]	**Output Buffer Control** LMX2515LQ1321, LMX2515LQ0701 00 = -10 dBm, -12 dBm 01 = -7 dBm, -8 dBm 10 = -4 dBm, -6 dBm 11 = -2 dBm, -3 dBm
OSC_FREQ [1:0]	**Reference Frequency Selection** 00 = 12.6 MHz 01 = 14.4 MHz 10 = 25.2 MHz 11 = 26.0 MHz

Programming Description (Continued)

R2 REGISTER

The R2 register address bits (R2 [1:0]) are “10”.

R2 REGISTER

Register	MSB	SHIFT REGISTER BIT LOCATION																					LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																						Address Field	
R2 (Default)	1	1	0	0	1	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	**1**	**0**

R3 REGISTER

The R3 register address bits (R3 [2:0]) are “011”. This register is only written to if the SPI_DEF bit is set to "0".

R3 REGISTER

Register	MSB	SHIFT REGISTER BIT LOCATION																					LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																					Address Field		
R3	1	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	1	**0**	**1**	**1**

R4 REGISTER

The R4 register address bits (R4 [3:0]) are “0111”. This register is only written to if the SPI_DEF bit is set to "0".

R4 REGISTER

Register	MSB	SHIFT REGISTER BIT LOCATION																					LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				Address Field			
R4	0	0	0	0	0	0	1	1	1	0	1	0	0	0	1	1	0	0	1	0	**0**	**1**	**1**	**1**

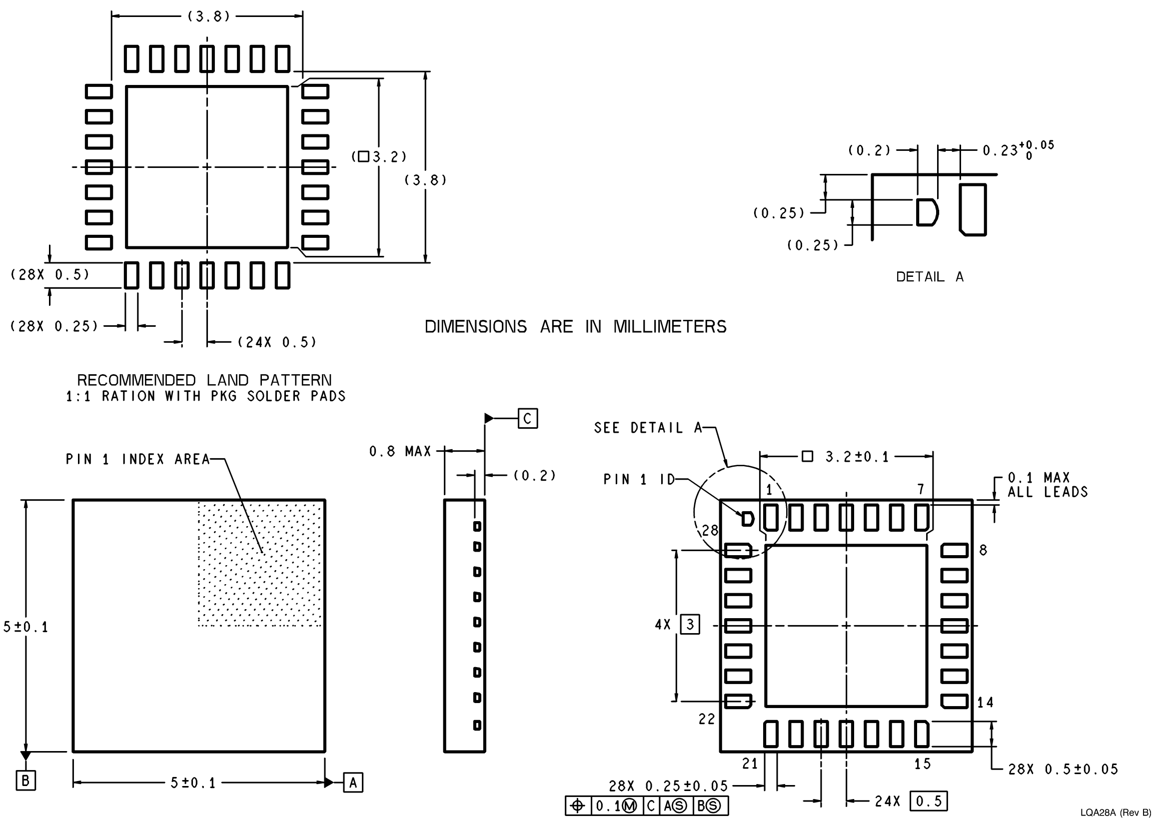
R5 REGISTER

The R5 register address bits (R5 [4:0]) are “01111”. This register is only written to if the SPI_DEF bit is set to "0".

R5 REGISTER

Register	MSB	SHIFT REGISTER BIT LOCATION																					LSB
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																			Address Field				
R5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**1**	**1**	**1**	**1**

Physical Dimensions inches (millimeters) unless otherwise noted



28-Pin Leadless Leadframe Package (LLP)
NSC Package Number LQA28A

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