## FEATURES

- Industrial temperature range (–40°C to +85°C)
- 3.3V power supply
- Clock and data recovery from 28Mbps up to 1.3Gbps NRZ data stream, clock generation from 28Mbps to 1.3Gbps
- Complies with Bellcore, ITU/CCITT and ANSI specifications for applications such as OC-1, OC-3, OC-12, ATM, FDDI, Fibre Channel and Gigabit Ethernet as well as proprietary applications
- Two on-chip PLLs: one for clock generation and another for clock recovery
- Selectable reference frequencies
- Differential PECL high-speed serial I/O
- Line receiver input: no external buffering needed
- Link fault indication
- 100k ECL compatible I/O
- Lower power: fully compatible with Micrel's SY87701V, but with 30% less power
- Available in 32-pin EPAD-TQFP and 28-pin SOIC packages (28-pin SOIC is available, but NOT recommended for new designs.)

## DESCRIPTION

The SY87701AL is a complete Clock Recovery and Data Retiming integrated circuit for data rates from 28Mbps up to 1.3Gbps NRZ. The device is ideally suited for SONET/SDH/ATM and Fibre Channel applications and other high-speed data transmission systems.

Clock recovery and data retiming is performed by synchronizing the on-chip VCO directly to the incoming data stream. The VCO center frequency is controlled by the reference clock frequency and the selected divide ratio. On-chip clock generation is performed through the use of a frequency multiplier PLL with a byte rate source as reference.

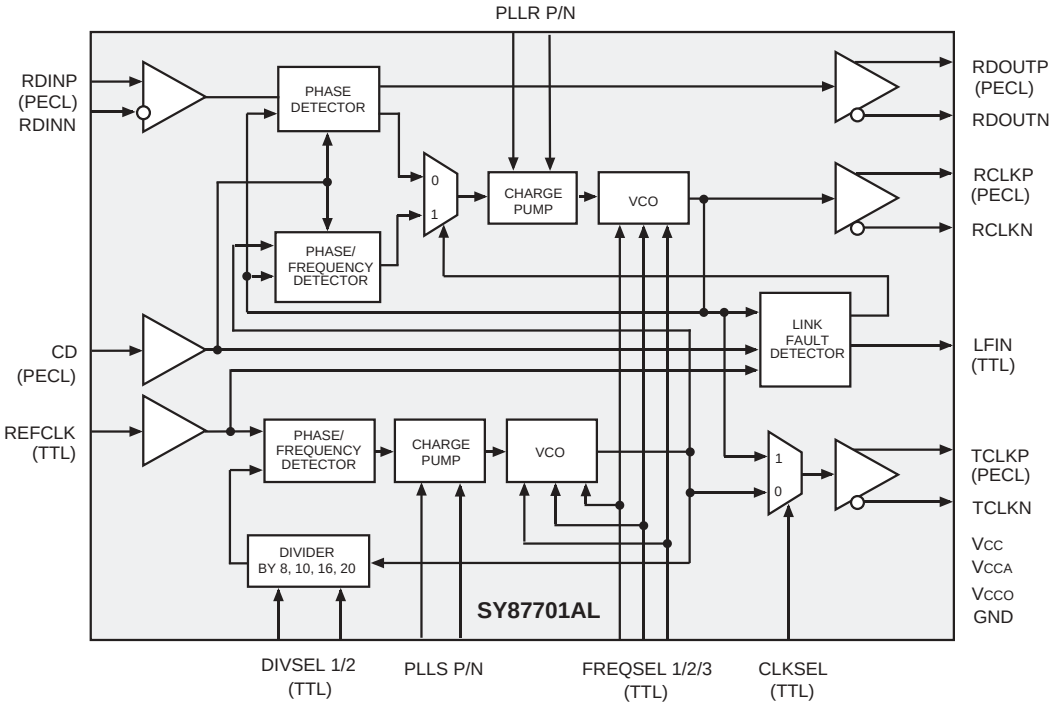
The SY87701AL also includes a link fault detection circuit.

All support documentation can be found on Micrel's web site at: www.micrel.com.

## APPLICATIONS

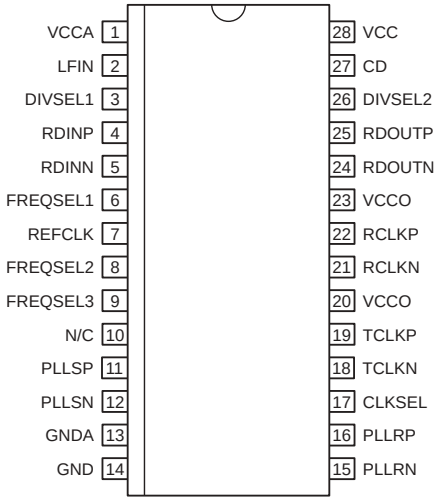
- SONET/SDH/ATM OC-1, OC-3, OC-12, OC-24
- Fibre Channel, Escon, SMPTE 259
- Gigabit Ethernet/Fast Ethernet
- Proprietary architecture up to 1.3Gbps

## BLOCK DIAGRAM

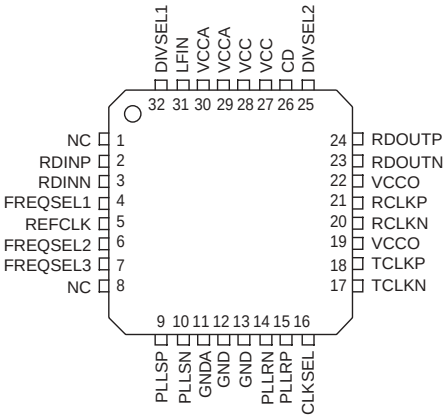



AnyRate is a registered trademark of Micrel, Inc.

## PACKAGE/ORDERING INFORMATION




**28-Pin SOIC (Z28-1)**




**32-Pin EPAD TQFP (H32-1)**

## Ordering Information

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|---|---|---|---|---|
| SY87701ALZI | Z28-1 | Industrial | SY87701ALZI | Sn-Pb |
| SY87701ALHI | H32-1 | Industrial | SY87701ALHI | Sn-Pb |
| SY87701ALZG | Z28-1 | Industrial | SY87701ALZG with Pb-Free bar-line indicator | Pb-Free NiPdAu |
| SY87701ALHG(1) | H32-1 | Industrial | SY87701ALHG with Pb-Free bar-line indicator | Pb-Free NiPdAu |

**Note:**

1. Pb-Free package recommended for new designs.

## PIN DESCRIPTIONS

| Pin Number SOIC | Pin Number TQFP | Pin Name | Pin Function |
|---|---|---|---|
| 4<br>5 | 2<br>3 | RDINP<br>RDINN | Serial Data Input (Differential PECL): These built-in line receiver inputs are connected to the differential receive serial data stream. An internal receive PLL recovers the embedded clock (RCLK) and data (RDOUT) information. The incoming data rate can be within one of eight frequency ranges depending on the state of the FREQSEL pins. See “Frequency Selection” table. |
| 7 | 5 | REFCLK | Reference Clock (TTL Inputs): This input is used as the reference for the internal frequency synthesizer and the “training” frequency for the receiver PLL to keep it centered in the absence of data coming in on the RDIN inputs. |
| 27 | 26 | CD | Carrier Detect (PECL Input): This input controls the recovery function of the Receive PLL and can be driven by the carrier detect output of optical modules or from external transition detection circuitry. When this input is HIGH the input data stream (RDIN) is recovered normally by the Receive PLL. When this input is LOW the data on the inputs RDIN will be internally forced to a constant LOW, the data outputs RDOUT will remain LOW, the Link Fault Indicator output LFIN forced LOW and the clock recovery PLL forced to look onto the clock frequency generated from REFCLK. |
| 6<br>8<br>9 | 4<br>6<br>7 | FREQSEL1<br>FREQSEL2<br>FREQSEL3 | Frequency Select (TTL Inputs): These inputs select the output clock frequency range as shown in the “Frequency Selection” table. |
| 3<br>26 | 32<br>25 | DIVSEL1<br>DIVSEL2 | Divider Select (TTL Inputs): These inputs select the ratio between the output clock frequency (RCLK/TCLK) and the REFCLK input frequency as shown in the “Reference Frequency Selection” table. |
| 17 | 16 | CLKSEL | Clock Select (TTL Inputs): This input is used to select either the recovered clock of the receiver PLL (CLKSEL = HIGH) or the clock of the frequency synthesizer (CLKSEL = LOW) to the TCLK outputs. |
| 2 | 31 | LFIN | Link Fault Indicator (TTL Output): This output indicates the status of the input data stream RDIN. Active HIGH signal is indicating when the internal clock recovery PLL has locked onto the incoming data stream. LFIN will go HIGH if CD is HIGH and RDIN is within the frequency range of the Receive PLL (1000ppm). |
| 25<br>24 | 24<br>23 | RDOUTP<br>RDOUTN | Receive Data Output (Differential PECL): These ECL 100k outputs represent the recovered data from the input data stream (RDIN). This recovered data is specified against the rising edge of RCLK. These outputs must be terminated with 50Ω to $V_{CC}$–2 or equivalent. Thhis applies even if these outputs are not used. |
| 22<br>21 | 21<br>20 | RCLKP<br>RCLKN | Clock Output (Differential PECL): These ECL 100k outputs represent the recovered clock used to sample the recovered data (RDOUT). |
| 19<br>18 | 18<br>17 | TCLKP<br>TCLKN | Clock Output (Differential PECL): These ECL 100k outputs represent either the recovered clock (CLKSEL = HIGH) used to sample the recovered data (RDOUT) or the transmit clock of the frequency synthesizer (CLKSEL = LOW). These outputs must be terminated with 50Ω to $V_{CC}$–2 or equivalent. This applies even if these outputs are not used. |
| 11<br>12 | 9<br>10 | PLLSP<br>PLLSN | Clock Synthesis PLL Loop Filter. External loop filter pins for the clock synthesis PLL. |
| 16<br>15 | 15<br>14 | PLLRP<br>PLLRN | Clock Recovery PLL Loop Filter. External loop filter pins for the receiver PLL. |
| 28 | 27, 28, | $V_{CC}$ | Supply Voltage(1) |
| 1 | 29, 30 | $V_{CCA}$ | Analog Supply Voltage(1) |
| 20, 23 | 19, 22 | $V_{CCO}$ | Output Supply Voltage(1) |
| 13, 14 | 12, 13 | GND | Ground |
| 10 | 1, 8 | NC | No Connect |
| 13 | 11 | GNDA | Analog Ground |

**Note:**

1. $V_{CC}$, $V_{CCA}$, $V_{CCO}$ must be the same value.

## FUNCTIONAL DESCRIPTION

### Clock Recovery

Clock Recovery, as shown in the block diagram, generates a clock that is at the same frequency as the incoming data bit rate at the Serial Data input. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency detector. Output pulses from the detector indicate the required direction of phase correction. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Frequency stability without incoming data is guaranteed by an alternate reference input (REFCLK) that the PLL locks onto when data is lost. If the Frequency of the incoming signal varies by greater than approximately 1000ppm with respect to the synthesizer frequency, then PLL will be declared out of lock, and the PLL will lock to the reference clock.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. This transfer function yields a 30μs data stream of continuous 1's or 0's for random incoming NRZ data.

The total loop dynamics of the clock recovery PLL provides jitter tolerance which is better than the specified tolerance in GR-253-CORE.

### Lock Detect

The SY87701AL contains a link fault indication circuit that monitors the integrity of the serial data input. If the recovered serial data from RDIN is at the correct data rate (within 1000ppm of the synthesizer frequency), the Link Fault Indicator (LFIN) output will be asserted HIGH indicating an in-lock condition and will remain HIGH as long as this condition is met.

In the event that the recovered serial data is not at the correct data rate (greater than 1000ppm difference from the synthesizer frequency), then LFIN output will go LOW indicating an out-of-lock condition. This condition will force the Clock and Data Recovery PLL (CDR) to lock onto the synthesizer frequency until it is within the correct frequency range (less than 1000ppm difference from the synthesizer frequency). Once the CDR is within the correct frequency range it will again lock onto the RDIN input.

During the interval when the CDR is not locked onto the RDIN input, the LFIN output will not be a static LOW, but will be changing.

## CHARACTERISTICS

### Performance

The SY87701AL PLL complies with the jitter specifications proposed for SONET/SDH equipment defined by the Bellcore Specifications: GR-253-CORE, Issue 2, December 1995 and ITU-T Recommendations: G.958 document, when used with differential inputs and outputs.

### Input Jitter Tolerance

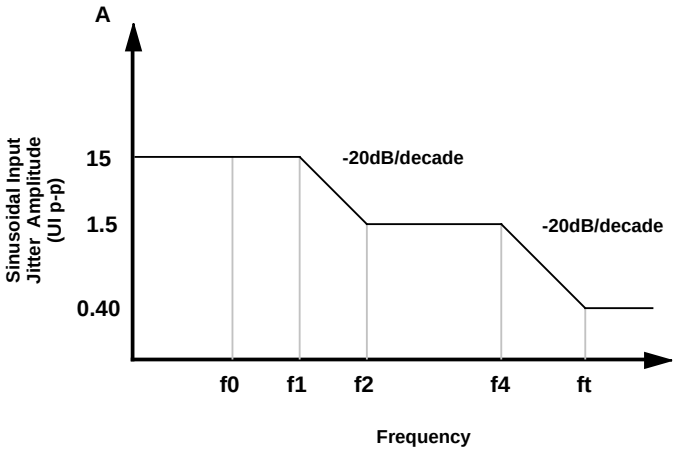
Input jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1dB optical/electrical power penalty. SONET input jitter tolerance requirement condition is the input jitter amplitude which causes an equivalent of 1dB power penalty.

### Jitter Transfer

Jitter transfer function is defined as the ratio of jitter on the output OC-N/STS-N signal to the jitter applied on the input OC-N/STS-N signal versus frequency. Jitter transfer requirements are shown in Figure 2.

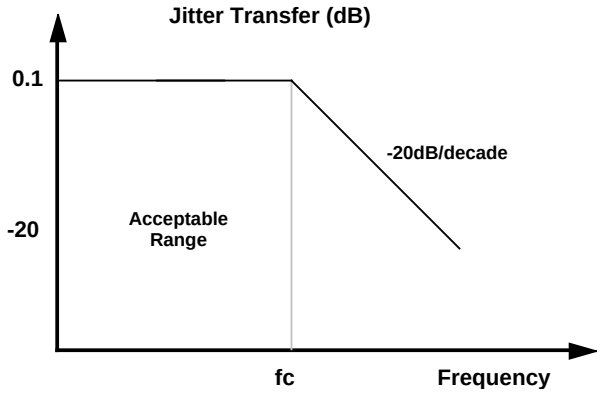
### Jitter Generation

The jitter of the serial clock and serial data outputs shall not exceed .01 U.I. rms when a serial data input with no jitter is presented to the serial data inputs.




| OC/STS-N Level | f0 (Hz) | f1 (Hz) | f2 (Hz) | f3 (kHz) | ft (kHz) |
|---|---|---|---|---|---|
| 3 | 10 | 30 | 300 | 6.5 | 65 |
| 12 | 10 | 30 | 300 | 25 | 250 |

**Figure 1. Input Jitter Tolerance**




| OC/STS-N Level | fc (kHz) | P (dB) |
|---|---|---|
| 3 | 130 | 0.1 |
| 12 | 225 | 0.1 |

**Figure 2. Jitter Transfer**

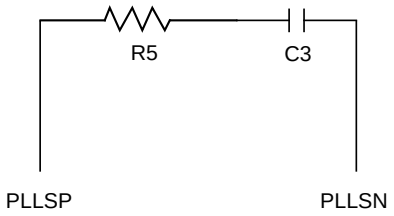
## FREQUENCY SELECTION TABLE

| FREQSEL1 | FREQSEL2 | FREQSEL3 | $f_{VCO}/f_{RCLK}$ | $f_{RCLK}$ Data Rates (Mbps) |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 650 - 1300 |
| 0 | 0 | 1 | 2 | 325 - 650 |
| 0 | 1 | 0 | 4 | 163 - 325 |
| 0 | 1 | 1 | 6 | 109 - 216 |
| 1 | 0 | 0 | 8 | 82 - 162 |
| 1 | 0 | 1 | 12 | 55 - 108 |
| 1 | 1 | 0 | 16 | 41 - 81 |
| 1 | 1 | 1 | 24 | 28 - 54 |

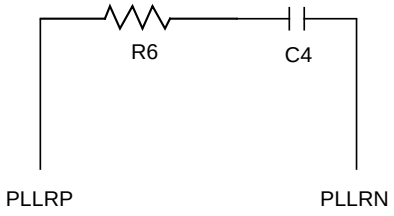
## REFERENCE FREQUENCY SELECTION

| DIVSEL1 | DIVSEL2 | $f_{RCLK}/f_{REFCLK}$ |
|---|---|---|
| 0 | 0 | 8 |
| 0 | 1 | 10 |
| 1 | 0 | 16 |
| 1 | 1 | 20 |

## LOOP FILTER COMPONENTS(1)




**Wide Range**
R5 = 350Ω
C3 = 1.0μF (X7R Dielectric)




**Wide Range**
R6 = 680Ω
C4 = 1.0μF (X7R Dielectric)

**Note:**
1. Suggested Values. Values may vary for different applications.

## Absolute Maximum Ratings[1]

Supply Voltage ($V_{CC}$) ..... –0.5V to +4.0V
Input Voltage ($V_{IN}$) ..... –0.5V to $V_{CC}$
Output Current ($I_{OUT}$)
  Continuous ..... 50mA
  Surge ..... 100mA
Lead Temperature (soldering, 20 sec.) ..... 260°C
Storage Temperature ($T_S$) ..... –65°C to +150°C

## Operating Ratings[2]

Supply Voltage ($V_{CC}$) ..... +3.15V to +3.45V
Ambient Temperature ($T_A$) ..... –40°C to +85°C
Package Thermal Resistance[3]
  SOIC ($\theta_{JA}$)[4] ..... 80°C/W
  EPAD TQFP ($\theta_{JA}$)[5]
    0lfpm airflow ..... 27.6°C/W
    200lfpm airflow ..... 22.6°C/W
    500lfpm airflow ..... 20.7°C/W

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | | 3.15 | 3.3 | 3.45 | V |
| $I_{CC}$ | Power Supply Current | | | 120 | 160 | mA |

## PECL 100K DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = V_{CCA}$ = 3.3V ±5%; $T_A$ = –40°C to +85°C; unless noted.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | $V_{CC}$ –1.165 | | $V_{CC}$ –0.880 | V |
| $V_{IL}$ | Input LOW Voltage | | $V_{CC}$ –1.810 | | $V_{CC}$ –1.475 | V |
| $V_{OH}$ | Output HIGH Voltage | 50Ω to $V_{CC}$ –2V | $V_{CC}$ –1.075 | | $V_{CC}$ –0.830 | V |
| $V_{OL}$ | Output LOW Voltage | 50Ω to $V_{CC}$ –2V | $V_{CC}$ –1.860 | | $V_{CC}$ –1.570 | V |
| $I_{IL}$ | Input LOW Current | $V_{IN} = V_{IL}$(min) | 0.5 | | | µA |

## TTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = V_{CCO} = V_{CCA}$ = 3.3V ±5%; $T_A$ = –40°C to +85°C; unless noted.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –0.4mA | 2.0 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 4mA | | | 0.5 | V |
| $I_{IH}$ | Input HIGH Current | $V_{IN} = 2.7V$, $V_{CC}$ = max.<br>$V_{IN} = V_{CC}$, $V_{CC}$ = max. | –175 | | <br>+100 | µA<br>µA |
| $I_{IL}$ | Input LOW Current | $V_{IN} = 0.5V$, $V_{CC}$ = max. | –300 | | | µA |
| $I_{OS}$ | Output Short Circuit Current | $V_{OUT}$ = 0V (maximum 1 sec) | –15 | | –100 | mA |

**Notes:**

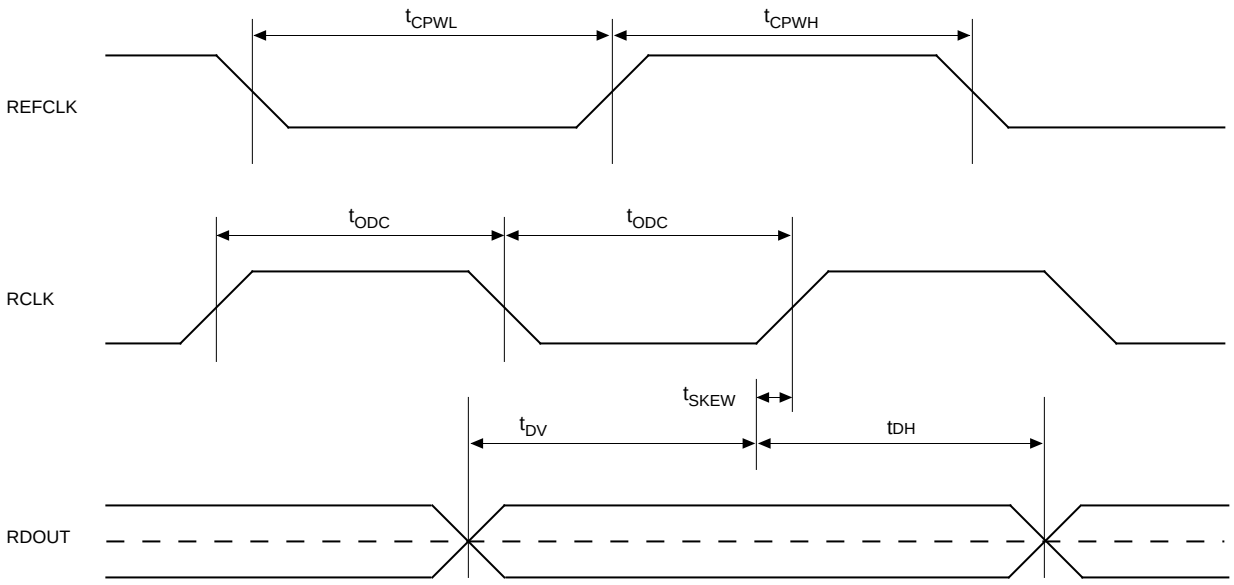
1. Permanent device damage may occur if “Absolute Maximum Ratings” are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to “Absolute Maximum Ratings” conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Airflow of 500lfpm recommended for 28-pin SOIC.
4. 28-pin SOIC package is NOT recommended for new designs.
5. Using JEDEC standard test boards with die attach pad soldered to PCB. See www.amkor.com for additional package details.

## AC ELECTRICAL CHARACTERISTICS

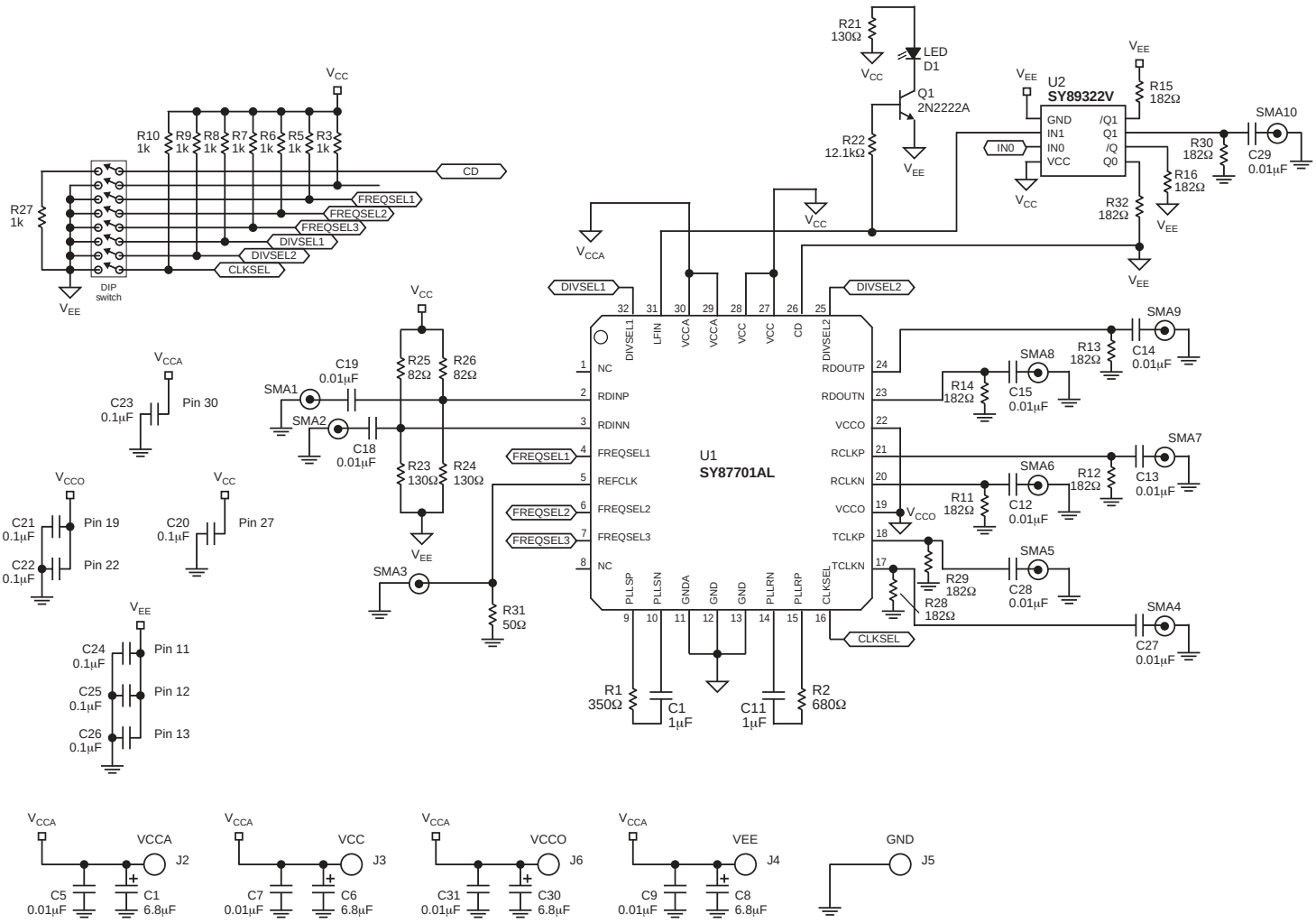
$V_{CC} = V_{CCO} = V_{CCA} = 3.3V \pm 5\%$; $T_A = -40°C$ to $+85°C$; unless noted.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{VCO}$ | VCO Center Frequency | $f_{REFCLK}$ × Byte Rate | 625 | | 1300 | MHz |
| $\Delta f_{VCO}$ | VCO Center Frequency Tolerance | Nominal | | 5 | | % |
| $t_{ACQ}$ | Acquisition Lock Time | | | | 15 | µs |
| $t_{CPWH}$ | REFCLK Pulse Width HIGH | | 3 | | | ns |
| $t_{CPWL}$ | REFCLK Pulse Width LOW | | 3 | | | ns |
| $t_{ir}$ | REFCLK Input Rise Time | | | 0.5 | 2 | ns |
| $t_{ODC}$ | Output Duty Cycle (RCLK/TCLK) | | 45 | | 55 | % of UI |
| $t_r$, $t_f$ | ECL Output Rise/Fall Time (20% to 80%) | 50Ω to $V_{CC}$ –2V | 100 | | 500 | ps |
| $t_{SKEW}$ | Recovered Clock Skew | | –200 | | +200 | ps |
| $t_{DV}$ | Data Valid | | $1/(2 \times f_{RCLK}) - 200$ | | | ps |
| $t_{DH}$ | Data Hold | | $1/(2 \times f_{RCLK}) - 200$ | | | ps |

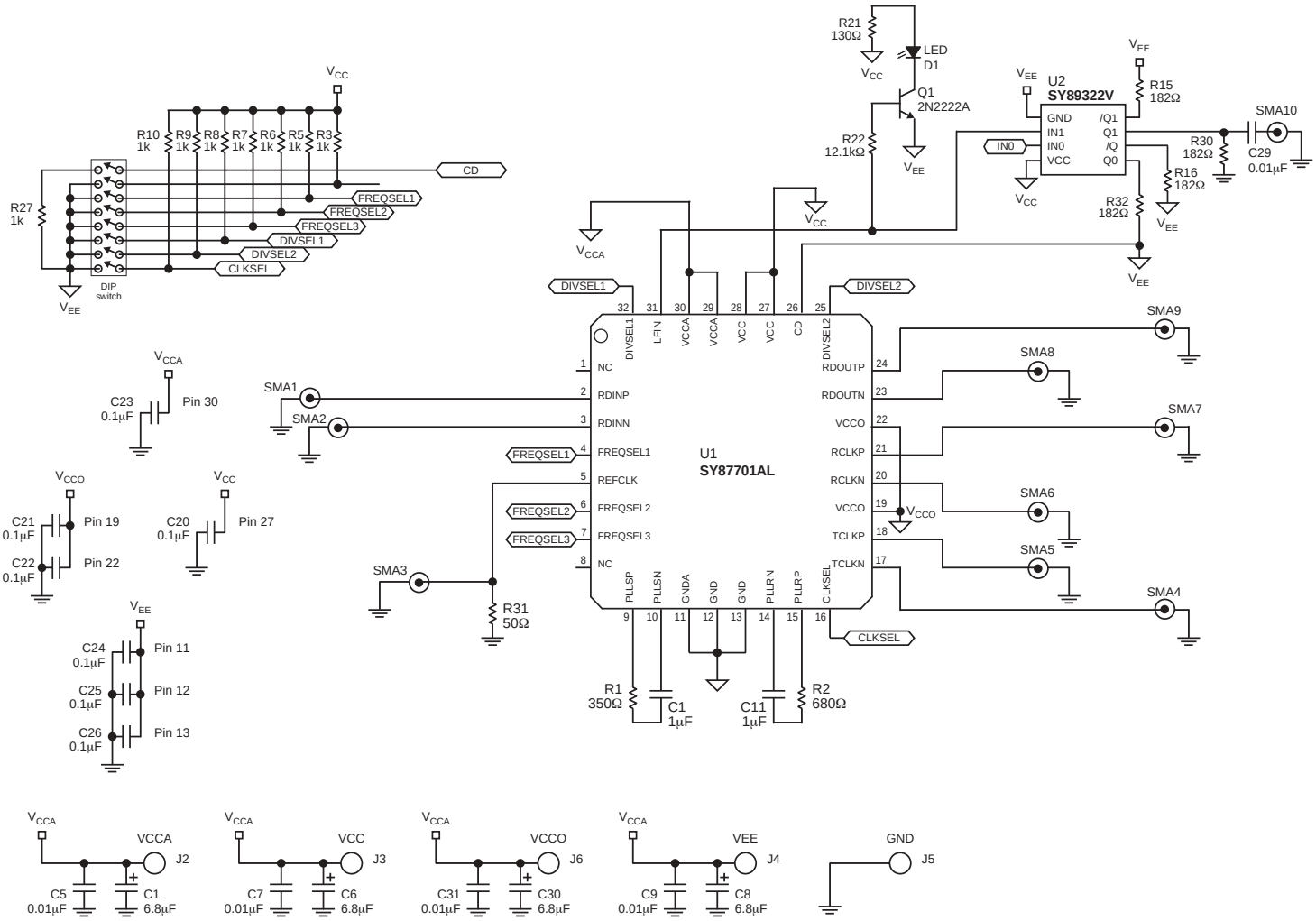
## TIMING WAVEFORMS



## APPLICATION EXAMPLE AC-COUPLED I/O



## APPLICATION EXAMPLE DC-COUPLED I/O



## BILL OF MATERIALS (AC-COUPLED)

| Item | Part Number | Manufacturer | Description | Qty |
|---|---|---|---|---|
| C6 | 293D685X0025B2T | Vishay[1] | 6.8µF, 25V, Tantalum Capacitor, Size B | 1 |
| C7 | VJ1206Y103JXJAT | Vishay[1] | 0.01µF, X7R, Ceramic Capacitor, Size 1206 | 1 |
| C10, C11 | VJ0603Y105JXJAT | Vishay[1] | 1.0µF, X7R, Ceramic Capacitor, Size 0603 | 2 |
| C12, C13, C14, C15, C18, C19, C27, C28 | VJ0402Y104JXJAT | Vishay[1] | 0.1µF, X7R, Ceramic Capacitor, Size 0402 | 8 |
| C20, C21, C22, C23, C24, C25, C26 | VJ0402Y104JXJAT | Vishay[1] | 0.01µF, X7R, Ceramic Capacitor, Size 0603 | 7 |
| D1 | P301-ND | Panasonic[2] | LED, T-1 3/4, Red Clear | 1 |
| D2 | P300-ND/P301-ND | Vishay[1] | T-1 3/4 Red LED | 1 |
| J2, J3, J4, J6 | 111-0702-001 | Johnson Components[3] | Red, Insulated Thumb Nut Binding Post (Jumped together) | 4 |
| J5 | 111-0703-001 | Johnson Components[3] | Black, Insulated Thumb Nut Binding Post, GND (Jumped to $V_{EE}$) | 1 |
| Q1 | 459-2598-5-ND | | 2N2222A Transistor | 1 |
| R1 | CRCW04023500F | Vishay[1] | 350Ω Resistor, 2%, Size 0402 | 1 |
| R2 | CRCW04026800F | Vishay[1] | 680Ω Resistor, 2%, Size 0402 | 1 |
| R3, R4, R5, R6, R7, R8, R9, R10 | CRCW04021001F | Vishay[1] | 1kΩ Pull-up Resistors, 2%, Size 1206 | 8 |
| R11, R12, R13, R14, R15, R16, R28, R29, R30, R32 | CRCW04021820F | Vishay[1] | 182Ω Resistor, 2%, Size 0402 | 10 |
| R21 | CRCW06031300F | Vishay[1] | 130Ω Resistor, 2%, Size 0603 | 1 |
| R22 | CRCW04021820F | Vishay[1] | 12.1kΩ Resistor, 2%, Size 1206 | 1 |
| R23, R24 | CRCW04022825F | Vishay[1] | 82Ω Resistor, 2%, Size 0402 | 2 |
| R25, 26 | CRCW04021300F | Vishay[1] | 130Ω Resistor, 2%, Size 0402 | 2 |
| R27 | CRCW040200R0F | Vishay[1] | 0Ω Resistor, 2%, Size 0402 | 1 |
| R31 | CRCW04025000F | Vishay[1] | 50Ω Resistor, 2%, Size 0402 | 1 |
| SMA1-SMA10 | 142-0701-851 | Johnson Components[1] | End Launch SMA Jack | 10 |
| SP1-SP6 | | | Solder Jumper Option | 6 |
| SW1 | CT2068-ND | | 8-Position, Top Actuated Slide Dip Switch | 1 |
| U1 | **SY87700/01** | **Micrel**[4] | 3.3V 28Mbps to 1.3Gbps AnyRate® Clock and Data Recovery | 1 |
| U2 | **SY89322V** | **Micrel**[4] | 3.3/5V Dual LVTTL/LVCMOS-to-Differential LVPECL Translator | 1 |

**Notes:**

1. Vishay: www.vishay.com.
2. Panasonic: www.panasonic.com.
3. Johnson Components: www.johnson-components.com.
4. **Micrel, Inc. www.micrel.com.**

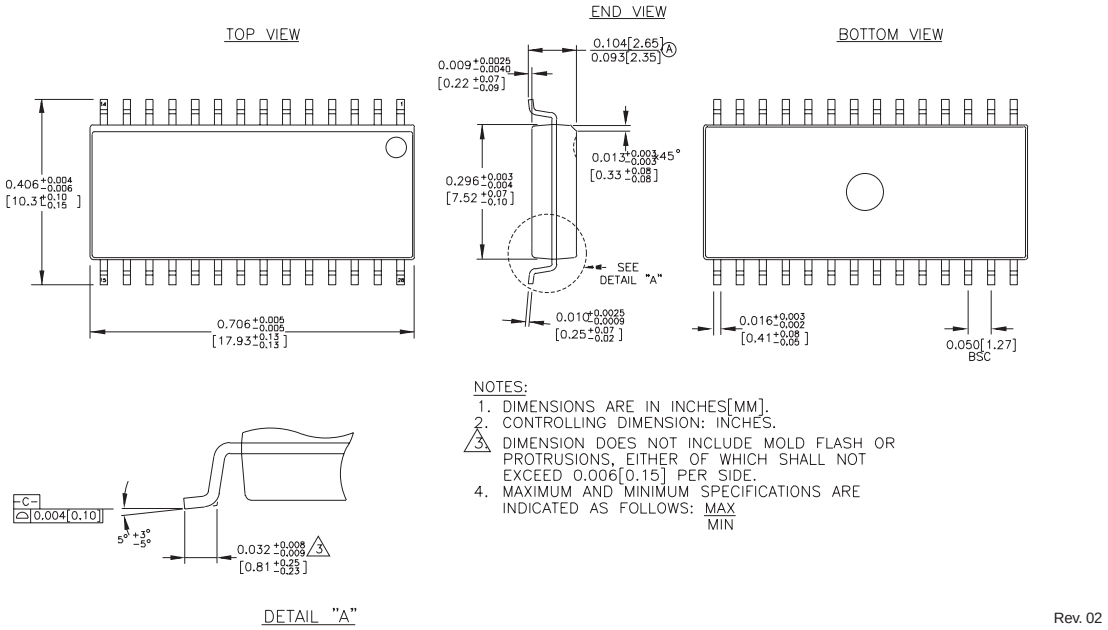
## BILL OF MATERIALS (DC-COUPLED)

| Item | Part Number | Manufacturer | Description | Qty |
|---|---|---|---|---|
| C6 | 293D685X0025B2T | Vishay[1] | 6.8μF, 25V, Tantalum Capacitor, Size B | 1 |
| C7 | VJ1206Y103JXJAT | Vishay[1] | 0.01μF, X7R, Ceramic Capacitor, Size 1206 | 1 |
| C10, C11 | VJ0603Y105JXJAT | Vishay[1] | 1.0μF, X7R, Ceramic Capacitor, Size 0603 | 2 |
| C12, C13, C14, C15, C18, C19, C27, C28 | VJ0402Y104JXJAT | Vishay[1] | 0.1μF, X7R, Ceramic Capacitor, Size 0402 | 8 |
| C20, C21, C22, C23, C24, C25, C26 | VJ0402Y104JXJAT | Vishay[1] | 0.01μF, X7R, Ceramic Capacitor, Size 0603 | 7 |
| D1 | P301-ND | Panasonic[2] | LED, T-1 3/4, Red Clear | 1 |
| D2 | P300-ND/P301-ND | Vishay[1] | T-1 3/4 Red LED | 1 |
| J2, J3, J4, J6 | 111-0702-001 | Johnson Components[3] | Red, Insulated Thumb Nut Binding Post (Jumped together) | 4 |
| J5 | 111-0703-001 | Johnson Components[3] | Black, Insulated Thumb Nut Binding Post, GND (Jumped to $V_{EE}$) | 1 |
| Q1 | 459-2598-5-ND | | 2N2222A Transistor | 1 |
| R1 | CRCW04023500F | Vishay[1] | 350Ω Resistor, 2%, Size 0402 | 1 |
| R2 | CRCW04026800F | Vishay[1] | 680Ω Resistor, 2%, Size 0402 | 1 |
| R3, R4, R5, R6, R7, R8, R9, R10 | CRCW04021001F | Vishay[1] | 1kΩ Pull-up Resistors, 2%, Size 1206 | 8 |
| R15, R16, R30, R32 | CRCW04021820F | Vishay[1] | 182Ω Resistor, 2%, Size 0402 | 4 |
| R21 | CRCW06031300F | Vishay[1] | 130Ω Resistor, 2%, Size 0603 | 1 |
| R22 | CRCW04021820F | Vishay[1] | 12.1kΩ Resistor, 2%, Size 1206 | 1 |
| R27 | CRCW040200R0F | Vishay[1] | 0Ω Resistor, 2%, Size 0402 | 1 |
| R31 | CRCW04025000F | Vishay[1] | 50Ω Resistor, 2%, Size 0402 | 1 |
| SMA1-SMA10 | 142-0701-851 | Johnson Components[1] | End Launch SMA Jack | 10 |
| SP1-SP6 | | | Solder Jumper Option | 6 |
| SW1 | CT2068-ND | | 8-Position, Top Actuated Slide Dip Switch | 1 |
| U1 | **SY87700/01** | **Micrel**[4] | 3.3V 28Mbps to 1.3Gbps AnyRate® Clock and Data Recovery | 1 |
| U2 | **SY89322V** | **Micrel**[4] | 3.3/5V Dual LVTTL/LVCMOS-to-Differential LVPECL Translator | 1 |

**Notes:**

1. Vishay: www.vishay.com.
2. Panasonic: www.panasonic.com.
3. Johnson Components: www.johnson-components.com.
4. **Micrel, Inc. www.micrel.com.**

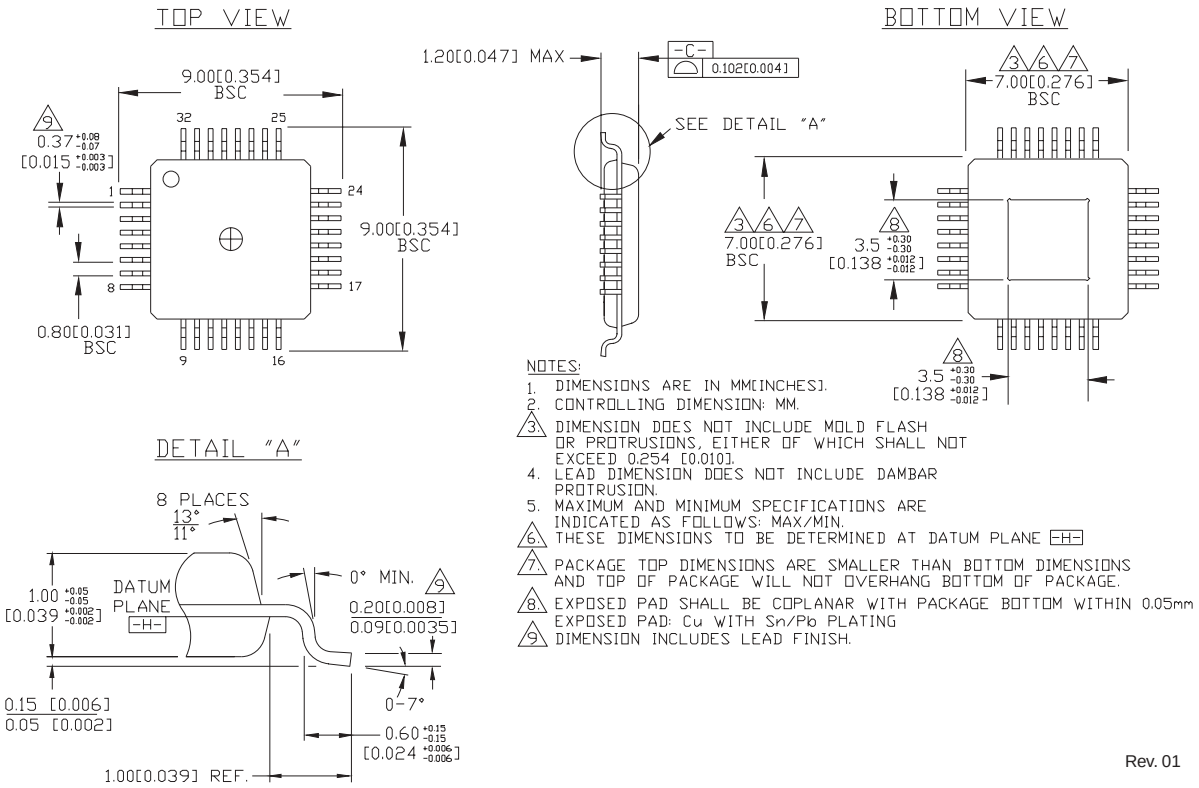
## 28-PIN SOIC .300" WIDE (Z28-1)



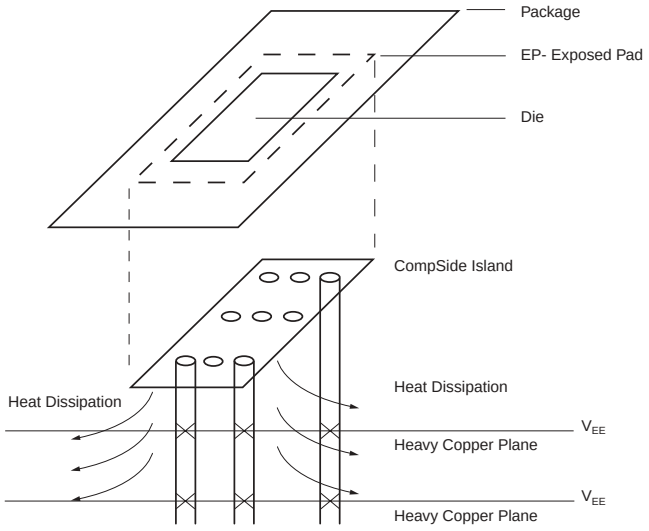

**Note:**

The 28-pin SOIC package is NOT recommended for new designs.

## 32-PIN EPAD TQFP (DIE UP) (H32-1)




Rev. 01




**PCB Thermal Consideration for 32-Pin EPAD-TQFP Package**

# APPENDIX A

## Layout and General Suggestions

1. Establish controlled impedance stripline, microstrip, or co-planar construction techniques.
2. Signal paths should have, approximately, the same width as the device pads.
3. All differential paths are critical timing paths, where skew should be matched to within ±10ps.
4. Signal trace impedance should not vary more than ±5%. If in doubt, perform TDR analysis of all high-speed signal traces.
5. Maintain compact filter networks as close to filter pins as possible. Provide ground plane relief under filter path to reduce stray capacitance. Be careful of crosstalk coupling into the filter network.
6. Maintain low jitter on the REFCLK input. Isolate the XTAL oscillator from power supply noise by adequately decoupling. Keep XTAL oscillator close to device, and minimize capacitive coupling from adjacent signals.
7. Higher speed operation may require use of fundamental-tone (third-overtone typically have more jitter) crystal based oscillator for optimum performance. Evaluate and compare candidates by measuring TXCLK jitter.
8. All unused outputs must be terminated. To conserve power, unused PECL outputs can be terminated with a 1kΩ resistor to $V_{EE}$.

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB http://www.micrel.com