3V LVTTL-TO-DIFFERENTIAL LVPECL AND DIFFERENTIAL LVPECL-TO-LVTTL TRANSLATOR

Precision Edge®
SY89328L

FEATURES

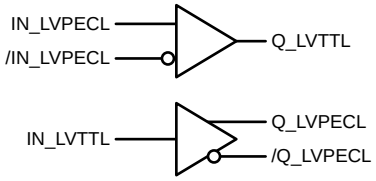
- **3.3V ±10% power supply**
- **Guaranteed AC parameters over temperature:**
  f_{MAX} > 275MHz (LVTTL)
- **< 2ns LVPECL-to-LVTTL propagation delay**
- **< 600ps LVTTL-to-LVPECL propagation delay**
- **Internal 75kΩ input pull-up and pull-down resistors**
- **Industrial temperature range: –40°C to +85°C**
- **Available in ultra-small 8-pin MLF™ (2mm × 2mm) package**

Precision Edge®

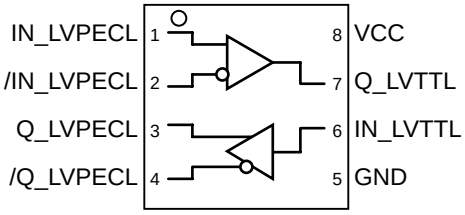
DESCRIPTION

The SY89328L is a differential LVPECL-to-LVTTL translator and an LVTTL-to-differential LVPECL translator in a single package. Because LVPECL (Positive ECL) levels are used, only +3.3V and ground are required. The SY89328L is functionally equivalent to the SY100EPT28L, but in an ultra-small 8-lead MLF™ package that features a 70% smaller footprint. This ultra-small package and the dual translation design of the SY89328L make it ideal for applications that are sending and receiving signals across a backplane.

BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION



8-Pin MLF™
Ultra-Small Outline (2mm × 2mm)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89328LMITR	MLF-8	Industrial	HEP28	Sn-Pb
SY89328LMGTR	MLF-8	Industrial	HEP28 with Pb-Free bar-line indicator	Pb-Free NiPdAu

PIN DESCRIPTION

Pin Number	Pin Name	Type	Pin Function
1, 2	IN_LVPECL, /IN_LVPECL	100k ECL Input	Differential LVPECL Input: Includes internal 75kΩ pull-down resistor on internal 75kΩ pull-up and pull-down resistors on /IN. See “Input Interface Applications” section for single-ended inputs.
7	Q_LVTTL	LVTTL Output	Single-ended LVTTL Output: Translated from LVPECL input. Q_LVTTL output will default LOW with IN_LVPECL and /IN_LVPECL inputs left open.
6	IN_LVTTL	LVTTL Input	Single-ended LVTTL Input.
3, 4	Q_LVPECL, /Q_LVPECL	100k ECL Output	Differential LVPECL Output: Translated from LVTTL input. See “Output Interface Applications” section for recommendations on terminations.
8	VCC	VCC Power	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors.
5	GND, Exposed Pad	Ground	GND and exposed pad must be tied to ground plane.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC}) ..... –0.5V to +3.8V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Input Current
  Source or sink current on IN, /IN ..... ±50mA
Lead Temperature (soldering, 20 sec.) ..... +260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings(Note 2)

Supply Voltage (V_{CC}) ..... 3.0V to 3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance, **Note 3**
MLF™ (θ_{JA})
  Still-Air ..... 93°C/W
  500lfpm ..... 87°C/W
MLF™ (Ψ_{JB})
  Junction-to-Board ..... 60°C/W

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.

DC ELECTRICAL CHARACTERISTICS(Note 4)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		3.0	3.3	3.6	V
I_{CC}	Power Supply Current	Max V_{CC}, No Load		22	40	mA

LVPECL DC ELECTRICAL CHARACTERISTICS(Note 4)

V_{CC} = +3.3V±10% and V_{EE} = 0V; R_L = 50Ω to V_{CC}–2V; T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage		V_{CC}–1.145	V_{CC}–1.020	V_{CC}–0.895	V
V_{OL}	Output LOW Voltage		V_{CC}–1.945	V_{CC}–1.820	V_{CC}–1.695	V
V_{IH}	Input HIGH Voltage		V_{CC}–1.225		V_{CC}–0.880	V
V_{IL}	Input LOW Voltage		V_{CC}–1.945		V_{CC}–1.625	V
V_{CMR}	LVPECL Common Mode Range		1.2		V_{CC}	V
I_{IH}	Input HIGH Current	V_{IN} = 3.46V			150	µA
I_{IL}	Input LOW Current IN		0.5			µA
	/IN		–300			µA

Note 4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

LVTTL DC ELECTRICAL CHARACTERISTICS(Note 5)

V_{CC} = +3.3V±10%; C_L = 20pF, T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	I_{OH} = –3mA	2.0	—	—	V
V_{OL}	Output LOW Voltage	I_{OH} = –24mA	—	—	0.5	V
V_{IH}	Input HIGH Voltage		2.0	—	—	V
V_{IL}	Input LOW Voltage		—	—	0.8	V
V_{IK}	Input Clamp Voltage	I_{IK} = –18mA	—	—	–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7V	—	—	20	µA
		V_{IN} = V_{CC}	—	—	100	µA
I_{IL}	Input LOW Current	V_{IN} = 0.5V	—	—	–0.2	µA
$I_{OUT(SC)}$	LVTTL Output Short-Circuit Current	V_{OUT} = 0V	–275	—	–80	mA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.3V±10%. T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency LVPECL	**Note 6**	700	—	—	MHz
	LVTTL	**Note 7**	275	350	—	MHz
t_{pd}	Propagation Delay IN_LVPECL-to-Q_LVTTL	**Note 7**	1.5	—	2.5	ns
	IN_LVTTL-to-Q_LVPECL	**Note 6**	100	400	600	ps
V_{PP}	LVPECL Input Voltage Swing (Single-Ended)	**Note 8**	100	—	—	mV
t_{DC}	Duty Cycle		45	50	55	%
t_{Jitter}	Cycle-toCycle Jitter	**Note 9**			<1	ps_{RMS}
	Total Jitter	**Note 10**			20	ps_{PP}
t_r, t_f	LVPECL Output Rise/Fall Times (20% to 80%)	At full output swing, **Note 5**	200	—	500	ns
	LVTTL Output Rise/Fall Times (10% to 90%)	At full output swing, **Note 6**	0.5	—	1.0	ns

Note 5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

Note 6. R_L = 50Ω to V_{CC} –2V

Note 7. C_L = 20pF

Note 8. V_{PP} (min) is the minimum input swing for which AC parameters are guaranteed.

Note 9. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$,where T is the time between rising edges of the output signal.

Note 10. Total jitter definition: with an ideal clock input of frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edge will deviate by more than the specified peak-to-peak jitter value.

LVPECL INPUT INTERFACE APPLICATIONS

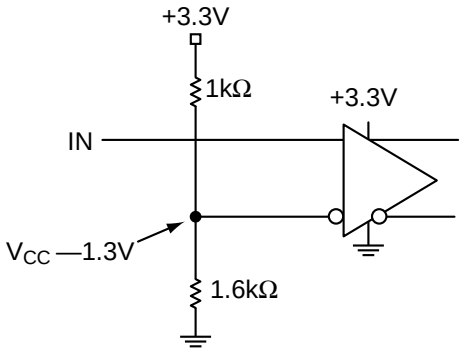


Figure 1. Single-Ended Input (Terminating unused input)

LVPECL OUTPUT INTERFACE APPLICATIONS

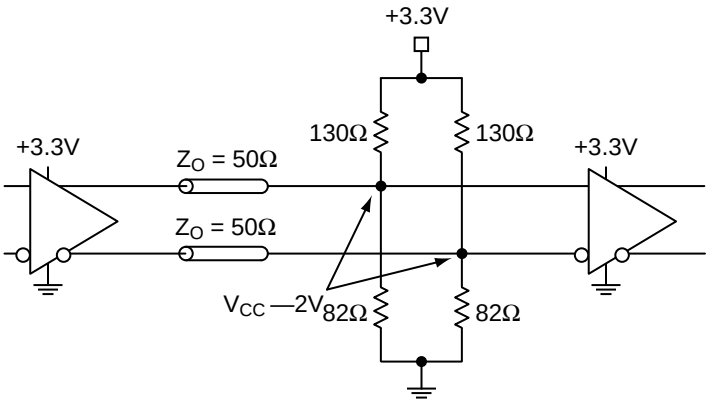


Figure 2a. Parallel Thevenin-Equivalent Termination

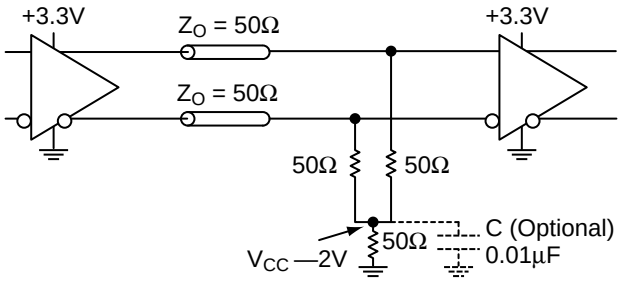


Figure 2b. Three Resistor "Y Termination"

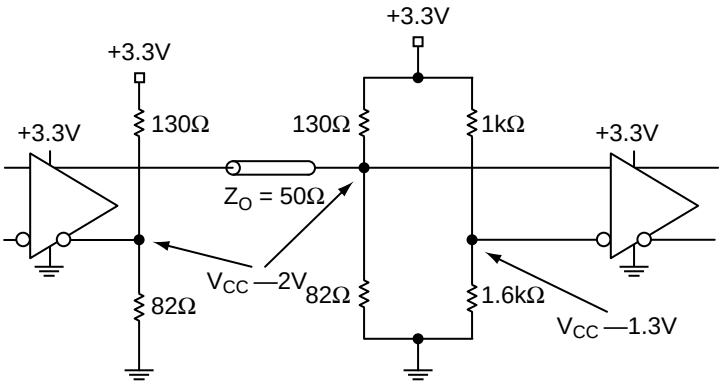
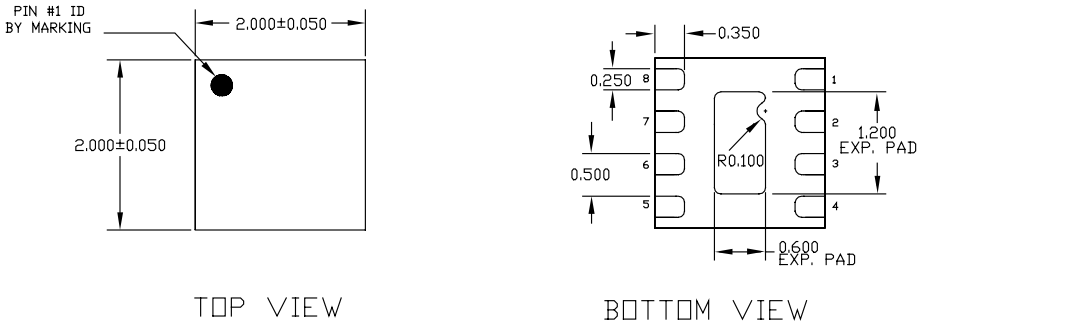
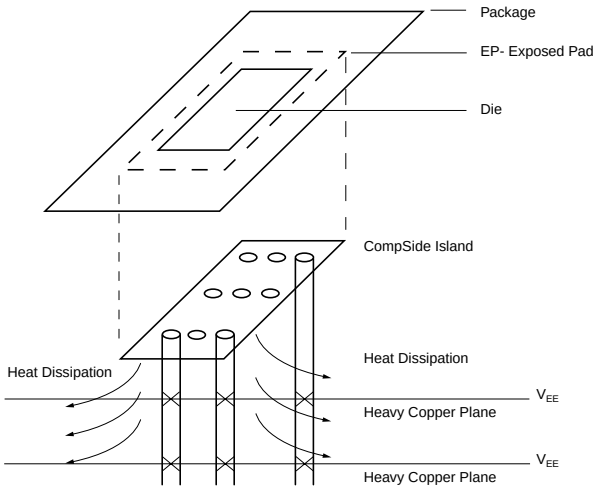


Figure 2c. Terminating Unused I/O

8 LEAD ULTRA-SMALL EPAD-*Micro*LeadFrame™ (MLF-8)





PCB Thermal Consideration for 8-Pin MLF™ Package

Package Notes:

Note 1. Package meets Level 2 qualification.

Note 2. All parts are dry-packaged before shipment.

Note 3. Exposed pads must be soldered to a ground for proper thermal management.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB http://www.micrel.com