SY89229U

1GHz Precision, LVDS ÷3, ÷5 Clock Divider with Fail Safe Input and Internal Termination

Precision Edge®

General Description

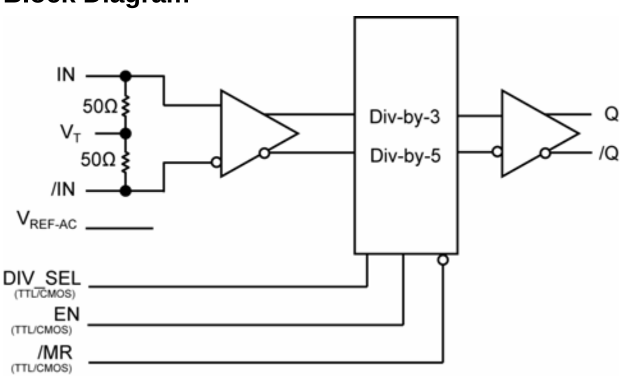
The SY89229U is a precision, low jitter 1GHz ÷3, ÷5 clock divider with an LVDS output. A unique Fail-Safe Input (FSI) protection prevents metastable output conditions when the input clock voltage swing drops significantly below 100mV or input is removed.

The differential input includes Micrel's unique, 3-pin internal termination architecture that allows the input to interface to any differential signal (AC- or DC-coupled) as small as 100mV (200mV$_{PP}$) without any level shifting or termination resistor networks in the signal path. The outputs are 325mV, 100K-compatible LVDS with fast rise/fall times guaranteed to be less than 220ps.

The SY89229U operates from a 2.5V ±5% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. The SY89229U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at: www.micrel.com.

Block Diagram



Features

- Accepts a high-speed input and provides a precision ÷3 and ÷5 sub-rate, LVDS output
- Fail-Safe Input
  – Prevents oscillations when input is invalid
- Guaranteed AC performance over temperature and supply voltage:
  – DC-to >1.0GHz throughput
  – <1500ps Propagation Delay (In-to-Q)
  – <220ps Rise/Fall times
- Ultra-low jitter design:
  – <1ps$_{RMS}$ random jitter
  – <1ps$_{RMS}$ cycle-to-cycle jitter
  – <10ps$_{PP}$ total jitter (clock)
  – <0.7ps$_{RMS}$ MUX crosstalk induced jitter
- Unique patented internal termination and VT pin accepts DC- and AC-coupled inputs (CML, PECL, LVDS)
- Wide input voltage range VCC to GND
- 325mV LVDS output
- 46% to 54% Duty Cycle(÷ 3)
- 47% to 53% Duty Cycle(÷ 5)
- 2.5V ±5% supply voltage
- -40°C to +85°C industrial temperature range
- Available in 16-pin (3mm x 3mm) MLF® package

Applications

- Fail-safe clock protection

Markets

- LAN/WAN
- Enterprise servers
- ATE
- Test and measurement

Precision Edge is a registered trademark of Micrel, Inc.
MLF and *Micro*LeadFrame are registered trademarks of Amkor Technology.

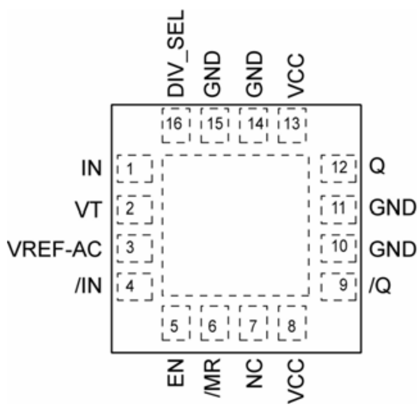
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89229UMG	MLF-16	Industrial	229U with Pb-Free bar-line Indicator	NiPdAu Pb-Free
SY89229UMGTR[2]	MLF-16	Industrial	229U with Pb-Free bar-line Indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals Only.
2. Tape and Reel.

Pin Configuration



16-Pin MLF® (MLF-16)

Pin Description

Pin Number	Pin Name	Pin Function
1, 4	IN, /IN	Differential Input: This input pair is the differential signal input to the device, which accepts AC- or DC-coupled signal as small as 100mV. The input internally terminates to a VT pin through 50□ and has level shifting resistors of 3.72 k□ to VCC. This allows a wide input voltage range from VCC to GND. See Figure 3, Simplified Differential Input Stage for details. Note that this input will default to a valid (either HIGH or LOW) state if left open. See "Input Interface Applications" subsection.
2	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to the VT pin. The VT pin provides a center-tap for the input (IN, /IN) to a termination network for maximum interface flexibility. See "Input Interface Applications" subsection for more details.
3	VREF-AC	Reference Voltage: This output biases to V_{CC}–1.2V. It is used for AC-coupling inputs IN and /IN. Connect VREF-AC directly to the VT pin. Bypass with 0.01µF low ESR capacitor to VCC. Due to limited drive capability, the VREF-AC pin is only intended to drive its respective VT pin. Maximum sink/source current is ±0.5mA. See "Input Interface Applications" subsection.
5	EN	Single-ended Input: This TTL/CMOS-compatible input disables and enables the output. It is internally connected to a 25k□ pull-up resistor and will default to a logic HIGH state if left open. When disabled, Q goes LOW and /Q goes HIGH. EN being synchronous, outputs will be enabled/disabled after a rising and a falling edge of the input clock. V_{TH} = V_{CC}/2.
6	/MR	Single-ended Input: This TTL/CMOS-compatible input, when pulled LOW, asynchronously sets Q output LOW and /Q output HIGH. Note that this input is internally connected to a 25k□ pull-up resistor and will default to logic HIGH state if left open. V_{TH} = V_{CC}/2.
7	NC	No Connect
8, 13	VCC	Positive Power Supply: Bypass with 0.1µF in parallel with 0.01µF low ESR capacitors as close to the V_{CC} pins as possible.
12, 9	Q, /Q	Differential Output: The output swing is typically 325mV. The output must be terminated with 100□ across the pair (Q, /Q). See the "Truth Table" below for the logic function.
10, 11, 14,15	GND, Exposed Pad	Ground: Ground and exposed pad must be connected to a ground plane that is the same potential as the ground pins.
16	DIV_SEL	Single-ended Input: This TTL/CMOS-compatible input selects divide-by-3 when pulled LOW and divide-by-5 when pulled HIGH. Note that this input is internally connected to a 25k□ pull-up resistor and will default to logic HIGH state if left open. V_{TH} = V_{CC}/2.

Truth Table

Inputs			Outputs	
DIV_SEL	**EN**	**/MR**	**Q**	**/Q**
X	X	0	0	1
0	1	1	÷3	÷3
1	1	1	÷5	÷5
X	0	1	0	1

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ....–0.5V to +4.0V
Input Voltage (V_{IN}) ....–0.5V to V_{CC}
LVDS Output Current (I_{OUT})…………………±10mA
Current (V_T)
Source or sink current on V_T pin…………±100mA
Input Current
Source or sink current on (IN, /IN) .... ±50mA
Current(V_{REF-AC})
Source/Sink Current on V_{REF-AC}[4]............ ±0.5mA
Maximum Operating Junction Temperature…..125°C
Lead Temperature (soldering, 20 sec.) ....+260°C
Storage Temperature (T_s)..................–65°C to 150°C

Operating Ratings[2]

Supply Voltage (V_{CC}).................. +2.375V to +2.625V
Ambient Temperature (T_A)................ –40°C to +85°C
Package Thermal Resistance[3]
MLF® (θ_{JA})
Still-Air .... 75°C/W
MLF® (ψ_{JB})
Junction-to-Board…………………………33°C/W

DC Electrical Characteristics[5]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		2.375	2.5	2.625	V
I_{CC}	Power Supply Current	No load, max V_{CC}		52	68	mA
R_{IN}	Input Resistance (IN-to-V_T)		45	50	55	□
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	□
V_{IH}	Input High Voltage (IN, /IN)		1.2		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 2a. Note 6.	0.1		V_{CC}	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN-/IN|	See Figure 2b.	0.2			V
V_{IN_FSI}	Input Voltage Threshold that Triggers FSI			30	100	mV
V_{REF-AC}	Output Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V
V_{T_IN}	Voltage from Input to V_T				1.8	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and ψ_{JB} values are determined for a 4-layer board in still air unless otherwise stated.
4. Due to limited drive capability use for input of the same package only.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. V_{IN} (max) is specified when V_T is floating.

LVDS Outputs DC Electrical Characteristics(7)

V_{CC} = +2.5V ±5%, R_L = 100Ω across the outputs; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage Swing (Q, /Q)	See Figure 2a	250	325		mV
V_{DIFF_OUT}	Differential Output Voltage Swing |Q – /Q|	See Figure 2b	500	650		mV
V_{OCM}	Output Common Mode Voltage (Q, /Q)	See Figure 5a	1.125	1.20	1.275	V
ΔV_{OCM}	Change in Common Mode Voltage (Q, /Q)	See Figure 5b	–50		+50	mV

LVTTL/CMOS DC Electrical Characteristics(7)

V_{CC} = 2.5V ±5%; T_A = –40°C to + 85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		-125		30	µA
I_{IL}	Input LOW Current		-300			µA

Note:

7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics[8]

V_{CC} = 2.5V ±5%; R_L = 100Ω across the outputs; T_A = –40°C to + 85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Input Operating Frequency	V_{OUT} ≥ 200mV	1.0	1.5		GHz
tw	Minimum Pulse Width	IN, /IN	400			ps
t_{pd}	Differential Propagation Delay In-to-Q	100mV < V_{IN} ≤ 200mV, Note 9	900	1150	1500	ps
	In-to-Q	200mV < V_{IN} ≤ 800mV, Note 9	800	1050	1400	ps
	/MR(H-L)-to-Q		350	530	800	ps
t_{RR}	Reset Recovery Time	/MR(L-H)-to-IN	400			ps
t_S EN	Set-up Time EN-to-IN	Note 10	300			ps
t_H EN	Hold Time IN-to-EN	Note 10	800			ps
t_{skew}	Part-to-Part Skew	Note 10			450	ps
t_{JITTER}	Clock Random Jitter	Note 11			1	ps_{RMS}
	Cycle-to-Cycle Jitter	Note 12			1	ps_{RMS}
	Total Jitter	Note 13			10	ps_{PP}
t_r, t_f	Output Rise/Fall Time (20% to 80%)	At full output swing.	100		220	ps
	Output Duty Cycle(÷ **3)**	Duty Cycle(input): 50%; f ≤ 1GHz; Note 14	46		54	%
	Output Duty Cycle(÷ **5)**	Duty Cycle(input): 50%; f ≤ 1GHz; Note 14	47		53	%

Notes:

8. High-frequency AC-parameters are guaranteed by design and characterization.
9. Propagation delay is measured with input t_r, t_f ≤ 300ps (20% to 80%). The propagation delay is function of the rise and fall times at IN. See "Typical Operating Characteristics" for details.
10. Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold do not apply.
11. Random Jitter is measured with a K28.7 character pattern, measured at <f_{MAX}.
12. Cycle-to-Cycle Jitter definition: the variation of periods between adjacent cycles, $T_n – T_{n-1}$ where T is the time between rising edges of the output signal.
13. Total Jitter definition: with an ideal clock input of frequency <f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
14. For Input Duty Cycle different from 50%, see "Output Duty Cycle Equation" in "Functional Description" subsection.

Functional Description

Fail-Safe Input (FSI)

The input includes a special failsafe circuit to sense the amplitude of the input signal and to latch the outputs when there is no input signal present, or when the amplitude of the input signal drops sufficiently below 100mV$_{PK}$ (200mV$_{PP}$), typically 30mV$_{PK}$. Maximum frequency of the SY89229U is limited by the FSI function. Refer to Figure 1b.

Input Clock Failure Case

If the input clock fails to a floating, static, or extremely low signal swing, the FSI function will eliminate a metastable condition and guarantee a stable output signal. No ringing and no undetermined state will occur at the output under these conditions.

Note that the FSI function will not prevent duty cycle distortion in case of a slowly deteriorating (but still toggling) input signal as it nears the FSI threshold (typically 30mV). Due to the FSI function, the propagation delay will depend on rise and fall time of the input signal and on its amplitude. See "Typical Operating Characteristics" for detailed information.

Output Duty Cycle Equation

For a non 50% input, derate the spec by:

For divide by 3:

$$(0.5 - \frac{1+\frac{X}{100}}{3})\ \text{x100, in \%}$$

For divide by 5:

$$(0.5 - \frac{2+\frac{X}{100}}{5})\ \text{x100, in \%}$$

X= input Duty Cycle, in %

Example: if a 45% input duty cycle is applied or X=45, in divide by 3 mode, the spec would expand by 1.67% to 44.3%-55.7%

Enable (EN)

EN is a synchronous TTL/CMOS-compatible input that enables/disables the outputs based on the input to this pin. Internal 25k□ pull-up resistor defaults the input to logic HIGH if left open. Input switching threshold is V$_{CC}$/2.

The Enable function operates as follows:

1. The enable/disable function is synchronous so that the clock outputs will be enabled or disabled following a rising and a falling edge of the input clock when switching from EN = LOW to EN = HIGH.

   However, when switching from EN = HIGH to EN = LOW, the clock outputs will be disabled following an input clock rising edge and an output clock falling edge.

2. The enable/disable function always guarantees the full pulse width at the output before the clock outputs are disabled, non-depending on the divider ratio.

Refer to Figure 1c for examples.

Divider Operation

The divider operation uses both the rising and falling edge of the input clock. For divide by 3, the falling edge of the second input clock cycle will determine the falling edge of the output. For divide by 5, the falling edge of the third input clock cycle. Refer to Figure 1d.

Timing Diagrams

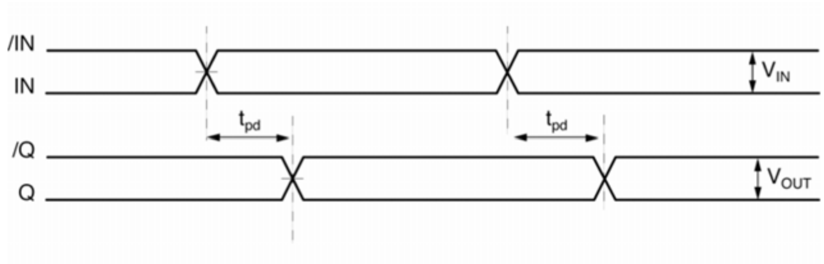


Figure 1a. Propagation Delay

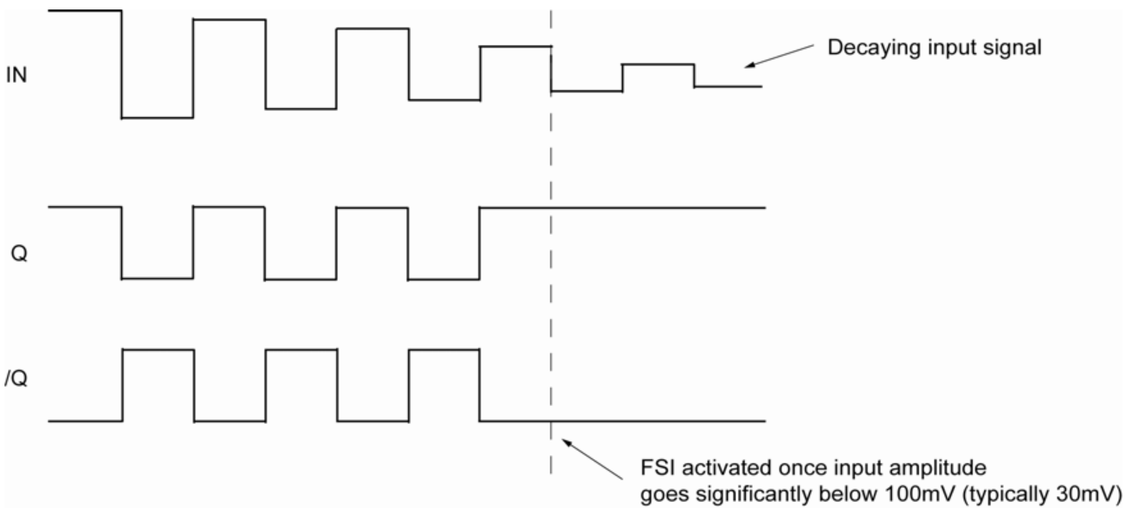


Figure 1b. Fail Safe Feature

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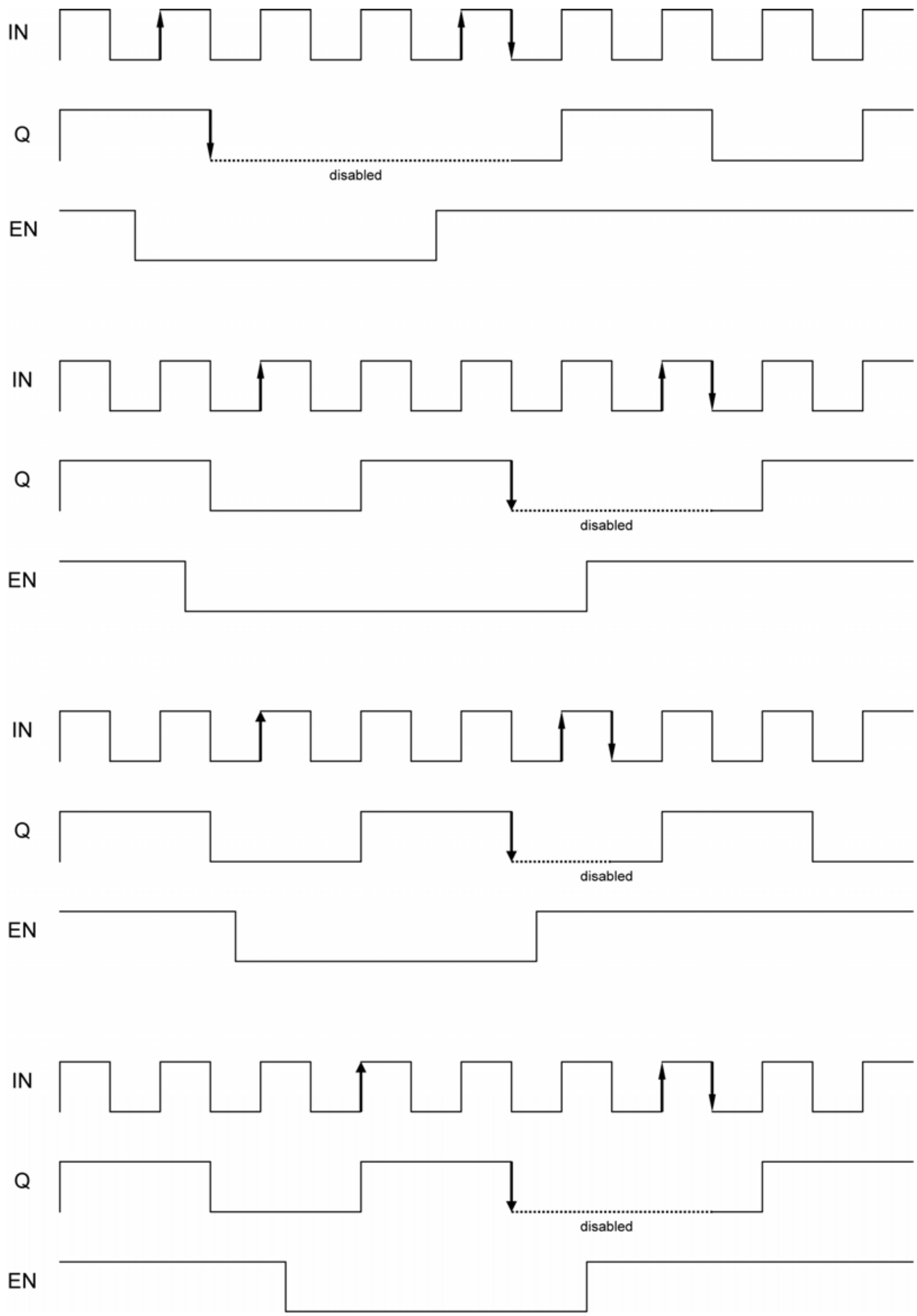

Figure 1c. Enable Output Timing Diagram Examples (Divide by 3)

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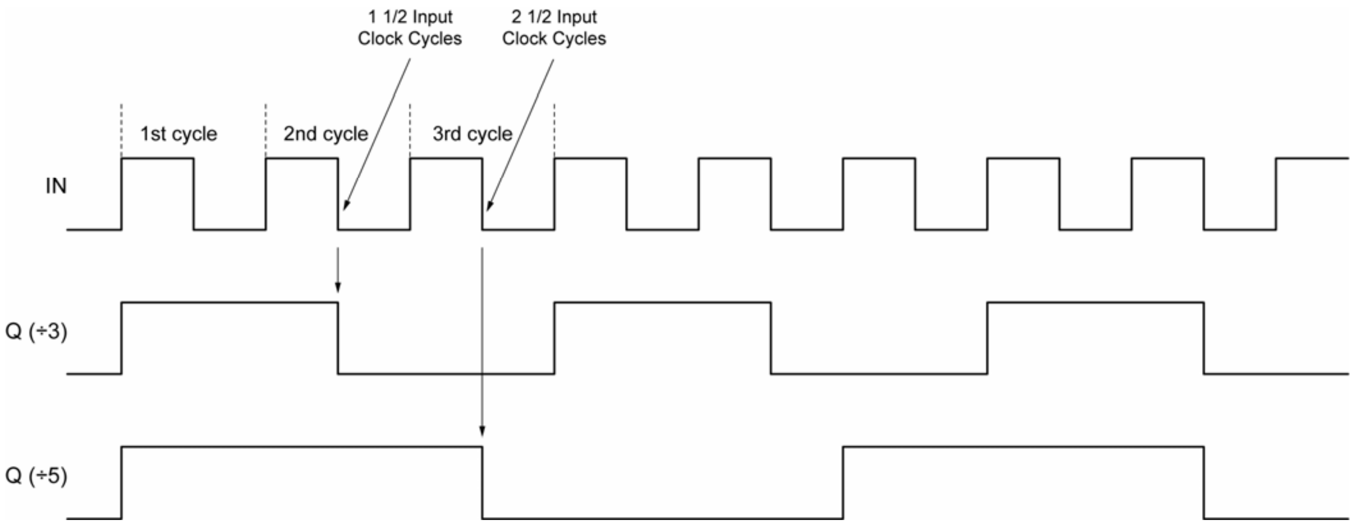

Figure 1d. Divider Operation Timing Diagram

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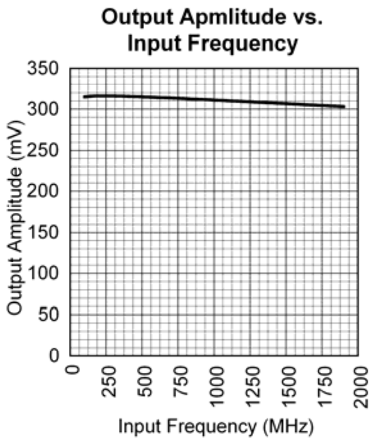
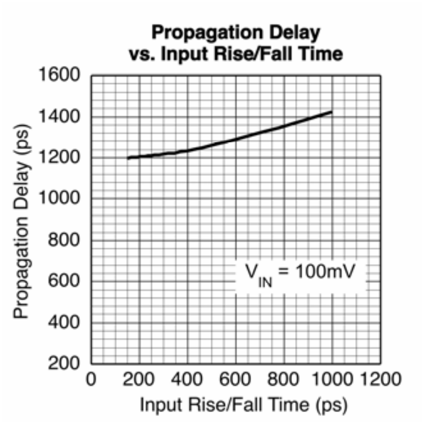
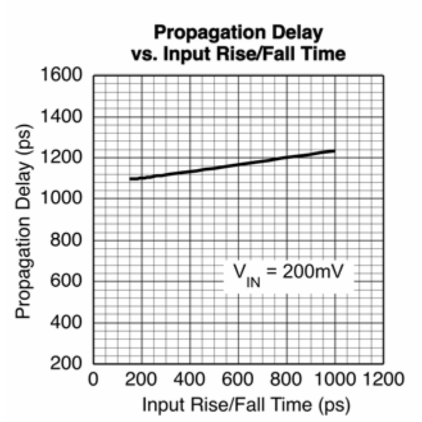
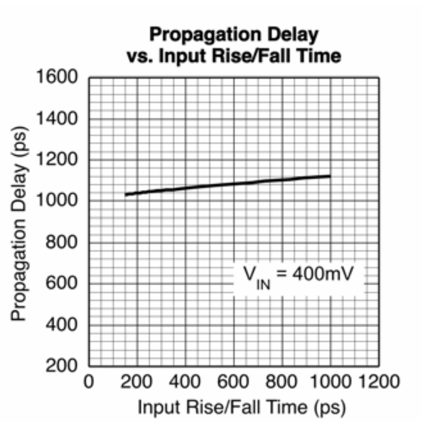
Typical Operating Characteristics

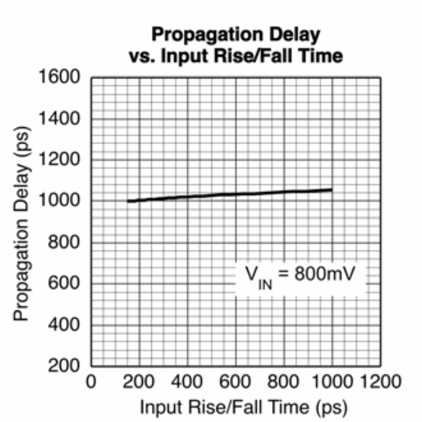
V_{CC} = 2.5V, GND = 0V, V_{IN} = 200mV, t_r / t_f ≤ 300ps, R_L = 100 across the outputs; T_A = 25°C, unless otherwise stated.











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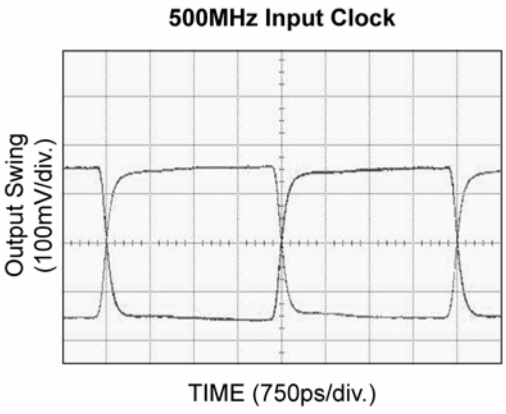
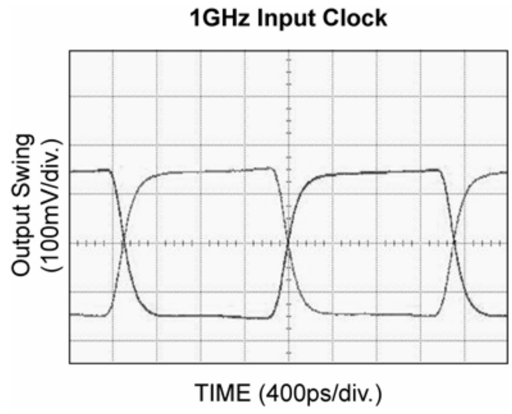
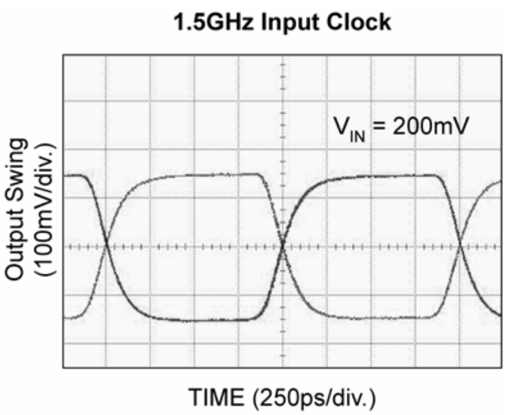
Functional Characteristics

V_{CC} =2.5V, GND = 0V, V_{IN} = 100mV, Q = Divide by 3, $t_r/t_f \leq$ 300ps, R_L = 100Ω across the outputs; T_A = 25°C, unless otherwise stated.







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Single-Ended and Differential Swings

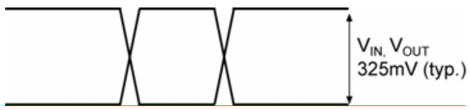

Figure 2a. Single-Ended Voltage Swing

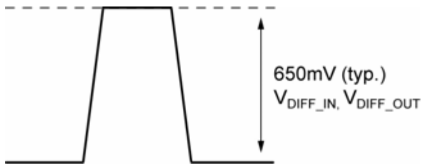

Figure 2b. Differential Voltage Swing

Input Stage

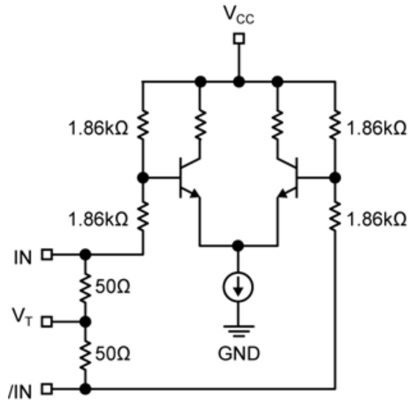

Figure 3. Simplified Differential Input Stage

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Input Interface Applications

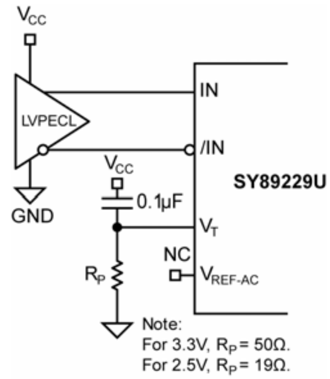


Figure 4a. LVPECL Interface (DC-Coupled)

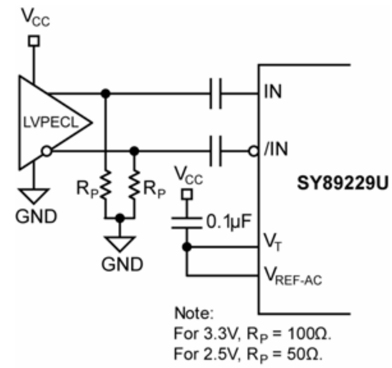
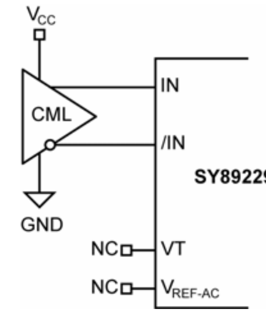


Figure 4b. LVPECL Interface (AC-Coupled)



Option: may connect V_T to V_{CC}

Figure 4c. CML Interface (DC-Coupled)

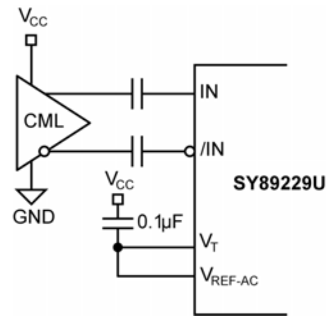


Figure 4d. CML Interface (AC-Coupled)

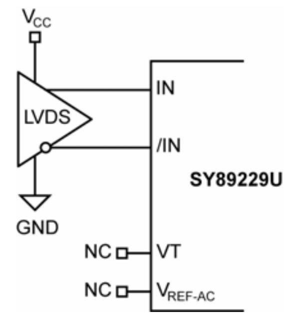


Figure 4e. LVDS Interface (DC-Coupled)

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LVDS Output Interface Applications

LVDS specifies a small swing of 325mV typical, on a nominal 1.2V common mode above ground. The common mode voltage has tight limits to permit large variations in the ground between and LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum, to keep EMI low.

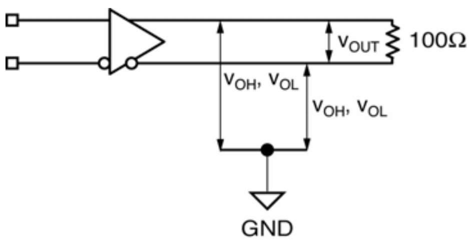


Figure 5a. LVDS Differential Measurement

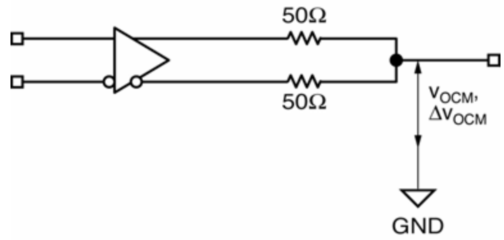
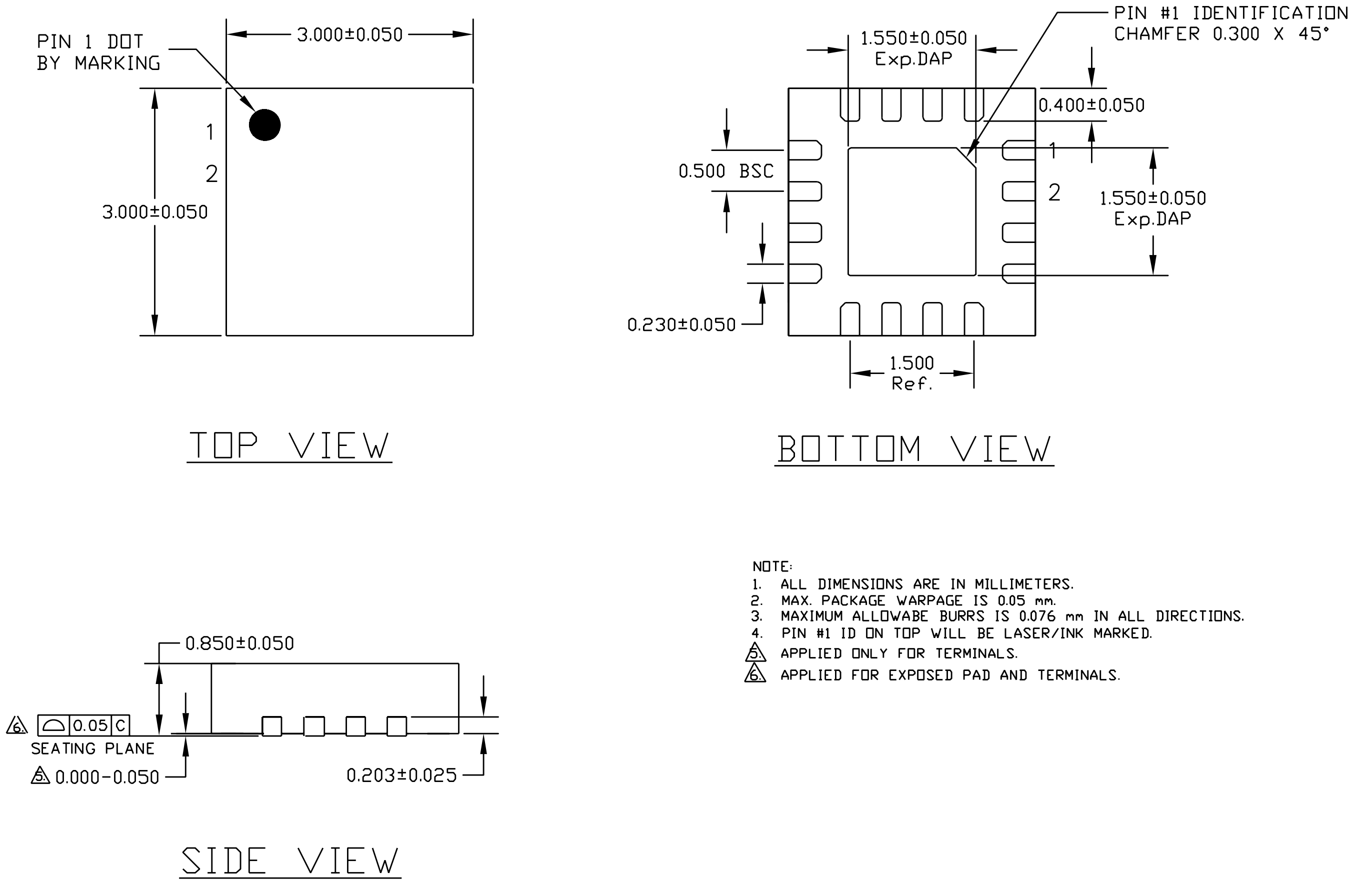


Figure 5b. LVDS Common Mode Measurement

Related Product and Support Documentation

Part Number	Function	Datasheet Link
SY89228U	1GHz Precision, LVPECL ÷3, ÷5 Clock Divider with Fail Safe Input and Internal Termination	http://www.micrel.com/_PDF/HBW/sy89228u.pdf
SY89230U	3.2GHz Precision, LVPECL ÷3, ÷5 Clock Divider	http://www.micrel.com/_PDF/HBW/sy89230u.pdf
SY89231U	3.2GHz Precision, LVDS ÷3, ÷5 Clock Divider	http://www.micrel.com/_PDF/HBW/sy89231u.pdf
	MLF® Application Note	www.amkor.com/products/notes_papers/MLFAppNote.pdf

Package Information



16-Pin MicroLeadFrame® (MLF-16)

Packages Notes:

1. Package meets Level 2 Moisture Sensitivity Classification.
2. All parts are dry-packed before shipment.
3. Exposed pad must be soldered to a ground for proper thermal management.

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