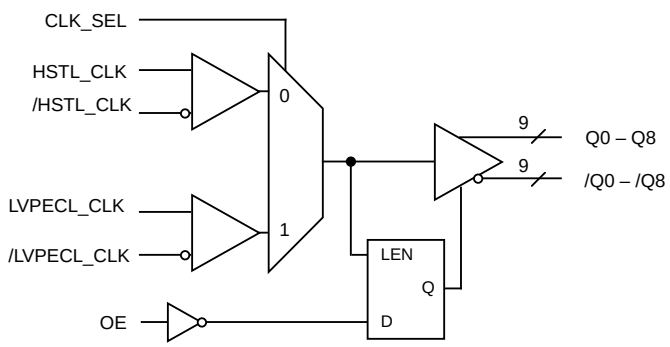
FEATURES

- 3.3V core supply, 1.8V output supply for reduced power
- LVPECL and HSTL inputs
- 9 differential HSTL (low-voltage swing) output pairs
- HSTL outputs drive 50Ω to ground with no offset voltage
- 500MHz maximum clock frequency
- Low part-to-part skew (200ps max.)
- Low pin-to-pin skew (50ps max.)
- Available in 32-pin TQFP package

Precision Edge®

LOGIC SYMBOL



DESCRIPTION

The SY89809L is a High-Performance Bus Clock Driver with 9 differential HSTL (High-Speed Transceiver Logic) output pairs. The part is designed for use in low-voltage (3.3V/1.8V) applications which require a large number of outputs to drive precisely aligned, ultralow skew signals to their destination. The input is multiplexed from either HSTL or LVPECL (Low-Voltage Positive-Emitter-Coupled Logic) by the CLK_SEL pin. The Output Enable (OE) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control.

The SY89809L features low pin-to-pin skew (50ps max.) and low part-to-part skew (200ps max.)—performance previously unachievable in a standard product having such a high number of outputs. The SY89809L is available in a single space saving package, enabling a lower overall cost solution.

APPLICATIONS

- High-performance PCs
- Workstations
- Parallel processor-based systems
- Other high-performance computing
- Communications

TRUTH TABLE

OE[1]	CLK_SEL	$Q_0 - Q_8$	$/Q_0 - /Q_8$
0	0	LOW	HIGH
0	1	LOW	HIGH
1	0	HSTL_CLK	/HSTL_CLK
1	1	LVPECL_CLK	/LVPECL_CLK

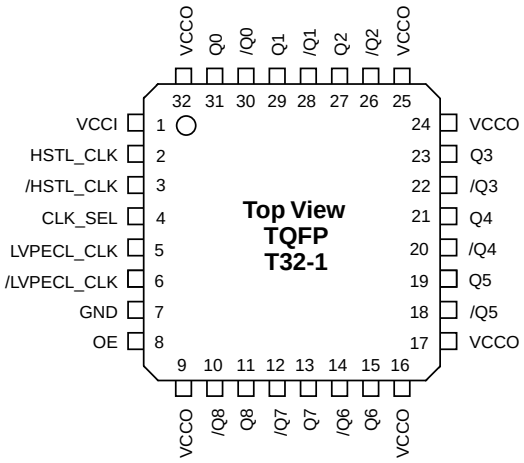
Note:

1. The OE (output enable) signal is synchronized with the low level of the HSTL_CLK and LVPECL_CLK signal.

SIGNAL GROUPS

Level	Direction	Signal
HSTL	Input	HSTL_CLK, /HSTL_CLK
HSTL	Output	$Q_0 - Q_8$, $/Q_0 - /Q_8$
LVPECL	Input	LVPECL_CLK, /LVPECL_CLK
LVCMOS/LVTTL	Input	CLK_SEL, OE

PACKAGE/ORDERING INFORMATION



32-Pin TQFP (T32-1)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89809LTC	T32-1	Industrial	SY89809LTC	Sn-Pb
SY89809LTCTR[2]	T32-1	Industrial	SY89809LTC	Sn-Pb
SY89809LTH[3]	T32-1	Industrial	SY89809LTH with Pb-Free bar line indicator	NiPdAu Pb-Free
SY89809LTHTR[2, 3]	T32-1	Industrial	SY89809LTH with Pb-Free bar line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Type	Pin Function
2, 3	HSTL_CLK, /HSTL_CLK	HSTL Input	Differential clock input selected by CLK_SEL. Can be left floating if not selected. Floating input, if selected produces an indeterminate output. HSTL input signal requires external termination 50Ω to GND.
5, 6	LVPECL_CLK, /LVPECL_CLK	LVPECL Input	Differential clock input selected by CLK_SEL. Can be left floating. Floating input, if selected produces a LOW at the output (internal 75Ω pull-downs). Requires external termination. 75kΩ pull-up.
4	CLK_SEL	LVTTL Input	Selects HSTL_CLK input when LOW and LVPECL_CLK output when HIGH. 11kΩ pull-up.
8	OE	LVTTL Input	Enable input synchronized internally to prevent glitching of the Q0-Q8 and /Q0-/Q8 outputs. Must be a minimum of three clock periods wide if synchronous with the CLK inputs and must meet the t_S and t_H requirements (refer to AC Electrical Characteristics). If asynchronous, must be a minimum of four clock periods wide. 11kΩ pull-up.
31, 29, 27, 23, 21, 19, 15, 13, 11	Q0–Q8	HSTL Output	Differential clock outputs from HSTL_CLK when CLK_SEL = LOW and LVPECL outputs when CLK_SEL = HIGH. HSTL outputs must be terminated with 50Ω to GND. Q0–Q8 outputs are static LOW when OE = LOW. Unused output pairs may be left floating.
30, 28, 26, 22, 20, 18, 14, 12, 10	/Q0–/Q8	HSTL Output	Differential clock outputs from HSTL_CLK when CLK_SEL = LOW and LVPECL outputs when CLK_SEL = HIGH. HSTL outputs must be terminated with 50Ω to GND. /Q0–/Q8 outputs are static HIGH when OE = LOW. Unused output pairs may be left floating.
1	VCCI	VCC Core Power	Core V_{CC} connected to 3.3V supply. Bypass with 0.1µF in parallel with 0.01µF low ESR capacitors as close to V_{CCI} pin as possible.
9, 16, 17, 24, 25, 32	VCCO	VCC Output Power	Output Buffer V_{CC} connected to 1.8V supply. Bypass with 0.1µF in parallel with 0.01µF low ESR capacitors as close to V_{CCO} pins as possible. All V_{CCO} pins should be connected together on the PCB.
7	GND	Ground	Ground.

Absolute Maximum Ratings[1]

Supply Voltage (V_{IN}) ..... –0.5V to V_{CCI}
V_{CC} Pin Potential to Ground Pin
(V_{CCI}, V_{CCO}) ..... –0.5V to +4.0V
DC Output Current, Output HIGH (I_{OUT}) ..... –50mA
Lead Temperature (soldering, 20 sec.) ..... 260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage
(V_{CCI}) ..... +3.15V to +3.45V
(V_{CCO}) ..... +1.6V to +2.0V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance
TQFP (θ_{JA})
–Still-Air ..... 50°C/W
–500lfpm ..... 42°C/W
TQFP (θ_{JC}) ..... 20°C/W

DC ELECTRICAL CHARACTERISTICS

Power Supply

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CCI}	V_{CC} Core	3.0	3.3	3.6	3.0	3.3	3.6	3.0	3.3	3.6	V
V_{CCO}	V_{CC} Output	1.6	1.8	2.0	1.6	1.8	2.0	1.6	1.8	2.0	V
I_{CCI}	I_{CC} Core	—	115	140	—	115	140	—	115	140	mA

HSTL

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage[3]	1.0	—	1.2	1.0	—	1.2	1.0	—	1.2	V
V_{OL}	Output LOW Voltage[3]	0.2	—	0.4	0.2	—	0.4	0.2	—	0.4	V
V_{IH}	Input HIGH Voltage	V_X +0.1	—	1.6	V_X +0.1	—	1.6	V_X +0.1	—	1.6	V
V_{IL}	Input LOW Voltage	–0.3	—	V_X –0.1	–0.3	—	V_X –0.1	–0.3	—	V_X –0.1	V
V_X	Input Crossover Voltage	0.68	—	0.9	0.68	—	0.9	0.68	—	0.9	V
I_{IH}	Input HIGH Current	+20	—	–350	+20	—	–350	+20	—	–350	µA
I_{IL}	Input LOW Current	—	—	–500	—	—	–500	—	—	–500	µA

Notes:

1. Permanent device damage may occur if “Absolute Maximum Ratings” are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Outputs loaded with 50Ω to ground.

DC ELECTRICAL CHARACTERISTICS (continued)

LVPECL

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	Input HIGH Voltage	V_{CCI} – 1.165	V_{CCI} – 0.880	V_{CCI} – 1.165	V_{CCI} – 0.880	V_{CCI} – 1.165	V_{CCI} – 0.880	V
V_{IL}	Input LOW Voltage	V_{CCI} – 1.810	V_{CCI} – 1.475	V_{CCI} – 1.810	V_{CCI} – 1.475	V_{CCI} – 1.810	V_{CCI} – 1.475	V
I_{IH}	Input HIGH Current	—	+150	—	+150	—	+150	µA
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	µA

LVCMOS/LVTTL

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IH}	Input HIGH Voltage	2.0	—	—	2.0	—	—	2.0	—	—	V
V_{IL}	Input LOW Voltage	—	—	0.8	—	—	0.8	—	—	0.8	V
I_{IH}	Input HIGH Current	+20	—	–250	+20	—	–250	+20	—	–250	µA
I_{IL}	Input LOW Current	—	—	–600	—	—	–600	—	—	–600	µA

AC ELECTRICAL CHARACTERISTICS[4]

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PHL} t_{PLH}	Propagation Delay[5]	—	1.0	—	—	1.0	—	—	1.0	—	ns
f_{MAX}	Maximum Operating Freq.[6]	500	—	—	500	—	—	500	—	—	MHz
t_{SKEW}	Within-Device Skew[7]	—	—	50	—	—	50	—	—	50	ps
t_{SKPP}	Part-to-Part Skew[8]	—	—	200	—	—	200	—	—	200	ps
V_{PP}	Minimum Input Swing[9] LVPECL_CLK	600	—	—	600	—	—	600	—	—	mV
V_{CMR}	Common Mode Range[10] LVPECL_CLK	–1.5	—	–0.4	–1.5	—	–0.4	–1.5	—	–0.4	V
t_S	OE Set-Up Time[11]	1.0	—	—	1.0	—	—	1.0	—	—	ns
t_H	OE Hold Time	0.5	—	—	0.5	—	—	0.5	—	—	ns
t_r t_f	Output Rise/Fall Time (20% – 80%)	300	—	650	300	—	650	300	—	650	ps

Notes:

4. Outputs loaded with 50Ω to ground. Airflow ≥ 300lfpm.
5. Differential propagation delay is defined as the delay from the crossing point of the differential input signals to the crossing point of the differential output signals.
6. Output swing greater than 450mV.
7. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device operating at the same voltage and temperature.
8. The part-to-part skew is defined as the absolute worst case difference between any two delay paths on any two devices operating at the same voltage and temperature.
9. The V_{PP}(min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay.
10. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The numbers in the table are referenced to V_{CCI}. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP}(min.). The lower end of the CMR range varies 1:1 with V_{CCI}. The V_{CMR}(min) will be fixed at 3.3V – |V_{CMR}(min)|.
11. OE set-up time is defined with respect to the rising edge of the clock. OE HIGH-to-LOW transition ensures outputs remain disabled during the next clock cycle. OE LOW-to-HIGH transition enables normal operation of the next input clock.

OUTPUT WAVEFORMS

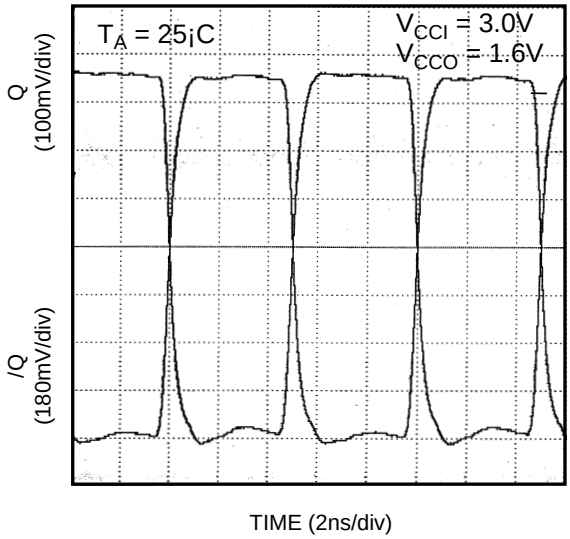


Figure 1. 100MHz Output Waveform

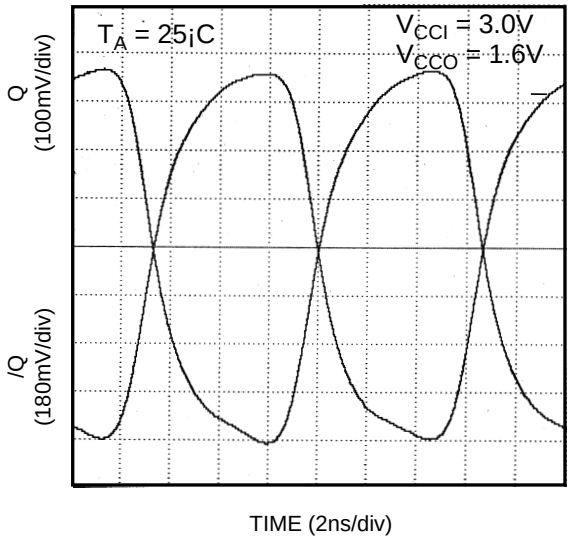
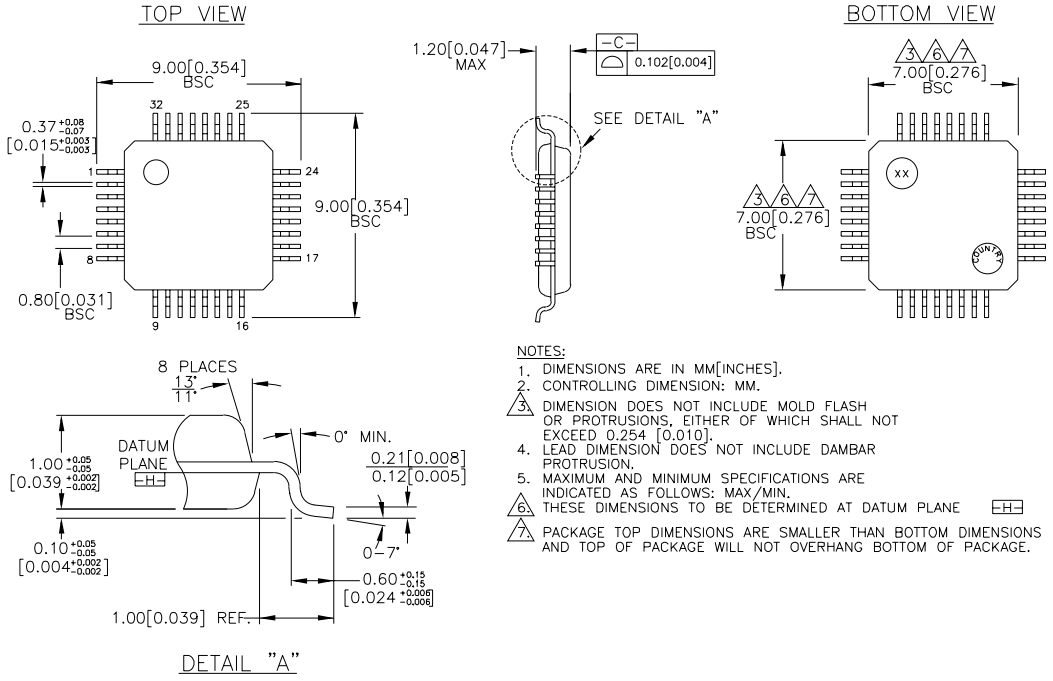


Figure 2. 300MHz Output Waveform

32 LEAD TQFP (T32-1)



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254 [0.010].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE −H−
7. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.

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