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**Precision LVPECL Runt Pulse Eliminator 2:1  
MUX with 1:2 Fanout and Internal Termination**

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## General Description

The SY89843U is a low jitter PECL, 2:1 differential input multiplexer (MUX) optimized for redundant source switchover applications. Unlike standard multiplexers, the SY89843U unique 2:1 Runt Pulse Eliminator (RPE) MUX prevents any short cycles or "runt" pulses during switchover. In addition, a unique Fail-Safe Input protection prevents metastable conditions when the selected input clock fails to a DC voltage (voltage between the pins of the differential input drops below 100mV).

The differential input includes Micrel's unique, 3-pin input termination architecture that allows customers to interface to any differential signal (AC- or DC-coupled) as small as 100mV (200mV<sub>PP</sub>) without any level shifting or termination resistor networks in the signal path. The output is 800mV, 100K compatible LVPECL with fast rise/fall times guaranteed to be less than 190ps.

The SY89843U operates from a 2.5V  $\pm 5\%$  or 3.3V  $\pm 10\%$  supply and is guaranteed over the full industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . The SY89843U is part of Micrel's high-speed, Precision Edge<sup>®</sup> product line. All support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).



Precision Edge<sup>®</sup>

## Features

- Selects between two sources, and provides a glitch-free, stable LVPECL output
- Guaranteed AC performance over temperature and supply voltage:
  - Wide operating frequency: 1kHz to  $>1.5\text{GHz}$
  - $< 880\text{ps}$  In-to-Out  $t_{pd}$
  - $< 190\text{ps}$   $t_r/t_f$
- Unique patent-pending input isolation design minimizes crosstalk
- Fail-Safe Input prevents oscillations
- Ultra-low jitter design:
  - $< 1\text{ps}_{\text{RMS}}$  random jitter
  - $< 1\text{ps}_{\text{RMS}}$  cycle-to-cycle jitter
  - $< 10\text{ps}_{\text{PP}}$  total jitter (clock)
  - $< 0.7\text{ps}_{\text{RMS}}$  MUX crosstalk induced jitter
- Unique patent-pending input termination and VT pin accepts DC- and AC-coupled inputs (CML, PECL, LVDS)
- 800mV LVPECL output swing
- 2.5V  $\pm 5\%$  or 3.3V  $\pm 10\%$  supply voltage
- $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  industrial temperature range
- Available in 24-pin (4mm x 4mm) MLF<sup>®</sup> package

## Applications

- Redundant clock switchover
- Failsafe clock protection

## Markets

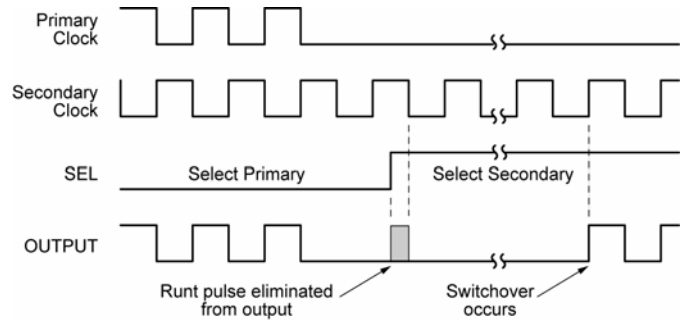
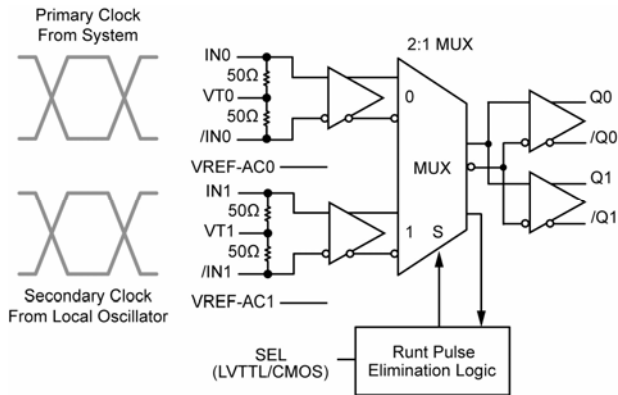
- LAN/WAN
- Enterprise servers
- ATE
- Test and measurement

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MLF and MicroLeadFrame are registered trademarks of Amkor Technology.

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# Typical Application



**Simplified Example Illustrating RPE (Runt Pulse Elimination) Circuit when Primary Clock Fails**

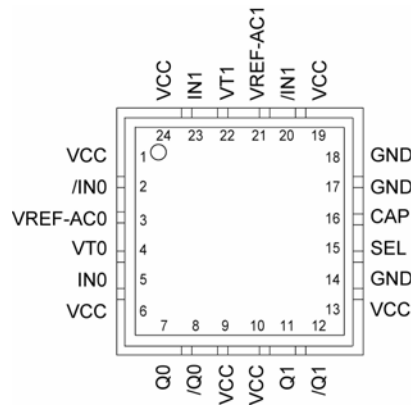
## Ordering Information<sup>(1)</sup>

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89843UMG	MLF-24	Industrial	843U with bar-line Pb-Free indicator	NiPdAu Pb-Free
SY89843UMGTR <sup>(2)</sup>	MLF-24	Industrial	843U with bar-line Pb-Free indicator	NiPdAu Pb-Free

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC Electricals Only.
2. Tape and Reel.

## Pin Configuration



**24-Pin MLF<sup>®</sup> (MLF-24)**

## Pin Description

Pin Number	Pin Name	Pin Function
5, 2 23, 20	IN0, /IN0, IN1, /IN1	Differential Inputs: These input pairs are the differential signal inputs to the device. These inputs accept AC- or DC-coupled signals as small as 100mV (200mV <sub>PP</sub> ). Each pin of a pair internally terminates to a VT pin through 50Ω. Please refer to the "Input Interface Applications" section for more details.
4, 22	VT0, VT1	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT0 and VT1 pins provide a center-tap to a termination network for maximum interface flexibility. Please refer to the "Input Interface Applications" section for more details.
3, 21	VREF-AC0 VREF-AC1	Reference Voltage: These outputs bias to V <sub>CC</sub> -1.2V. They are used for AC-coupling inputs IN and /IN. Connect VREF-AC directly to the corresponding VT pin. Bypass with 0.01μF low ESR capacitor to VCC. Maximum sink/source current is ±1.5mA. Please refer to the "Input Interface Applications" section for more details.
15	SEL	This single-ended TTL/CMOS-compatible input selects the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open.
1, 6, 9, 10, 13, 19, 24	VCC	Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors as close to VCC pins as possible.
7, 8 11, 12	Q0, /Q0 Q1, /Q1	Differential Outputs: These differential LVPECL outputs are a logic function of the IN0, IN1, and SEL inputs. Please refer to the truth table below for details.
14, 17, 18	GND Exposed Pad	Ground: Ground pin and exposed pad must be connected to the same ground plane.
16	CAP	Power-On Reset (POR) Initialization capacitor. When using the multiplexer with RPE capability, the pin is tied to a capacitor to VCC. The purpose is to ensure the internal RPE logic starts up in a known state. See "Power-On Reset (POR) Description" section for more details regarding capacitor selection. If this pin is tied directly to VCC, the RPE function will be disabled and the multiplexer will function as a normal multiplexer. The CAP pin should never be left open.

## Truth Table

INPUTS					OUTPUTS	
IN0	/IN0	IN1	/IN1	SEL	Q	/Q
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

### Absolute Maximum Ratings<sup>(1)</sup>

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.0V
Input Voltage ( $V_{IN}$ )	-0.5V to $V_{CC}$
LVPECL Output Current ( $I_{OUT}$ )	
Continuous	±50mA
Surge	±100mA
Termination Current	
Source/Sink Current on $V_T$	±100mA
Input Current	
Source/sink current on IN, /IN	±50mA
$V_{REF-AC}$ Current	
Source/sink current on $V_{REF-AC}$	±2mA
Lead Temperature (soldering, 20 sec.)	+260°C
Storage Temperature ( $T_s$ )	-65°C to 150°C

### Operating Ratings<sup>(2)</sup>

Supply Voltage ( $V_{CC}$ )	+2.375V to +2.625V
	+3.0V to +3.6V
Ambient Temperature ( $T_A$ )	-40°C to +85°C
Package Thermal Resistance <sup>(3)</sup>	
MLF <sup>®</sup> ( $\theta_{JA}$ )	
Still-Air	50°C/W
MLF <sup>®</sup> ( $\Psi_{JB}$ )	
Junction-to-Board	30°C/W

### DC Electrical Characteristics<sup>(4)</sup>

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ; unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{CC}$	Power Supply		2.375	2.5	2.625	V
			3.0	3.3	3.6	V
$I_{CC}$	Power Supply Current	No load, max $V_{CC}$ .		70	100	mA
$R_{IN}$	Input Resistance (IN-to- $V_T$ )		45	50	55	$\square$
$R_{DIFF\_IN}$	Differential Input Resistance (IN-to-/IN)		90	100	110	$\square$
$V_{IH}$	Input High Voltage (IN, /IN)		1.2		$V_{CC}$	V
$V_{IL}$	Input Low Voltage (IN, /IN)		0		$V_{IH}-0.1$	V
$V_{IN}$	Input Voltage Swing (IN, /IN)	See Figure 1a. Note 5	0.1		$V_{CC}$	V
$V_{DIFF\_IN}$	Differential Input Voltage Swing $ I_{IN}-/I_{IN} $	See Figure 1b.	0.2			V
$V_{IN\_FSI}$	Input Voltage Threshold that triggers FSI			30	100	mV
$V_{T\_IN}$	IN-to- $V_T$ (IN, /IN)				1.28	V
$V_{REF-AC}$	Output Reference Voltage		$V_{CC}-1.3$	$V_{CC}-1.2$	$V_{CC}-1.1$	V

**Notes:**

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.  $\theta_{JA}$  and  $\Psi_{JB}$  values are determined for a 4-layer board in still air unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5.  $V_{IN}$  (max) is specified when  $V_T$  is floating.

## LVPECL Outputs DC Electrical Characteristics<sup>(6)</sup>

$V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ,  $R_L = 50\Omega$  to  $V_{CC}-2V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output HIGH Voltage Q, /Q		$V_{CC}-1.145$		$V_{CC}-0.895$	V
$V_{OL}$	Output Low Voltage Q, /Q		$V_{CC}-1.945$		$V_{CC}-1.695$	V
$V_{OUT}$	Output Voltage Swing Q, /Q	See Figure 1a.	550	800		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing Q, /Q	See Figure 1b.	1100	1600		mV

## LVTTL/CMOS DC Electrical Characteristics<sup>(6)</sup>

$V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{IH}$	Input HIGH Voltage		2.0			V
$V_{IL}$	Input LOW Voltage				0.8	V
$I_{IH}$	Input HIGH Current		-125		30	$\mu A$
$I_{IL}$	Input LOW Current		-300			$\mu A$

**Note:**

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## AC Electrical Characteristics<sup>(7)</sup>

$V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ,  $R_L = 50\Omega$  to  $V_{CC} - 2V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$f_{MAX}$	Maximum Operating Frequency	$V_{OUT} \leq 400mV$	1.5	2.0		GHz
$t_{pd}$	Differential Propagation Delay	In-to-Q $100mV < V_{IN} \leq 200mV^{(8, 9)}$	480	600	880	ps
		In-to-Q $200mV < V_{IN} \leq 800mV^{(8, 9)}$	430	575	780	ps
		SEL-to-Q RPE enabled, see Timing Diagram			17	cycles
		SEL-to-Q RPE disabled ( $V_{SEL} = V_{CC}/2$ )	550		900	ps
$t_{pd}$ Tempco	Differential Propagation Delay Temperature Coefficient			410		fs/ $^\circ C$
$t_{SKEW}$	Output-to-Output Skew	Within device <sup>(10)</sup>			20	ps
	Part-to-Part Skew	Note 11			200	ps
$t_{JITTER}$	Clock					
	Random Jitter	Note 12			1	ps <sub>RMS</sub>
	Cycle-to-Cycle Jitter	Note 13			1	ps <sub>RMS</sub>
	Total Jitter	Note 14			10	ps <sub>PP</sub>
	Crosstalk-induced Jitter	Note 15			0.7	ps <sub>RMS</sub>
$t_r, t_f$	Output Rise/Fall Time (20% to 80%)	At full output swing.	70		190	ps

### Notes:

- High-frequency AC-parameters are guaranteed by design and characterization.
- Propagation delay is measured with input  $t_r, t_f \leq 300ps$  (20% to 80%) and  $V_{IL} \leq 800mV$ .
- Propagation delay is a function of the rise and fall times at IN. See "Typical Operating Characteristics" for details.
- Output-to-output skew is measured between two different outputs under identical conditions.
- Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
- Random jitter is measured with a K28.7 character pattern, measured at  $<f_{MAX}$ .
- Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles,  $T_n - T_{n-1}$  where T is the time between rising edges of the output signal.
- Total jitter definition: with an ideal clock input of frequency  $<f_{MAX}$ , no more than one output edge in  $10^{12}$  output edges will deviate by more than the specified peak-to-peak jitter value.
- Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.

## Functional Description

### RPE MUX and Fail-Safe Input

The SY89843U is optimized for clock switchover applications where switching from one clock to another clock without runt pulses (short cycles) is required. It features two unique circuits:

#### *Runt-Pulse Eliminator (RPE) Circuit:*

The RPE MUX provides a “glitchless” switchover between two clocks and prevents any runt pulses from occurring during the switchover transition. The design of both clock inputs is identical (i.e., the switchover sequence and protection is symmetrical for both input pair, IN0 or IN1. Thus, either input pair may be defined as the primary input). If not required, the RPE function can be permanently disabled to allow the switchover between inputs to occur immediately. If the CAP pin is tied directly to V<sub>CC</sub>, then the RPE function will be disabled and the multiplexer will function as a normal multiplexer.

#### *Fail-Safe Input (FSI) Circuit:*

The FSI function provides protection against a selected input pair that drops below the minimum amplitude requirement. If the selected input pair drops sufficiently below the 100mV minimum single-ended input amplitude limit (V<sub>IN</sub>), or 200mV differentially (V<sub>DIFF\_IN</sub>), then the output will latch to the last valid clock state.

### RPE and FSI Functionality

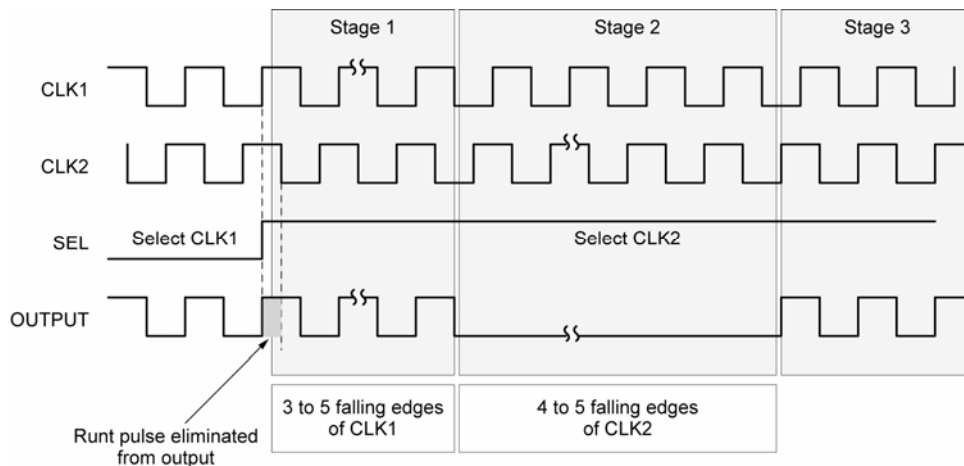
The basic operation of the RPE MUX and FSI functionality is described with the following four case descriptions. All descriptions are related to the true inputs and outputs. The primary (or selected) clock is called CLK1; the secondary (or alternate) clock is called CLK2. Due to the totally asynchronous relation of the IN and SEL signals and an additional internal protection against metastability, the number of pulses required for the operations described in cases 1-4 can vary within certain limits. Refer to “Timing Diagrams” for more detailed information.

#### *Case #1 Two Normal Clocks and RPE Enabled*

In this case, the frequency difference between the two running clocks IN0 and IN1 must not be greater than 1.5:1. For example, if the IN0 clock is 500MHz, the IN1 clock must be within the range of 334MHz to 750MHz.

If the SEL input changes state to select the alternate clock, then the switchover from CLK1 to CLK2 will occur in three stages.

- Stage 1: The output will continue to follow CLK1 for a limited number of pulses.
- Stage 2: The output will remain LOW for a limited number of pulses of CLK2.
- Stage 3: The output follows CLK2.



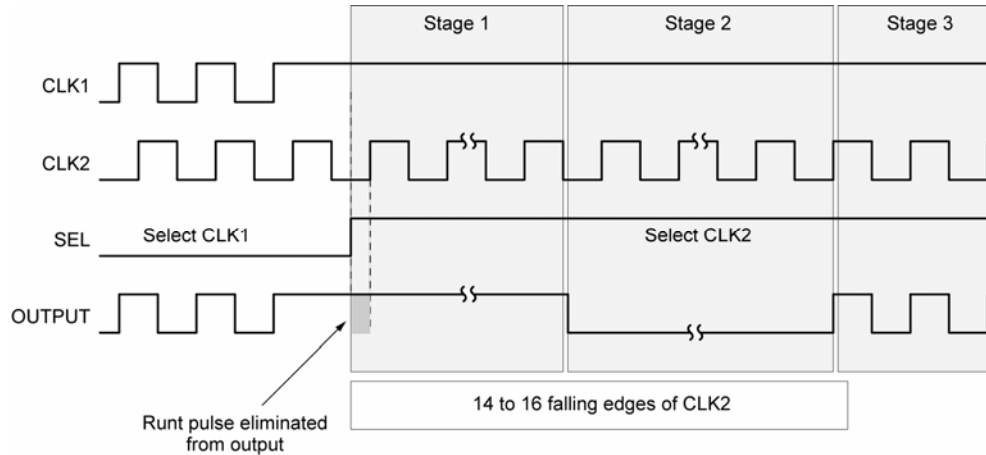
Timing Diagram 1



*Case #2 Input Clock Failure: Switching from a selected clock stuck HIGH to a valid clock (RPE enabled).*

If CLK1 fails HIGH before the RPE MUX selects CLK2 (using the SEL pin), then the switchover will occur in three stages.

- Stage 1: The output will remain HIGH for a limited number of pulses of CLK2.
- Stage 2: The output will switch to LOW and then remain LOW for a limited number of falling edges of CLK2.
- Stage 3: The output will follow CLK2



**Timing Diagram 2**

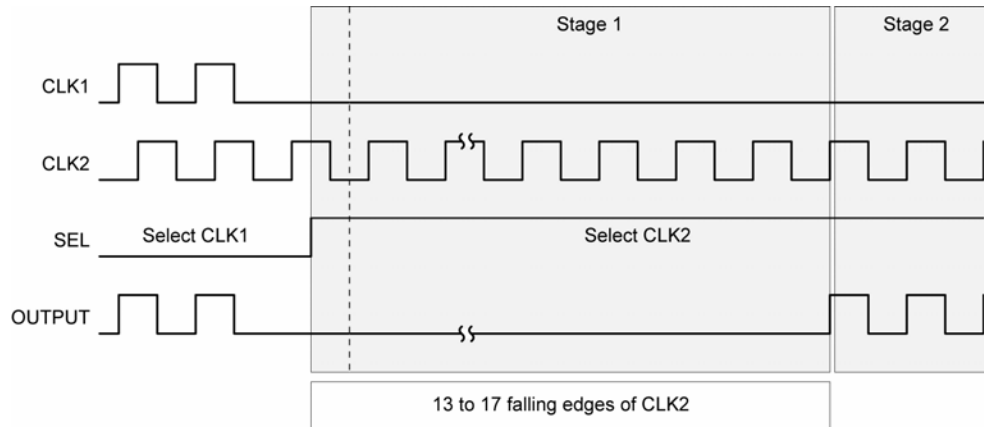
Note:

Output shows extended clock cycle during switchover. Pulse width for both high and low of this cycle will always be greater than 50% of the CLK2 period.

*Case #3 Input Clock Failure: Switching from a selected clock stuck Low to a valid clock (RPE enabled).*

If CLK1 fails LOW before the RPE MUX selects CLK2 (using the SEL pin), the switchover will occur in two stages.

- Stage 1: The output will remain LOW for a limited number of falling edges of CLK2.
- Stage 2: The output will follow CLK2.



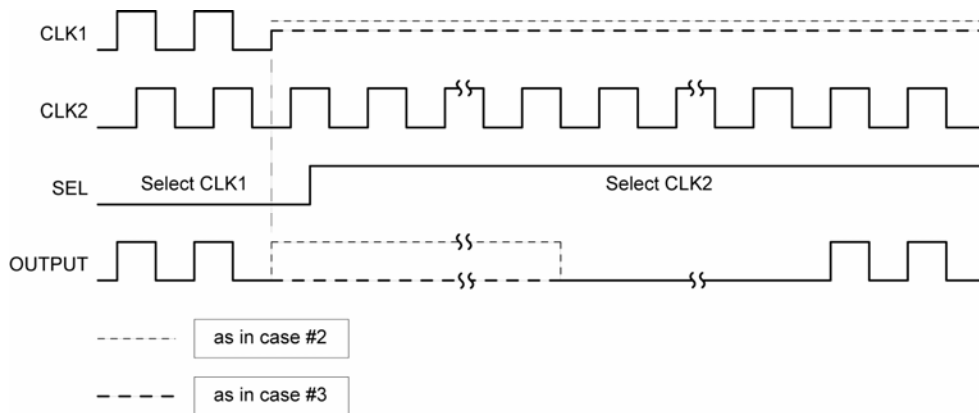
**Timing Diagram 3**

*Case #4 Input Clock Failure: Switching from the selected clock input stuck in an undetermined state to a valid clock input (RPE enabled).*

If CLK1 fails to an undetermined state (e.g., amplitude falls below the 100mV (V<sub>IN</sub>) minimum single-ended input limit, or 200mV differentially) before the RPE MUX selects CLK2 (using the SEL pin), the switchover to the valid clock CLK2 will occur either following Case #2 or Case #3, depending upon the last valid state at the CLK1. If the selected input clock fails to a floating, static, or extremely low signal swing, including 0mV, the FSI

function will eliminate any metastable condition and guarantee a stable output signal. No ringing and no undetermined state will occur at the output under these conditions.

Please note that the FSI function will not prevent duty cycle distortions or runt pulses in case of a slowly deteriorating (but still toggling) input signal. Due to the FSI function, the propagation delay will depend on rise and fall time of the input signal and on its amplitude. Refer to “Typical Operating Characteristics” for more detailed information.



Timing Diagram 4

### Power-On Reset (POR) Description

The SY89843U includes an internal power-on reset (POR) function to ensure the RPE logic starts-up in a known logic state once the power-supply voltage is stable. An external capacitor connected between V<sub>CC</sub> and the CAP pin (pin 16) controls the delay for the power-on reset function.

Calculating the required capacitor value is based on the time the system power supply needs to power up to a minimum of 2.3V. The time constant for the internal power-on-reset must be greater than the time required for the power supply to ramp up to a minimum of 2.3V.

The following equation describes this relationship:

$$C(\mu F) \geq \frac{t_{dPS}(ms)}{12(ms / \mu F)}$$

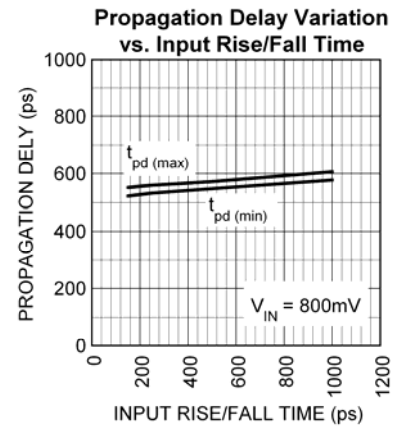
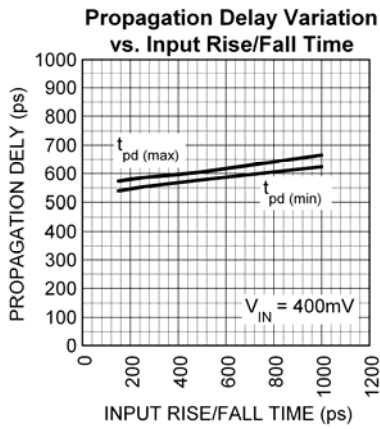
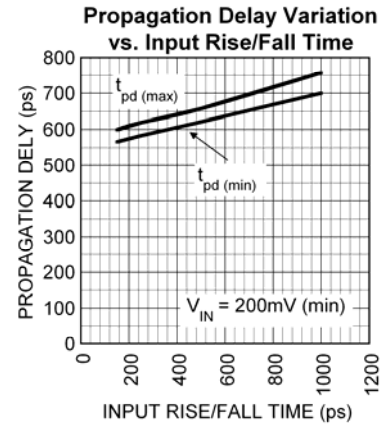
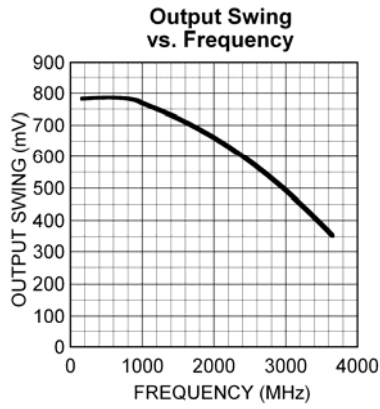
As an example, if the time required for the system power supply to power up past 2.3V is 12ms, the required capacitor value on pin 16 would be:

$$C(\mu F) \square \frac{12ms}{12(ms / \mu F)}$$

$$C(\mu F) \square 1\mu F$$

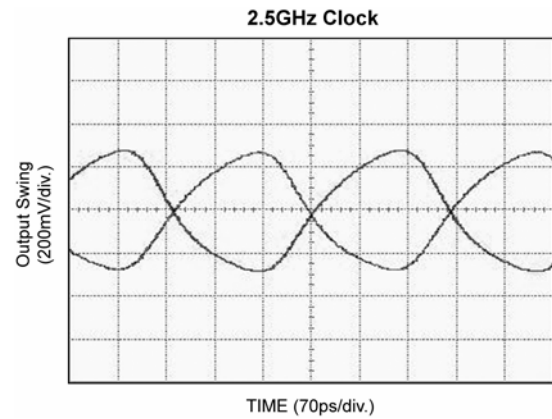
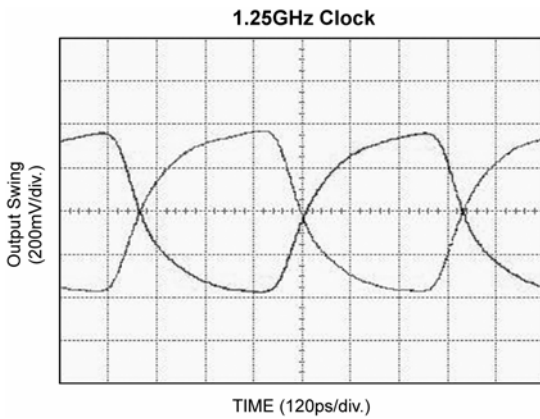
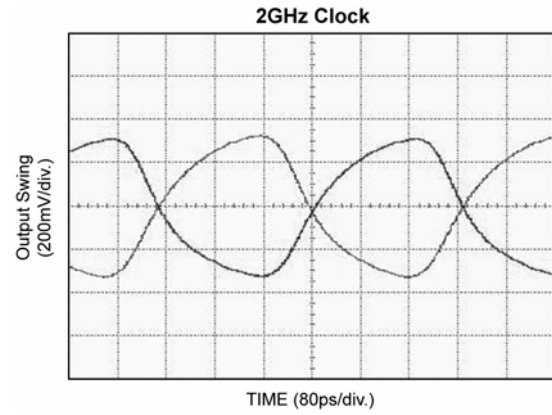
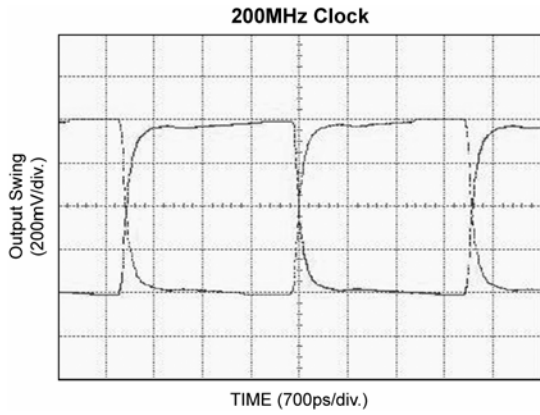
### Typical Operating Characteristics

$V_{CC} = 3.3V$ ,  $GND = 0V$ ,  $V_{IN} = 400mV_{pk}$ ,  $t_r/t_f = 300ps$ ,  $R_L = 50\Omega$  to  $V_{CC}-2V$ ,  $T_A = 25^\circ C$ , unless otherwise stated.



### Functional Characteristics

$V_{CC} = 3.3V$ ,  $GND = 0V$ ,  $V_{IN} \approx 400mV_{pk}$ ,  $t_r/t_f \approx 300ps$ ,  $R_L = 50\Omega$  to  $V_{CC}-2V$ ,  $T_A = 25^\circ C$ , unless otherwise stated.



## Singled-Ended and Differential Swings

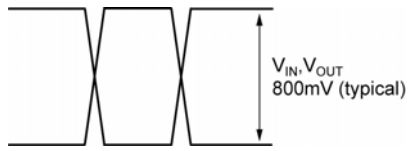


Figure 1a. Single-Ended Voltage Swing

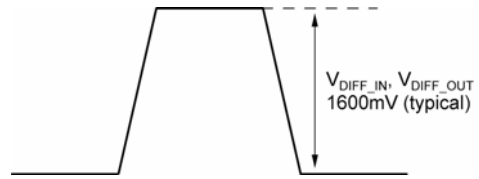


Figure 1b. Differential Voltage Swing

## Input and Output Stages

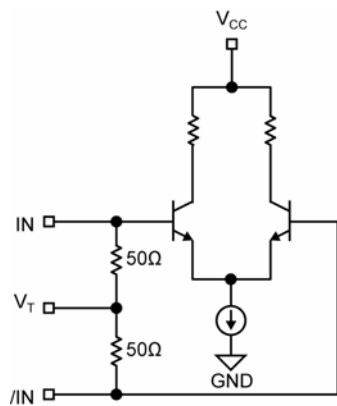


Figure 2a. Simplified Differential Input Stage

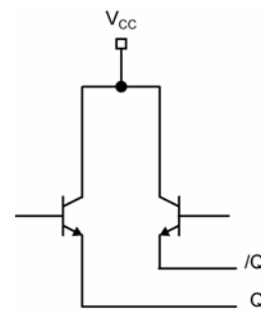
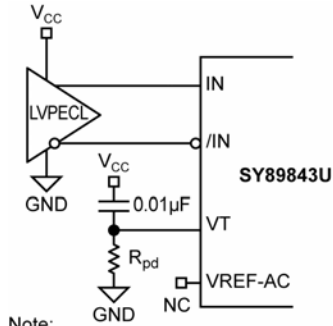


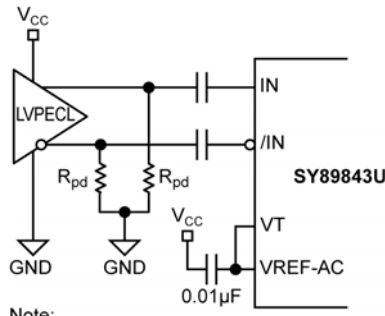
Figure 2b. Simplified LVPECL Output Stage

## Input Interface Applications



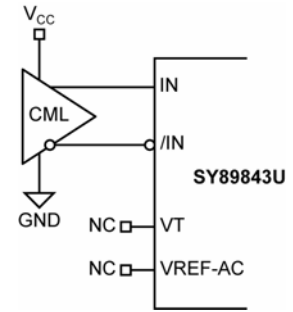
Note:  
 For 3.3V,  $R_{pd} = 50\Omega$ .  
 For 2.5V,  $R_{pd} = 19\Omega$ .

**Figure 3a. LVPECL Interface (DC-Coupled)**



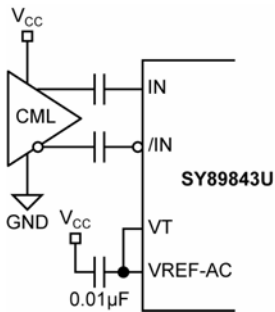
Note:  
 For 3.3V,  $R_{pd} = 100\Omega$ .  
 For 2.5V,  $R_{pd} = 50\Omega$ .

**Figure 3b. LVPECL Interface (AC-Coupled)**

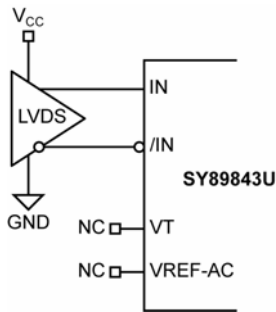


*Option: may connect  $V_T$  to  $V_{CC}$*

**Figure 3c. CML Interface (DC-Coupled)**



**Figure 3d. CML Interface (AC-Coupled)**



**Figure 3e. LVDS Interface**

### LVPECL Output Interface Applications

LVPECL has a high input impedance, a very low output impedance (open emitter), and a small signal swing which results in low EMI. LVPECL is ideal for driving 50Ω and 100Ω controlled impedance transmission lines. There are several techniques for terminating the

LVPECL output: parallel termination-thevenin equivalent, parallel termination (3-resistor), and AC-coupled termination. Unused output pairs may be left floating. However, single-ended outputs must be terminated, or balanced.

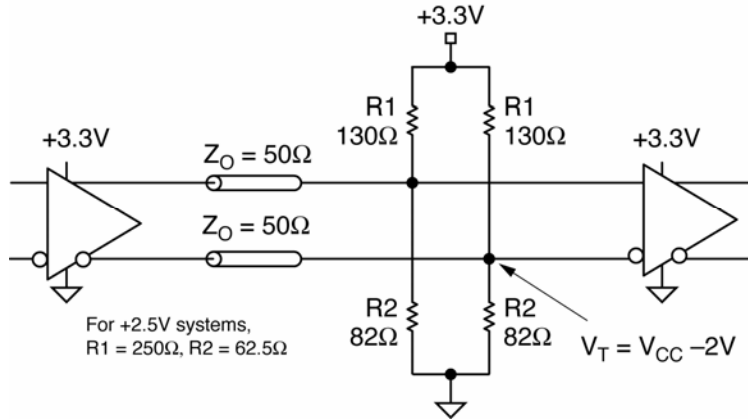
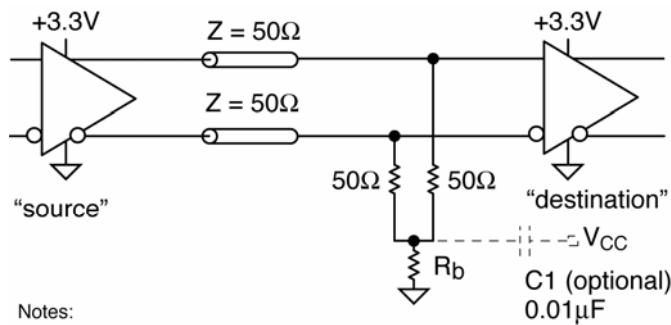


Figure 4a. Parallel Termination-Thevenin Equivalent



Notes:

1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. R<sub>b</sub> resistor sets the DC bias voltage, equal to V<sub>T</sub>.
4. For 2.5V systems, R<sub>b</sub> = 19Ω, For 3.3V systems, R<sub>b</sub> = 50Ω

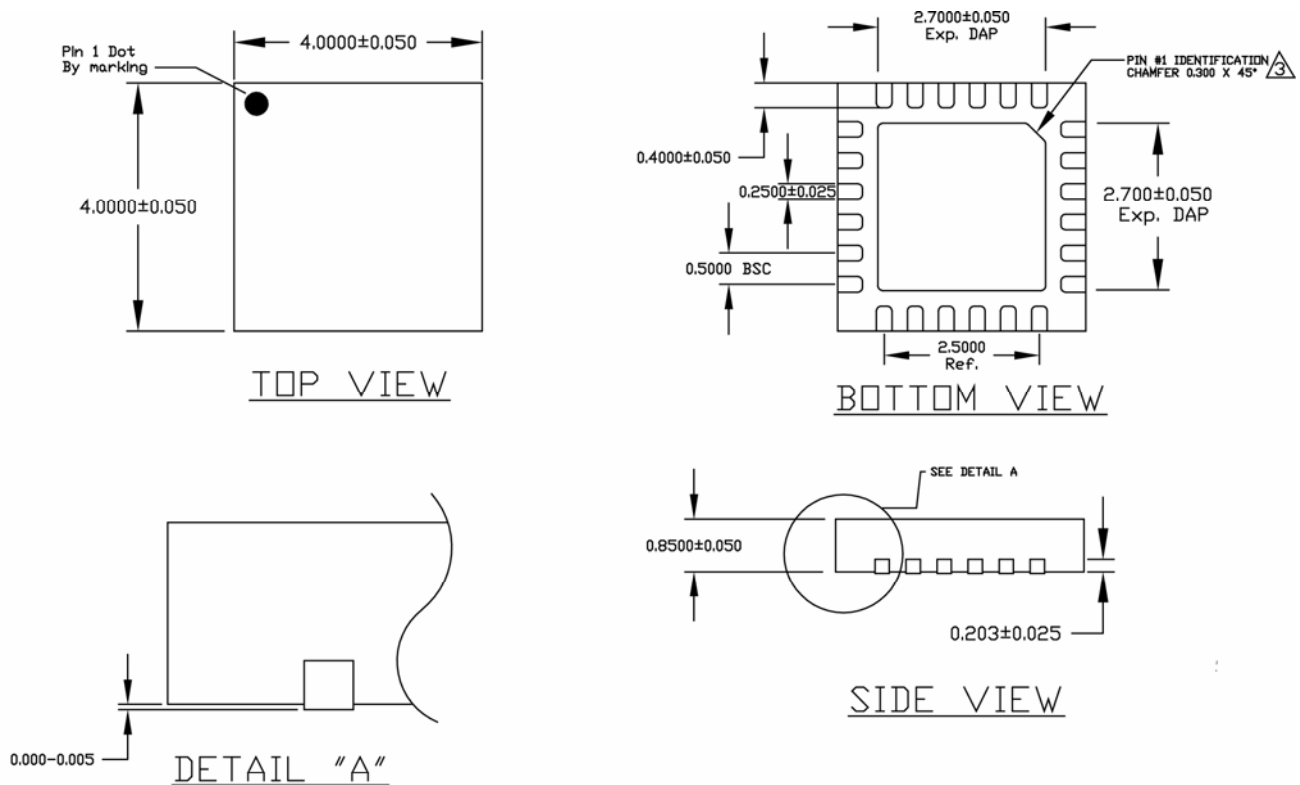
Figure 4b. Parallel Termination (3-Resistor)

### Related Product and Support Documentation

Part Number	Function	Data Sheet Link
SY89844U	Precision LVDS Runt Pulse Eliminator 2:1 MUX with 1:2 Fanout and Internal Termination	<a href="http://www.micrel.com/product-info/products/sy89844u.shtml">www.micrel.com/product-info/products/sy89844u.shtml</a>
SY89845U	Precision CML Runt Pulse Eliminator 2:1 MUX with 2:1 Fanout and Internal Termination	<a href="http://www.micrel.com/product-info/products/sy89845u.shtml">www.micrel.com/product-info/products/sy89845u.shtml</a>
	MLF® Application Note	<a href="http://www.amkor.com/products/notes_papers/MLFAppNote.pdf">www.amkor.com/products/notes_papers/MLFAppNote.pdf</a>
HBW Solutions	New Products and Applications	<a href="http://www.micrel.com/product-info/products/solutions.shtml">www.micrel.com/product-info/products/solutions.shtml</a>



**Product Information**



**NOTE:**

1. ALL DIMENSIONS ARE IN MILLIMETERS (mm).
2. THE PIN#1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.
3. CHAMFER STYLE PIN 1 IDENTIFIER ON BOTTOM SIDE

**24-Pin MLF<sup>®</sup> (MLF-24)**

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