400 MHz Low Voltage PECL Clock Synthesizer w/Spread Spectrum

MPC92469

The MPC92469 is a 3.3 V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking and computing applications. With output frequencies from 25 MHz to 400 MHz and the support of differential PECL output signals the device meets the needs of the most demanding clock applications.

400 MHz LOW VOLTAGE CLOCK SYNTHESIZER w/SPREAD SPECTRUM

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-03

Features

- 25 MHz to 400 MHz synthesized clock output signal
- Differential PECL output
- LVCMOS compatible control inputs
- On-chip crystal oscillator for reference frequency generation
- Spread Spectrum output for EMI reduction
- 3.3 V power supply
- Fully integrated PLL
- Minimal frequency overshoot
- Serial 3-wire programming interface
- Parallel programming interface for power-up
- 32-lead LQFP packaging
- 32-lead Pb-free package available
- SiGe Technology
- Ambient temperature range 0°C to +70°C
- Pin compatible to the MC12429, MPC9229, MPC92429, and ICS84329

Functional Description

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. The frequency of the internal crystal oscillator is divided by 16 and then multiplied by the PLL. The VCO within the PLL operates over a range of 400 to 800 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The crystal oscillator frequency f_{XTAL}, the PLL feedback-divider M and the PLL post-divider N determine the output frequency.

The feedback path of the PLL is internal. The PLL adjusts the VCO output frequency to be 2·M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve phase lock. The PLL will be stable if the VCO frequency is within the specified VCO frequency range (400 to 800 MHz). The M-value must be programmed by the serial or parallel interface.

The PLL post-divider N is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle. The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated 50 Ω to V_{CC} – 2.0 V. The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. It is recommended on system reset to hold the P_LOAD input LOW until power becomes valid. On the LOW-to-HIGH transition of P_LOAD, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs prevent the LVCMOS compatible control inputs from floating.

The serial interface centers on a eighteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See PROGRAMMING INTERFACE for more information. The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. In order to minimize the PLL jitter, it is recommended to avoid active signal on the TEST output.

PACKAGE DIMENSIONS

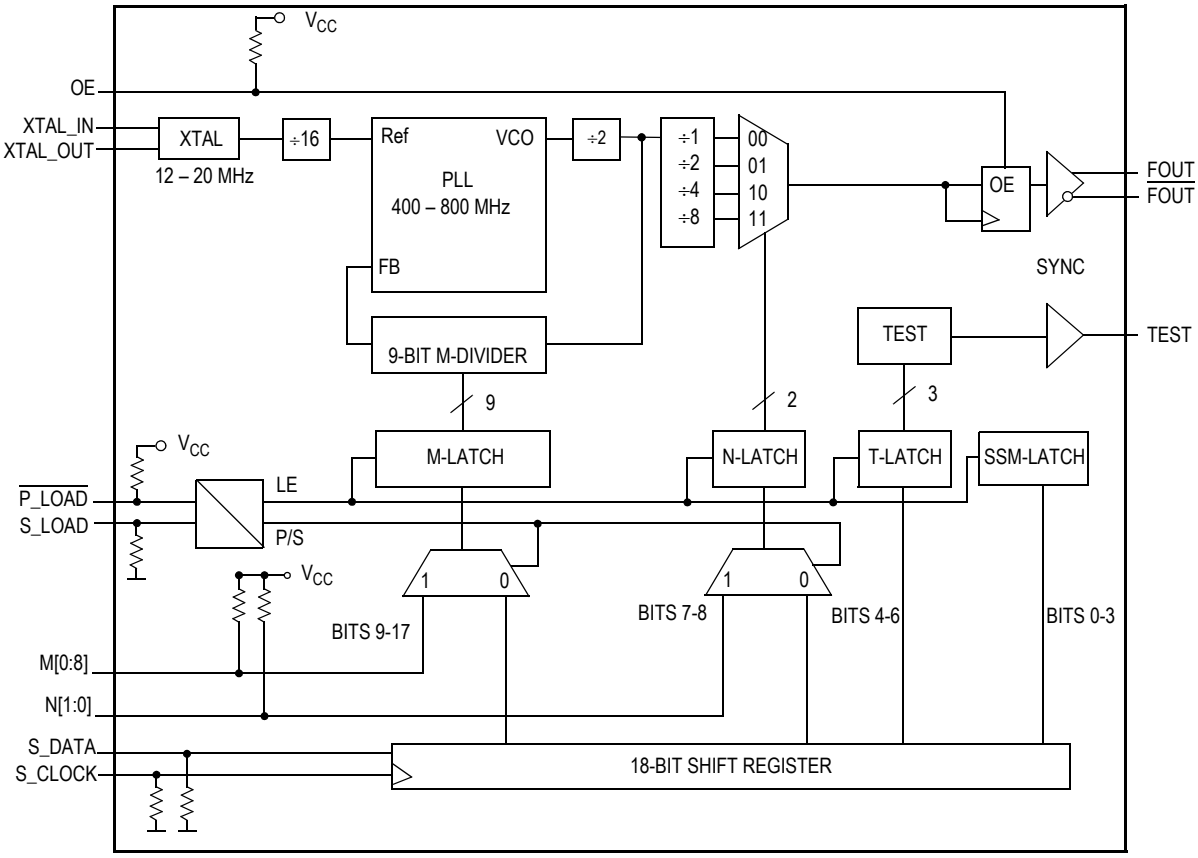

Figure 1. MPC92469 Logic Diagram

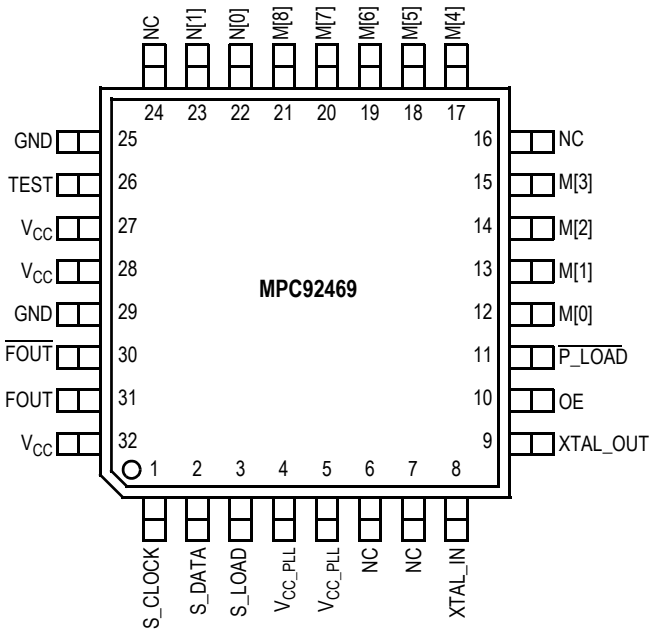

Figure 2. MPC92469 32-Lead Package Pinout
(Top View)

Table 1. Pin Configurations

Pin	I/O	Default	Type	Function
XTAL_IN, XTAL_OUT			Analog	Crystal oscillator interface.
FOUT, $\overline{\text{FOUT}}$	Output		LVPECL	Differential clock output.
TEST	Output		LVCMOS	Test and device diagnosis output.
S_LOAD	Input	0	LVCMOS	Serial configuration control input. This inputs controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition.
$\overline{\text{P\_LOAD}}$	Input	1	LVCMOS	Parallel configuration control input. This input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of $\overline{\text{P\_LOAD}}$. $\overline{\text{P\_LOAD}}$ is state sensitive.
S_DATA	Input	0	LVCMOS	Serial configuration data input.
S_CLOCK	Input	0	LVCMOS	Serial configuration clock input.
M[8:0]	Input	1	LVCMOS	Parallel configuration for PLL feedback divider (M). M is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$.
N[1:0]	Input	1	LVCMOS	Parallel configuration for Post-PLL divider (N). N is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$.
OE	Input	1	LVCMOS	Output enable (active high). The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the F_{OUT} output. OE = L low stops F_{OUT} in the logic low state (F_{OUT} = L, $\overline{\text{FOUT}}$ = H).
GND	Supply	Supply	Ground	Negative power supply (GND).
V_{CC}	Supply	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation.
V_{CC_PLL}	Supply	Supply	V_{CC}	PLL positive power supply (analog power supply).

Table 2. Output Frequency Range and PLL Post-Divider N

N		Output Division	Output Frequency Range
N1	N0		
0	0	1	200 – 400 MHz
0	1	2	100 – 200 MHz
1	0	4	50 – 100 MHz
1	1	8	25 – 50 MHz

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	LQFP 32 Thermal Resistance Junction to Ambient Single layer test board Multi-layer test board			 67.8 55.9 50.1 47.9 42.1 39.4	 °C/W °C/W °C/W °C/W °C/W °C/W	 0 lfpm 200 lfpm 500 lfpm 0 lfpm 200 lfpm 500 lfpm
θ_{JC}	LQFP 32 Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1

Table 4. Absolute Maximum Ratings(1)

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs ($\overline{P\_LOAD}$, S_LOAD, S_DATA, S_CLOCK, M[0:8], N[0:1]. OE)						
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current(1)			±200	µA	V_{IN} = V_{CC} or GND
Differential Clock Output F_{OUT}(2)						
V_{OH}	Output High Voltage(3)	V_{CC}–1.11		V_{CC}–0.74	V	LVPECL
V_{OL}	Output Low Voltage(3)	V_{CC}–1.95		V_{CC}–1.60	V	LVPECL
Test and Diagnosis Output TEST						
V_{OH}	Output High Voltage(3)	2.0			V	I_{OH} = –0.8 mA
V_{OL}	Output Low Voltage(3)			0.55	V	I_{OH} = 0.8 mA
Supply Current						
I_{CC_PLL}	Maximum PLL Supply Current			8	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current			95	mA	All V_{CC} Pins

1. Inputs have pull-down resistors affecting the input current.
2. Outputs terminated 50 Ω to V_{TT} = V_{CC} – 2 V.
3. The MPC92469 TEST output levels are compatible to the MC12429 output levels.

Table 6. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal Interface Frequency Range		12		20	MHz	
f_{VCO}	VCO Frequency Range[2]		400		800	MHz	
f_{MAX}	Output Frequency	N = 00 (÷1) N = 01 (÷2) N = 10 (÷4) N = 11 (÷8)	200 100 50 25		400 200 100 50	MHz MHz MHz MHz	
DC	Output Duty Cycle		48	50	52	%	
t_r, t_f	Output Rise/Fall Time		0.05		0.3	ns	20% to 80%
f_{S_CLOCK}	Serial Interface Programming Clock Frequency[3]				10	MHz	
$t_{P,MIN}$	Minimum Pulse Width	(S_LOAD, $\overline{\text{P\_LOAD}}$)	50			ns	
t_S	Setup Time	S_DATA to S_CLOCK S_CLOCK to $\overline{\text{S\_LOAD}}$ M, N to $\overline{\text{P\_LOAD}}$	20 20 20			ns ns ns	
t_S	Hold Time	S_DATA to S_CLOCK M, N to $\overline{\text{P\_LOAD}}$	20 20			ns ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter				50	ps	N ≠ 8
$t_{JIT(PER)}$	Period Jitter				50	ps	N ≠ 8
t_{LOCK}	Maximum PLL Lock Time				10	ms	
SSM_{fmod}	Spread Spectrum Modulation Frequency			32		kHz	f_{XTAL} = 16 MHz
SSM_{dev}	Spread Spectrum Modulation Deviation	SS[3:0] = 0001 SS[3:0] = 1001		±0.30 -0.3	±0.5 -0.5	% %	f_{out} = 300 MHz f_{XTAL} = 16 MHz

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. The input frequency f_{XTAL} and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \times M \div 8$.
3. The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. See APPLICATIONS INFORMATION for more details.

PROGRAMMING INTERFACE

Programming the MPC92469

Programming the MPC92469 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at the output. The output frequency can be represented by this formula:

$$F_{OUT} = (f_{XTAL} \div 16) \times (M) \div (N) \quad (1)$$

where f_{XTAL} is the crystal frequency, M is the PLL feedback-divider and N is the PLL post-divider. The input frequency and the selection of the feedback divider M is limited by the VCO-frequency range. f_{XTAL} and M must be configured to match the VCO frequency range of 400 to 800 MHz in order to achieve stable PLL operation:

$$M_{MIN} = f_{VCO,MIN} \div f_{XTAL} * 8 \text{ and} \quad (2)$$

$$M_{MAX} = f_{VCO,MAX} \div f_{XTAL} * 8 \quad (3)$$

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between M = 200 and M = 400. Table 7 shows the usable VCO frequency and M divider range for other example input frequencies. Assuming that a 16 MHz input frequency is used, equation 1 reduces to:

$$F_{OUT} = M \div N \quad (4)$$

Table 7. MPC92469 Frequency Operating Range

M	M[8:0]	VCO frequency for a crystal interface frequency of					Output frequency for f_{XTAL} = 16 MHz and for N =			
		12	14	16	18	20	1	2	4	8
160	010100000					400				
170	010101010					425				
180	010110100				405	450				
190	010111110				427.5	475				
200	011001000			400	450	500	200	100	50	25
210	011010010			420	472.5	525	210	105	52.5	26.25
220	011011100			440	495	550	220	110	55	27.50
230	011100110		402.5	460	517.5	575	230	115	57.5	28.75
240	011110000		420	480	540	600	240	120	60	30
250	011111010		437.5	500	562.5	625	250	125	62.5	31.25
260	100000100		455	520	585	650	260	130	65	32.50
270	100001110	405	472.5	540	607.5	675	270	135	67.5	33.75
280	100011000	420	490	560	630	700	280	140	70	35
290	100100010	435	507.5	580	652.5	725	290	145	72.5	36.25
300	100101100	450	525	600	675	750	300	150	75	37.5
310	100110110	465	542.5	620	697.5	775	310	155	77.5	38.75
320	101000000	480	560	640	720	800	320	160	80	40
330	101001010	495	577.5	660	742.5		330	165	82.5	41.25
340	101010100	510	595	680	765		340	170	85	42.5
350	101011110	525	612.5	700	787.5		350	175	87.5	43.75
360	101101000	540	630	720			360	180	90	45
370	101110010	555	647.5	740			370	185	92.5	46.25
380	101111100	570	665	760			380	190	95	47.5
390	110000110	585	682.5	780			390	195	97.5	48.75
400	110010000	600	700	800			400	200	100	50
410	110011010	615	717.5							
420	110100100	630	735							
430	110101110	645	752.5							
440	110111000	660	770							
450	111000010	675	787.5							
510	111111110	765								

Substituting N for the four available values for N (1, 2, 4, 8) yields:

Table 8. Output Frequency Range for f_{XTAL} = 16 MHz

N			F_{OUT}	F_{OUT} Range	F_{OUT} Step
1	0	Value			
0	0	1	M	200 – 400 MHz	1 MHz
0	1	2	M÷2	100 – 200 MHz	500 kHz
1	0	4	M÷4	50 – 100 MHz	250 kHz
1	1	8	M÷8	25 – 50 MHz	125 kHz

Example Frequency Calculation for an 16 MHz Input Frequency

If an output frequency of 131 MHz was desired the following steps would be taken to identify the appropriate M and N values. According to Table 8, 131 MHz falls in the frequency set by an value of 2 so N[1:0] = 01. For N = 2 the output frequency is F_{OUT} = M ÷ 2 and M = F_{OUT} x 2. Therefore M = 2 x 131 = 262, so M[8:0] = 100000110. Following this procedure a user can generate any whole frequency between 25 MHz and 400 MHz. Note than for N > 2 fractional values of can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies achievable) will be equal to:

$$f_{STEP} = f_{XTAL} \div 16 \div N \quad (5)$$

APPLICATIONS INFORMATION

Using the Parallel and Serial Interface

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the P_LOAD signal such that a LOW-to-HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the P_LOAD signal is LOW the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the P_LOAD signal must be HIGH for the serial load operation to function. The SSM register is loaded with the first four bits, the Test register is loaded with the next three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH-to-LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 3 illustrates the timing diagram for both a parallel and a serial load of the MPC92469 synthesizer. M[8:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

Using the Test and Diagnosis Output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents F_{OUT}, the CMOS output is not able to toggle fast enough for higher output frequencies and should only be used for test and diagnosis. The T2, T1 and T0 control bits are preset to '000' when P_LOAD is LOW so that the PECL FOUT outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin. Most of the signals available on the TEST output pin are useful only for performance verification of the MPC92469 itself. However the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MPC92469 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the F_{OUT} differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving F_{OUT} directly gives the user more control on the test clocks sent through the clock tree. Because the S_CLOCK is a CMOS level the input frequency is limited to 200 MHz. This means the fastest the F_{OUT} pin can be toggled via the S_CLOCK is 100 MHz as the divide ratio of the Post-PLL divider is 2 (if N = 1). Note that the M counter output on the TEST output will not be a 50% duty cycle.

Table 9. Test and Debug Configuration for TEST

T[2:0]			TEST Output
T2	T1	T0	
0	0	0	18-bit shift register out(1)
0	0	1	Logic 1
0	1	0	f_{XTAL} ÷ 16
0	1	1	M-Counter out
1	0	0	FOUT
1	0	1	Logic 0
1	1	0	M-Counter out in PLL-bypass mode
1	1	1	FOUT ÷ 4

1. Clocked out at the rate of S_CLOCK.

Table 10. Debug Configuration for PLL Bypass(1)

Output	Configuration
F_{OUT}	S_CLOCK ÷ N
TEST	M-Counter out(2)

1. T[2:0] = 110. AC specifications do not apply in PLL bypass mode.
2. Clocked out at the rate of S_CLOCK÷(4·N)

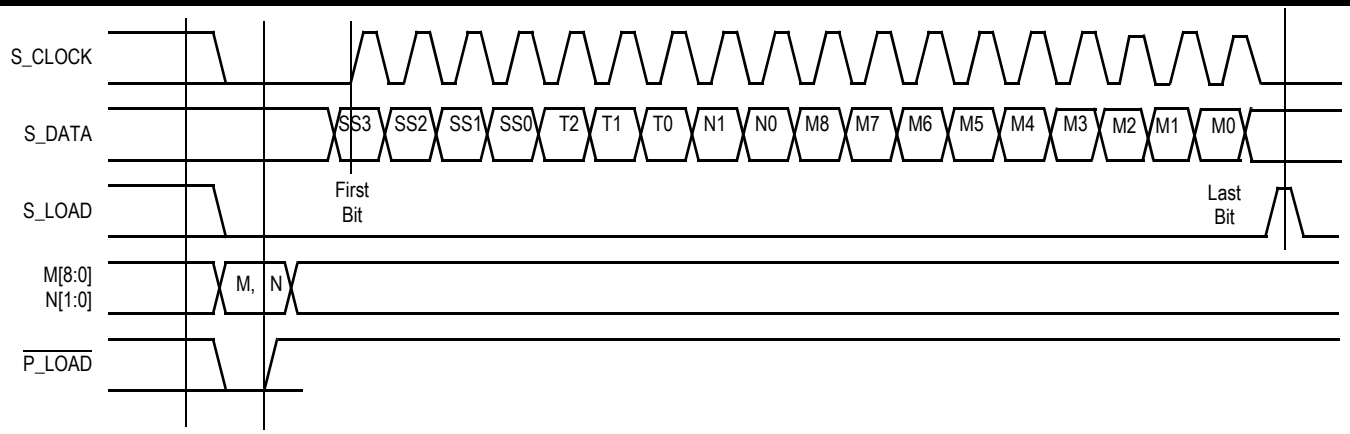

Figure 3. Serial Interface Timing Diagram

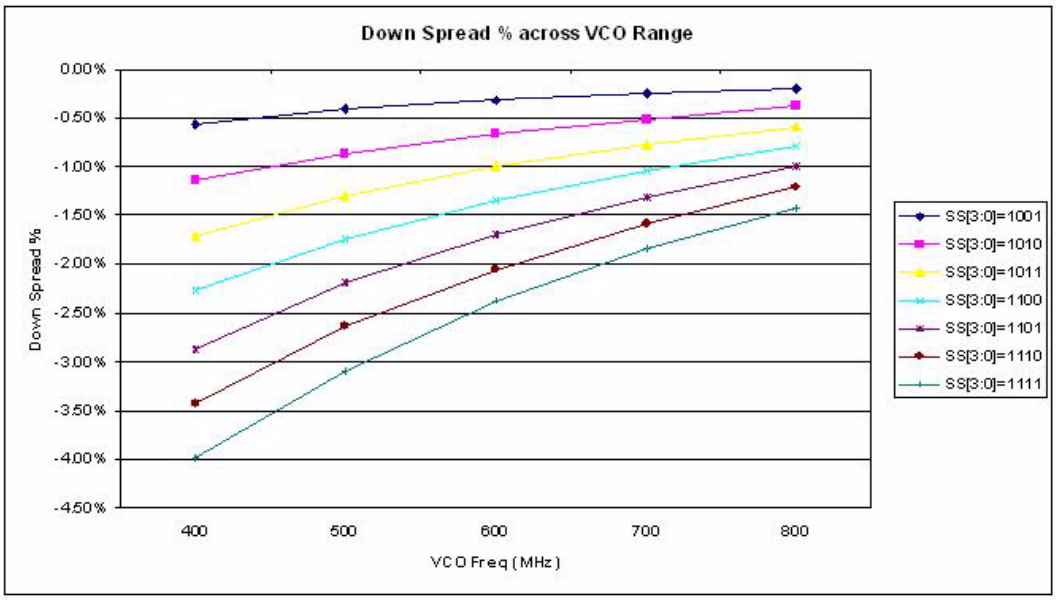

Figure 4. Down Spread % across VCO Range with 16 MHz Reference

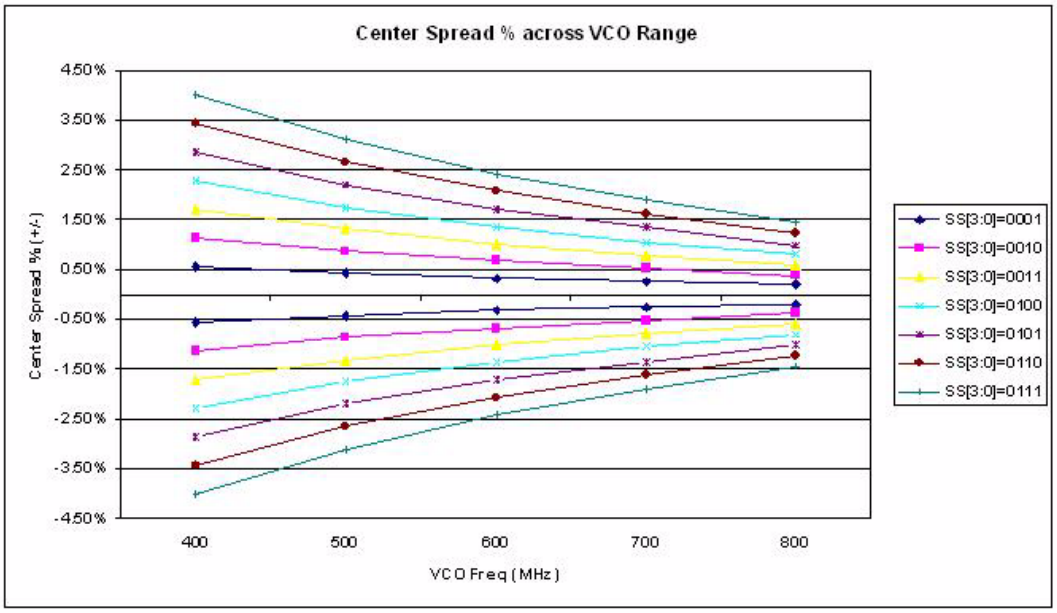

Figure 5. Center Spread % across VCO Range with 16 MHz Reference

Spread Spectrum Modulation

The MPC92469 offers the option of a spread spectrum (SSM) output clock and is controlled by four bits in the serial load bit stream. These four bits configure the SSM to be enabled, the type of spread and the amount of spread modulation to be selected. Table 11 shows the definition of these four bits. These spread control bits are located at the beginning of the serial data stream and are labeled SS3, SS2, SS1 and SS0. The initial state of these four bits (SS3:SS0) is 0000 which places the MPC92469 in the configuration of SSM being off. Any parallel load operation will also result in the spread spectrum modulation programming being reset to the value 0000 which likewise turns spread spectrum modulation off. The MPC92469 offers down-spread or center spread.

Figure 4 and Figure 5 show the amount of spread based upon both the VCO frequency and the Spread Spectrum control bit pattern. Figure 4 is for down-spread with 0% spread being at the top of the figure. Figure 5 is for center-spread with 0% spread in the middle of the figure. Increasing values of SS2:SS0 increase the amount of spread and SS3 is used to configure either center-spread (SS3=0) or down-spread (SS3=1). Note, for both tables, the horizontal axis is the VCO frequency which ranges from 400MHz to 800MHz. The VCO frequency is 2X the output frequency which corresponds to an output frequency range of 200MHz to 400MHz for the output divider of N=1.

Table 11. SSM Operation

SS Bit Pattern				Operation
SS3	**SS2**	**SS1**	**SS0**	**Mode**
0	0	0	0	off
0	0	0	1	center-spread (increasing amount)
•	•	•	•	
0	1	1	1	
1	0	0	0	off
1	0	0	1	down-spread (increasing amount)
•	•	•	•	
1	1	1	1	

Power Supply Filtering

The MPC92469 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} pin impacts the device characteristics. The MPC92469 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (V_{CC_PLL}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC92469. Figure 6 illustrates a typical power supply filter scheme. The MPC92469 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CC_PLL} pin of the MPC92469. From the data sheet, the V_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is maximum 8 mA, assuming that a minimum of 3.0 V must be maintained on the V_{CC_PLL} pin. The resistor shown in Figure 6 must have a resistance of 10-15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

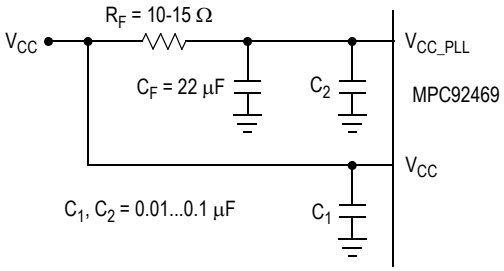

Figure 6. V_{CC_PLL} Power Supply Filter

Additional noise suppression may be achieved with the use of a ferrite chip bead. The ferrite chip bead offers a high value of RF impedance while maintaining a very low DC resistance. Ferrite beads are available from 15 Ω to over 1k Ω RF impedance (measured @ 100 MHz), but would have DC resistance values of less than 1 Ω. Max current ratings range from a few hundred mA to over 1 A. The selected bead should have a max current rating well in excess of the actual circuit requirements preventing saturation of the ferrite material. The ferrite chip bead is placed in series with a low value resistor as shown in Figure 7. Capacitor values should be staggered in value by a factor of 5 to 10. Proper curcuit modeling should be performed to optimize circuit components in specific user applications.

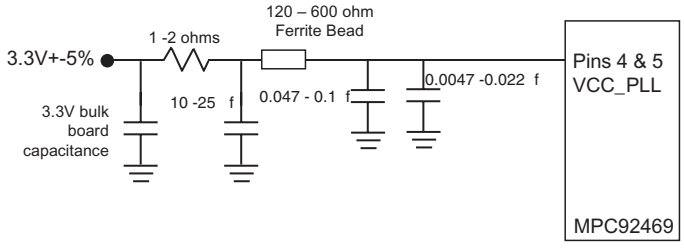

Figure 7. V_{CC_PLL} Power Supply Filter Using a Ferrite Bead

Using the On-Board Crystal Oscillator

The MPC92469 features a fully integrated Pierce oscillator to minimize system implementation costs. The MPC92469 may be operated with a 12 MHz to 20 MHz crystal and without additional components. Recommended operation for the crystal should be of a parallel resonant type and a load specification of C_L = 18 pF. See Table 12 for complete crystal specifications.

If more precise frequency control is desired, the addition of capacitors from each of the XTAL_IN and XTAL_OUT pins to ground may be used to trim the frequency as shown in Figure 8.

The crystal and optional trim capacitors should be located as close to the MPC92469 XTAL_IN and XTAL_OUT pins as possible to avoid any board level parasitic.

Table 12. Recommended Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Parrallel Resonance
Shunt Capacitance (C_L)	5–7 pF

Table 12. Recommended Crystal Specifications

Load Capacitance (C_O)	18 pF
Equivalent Series Resistance (ESR)	20 to 50 Ω

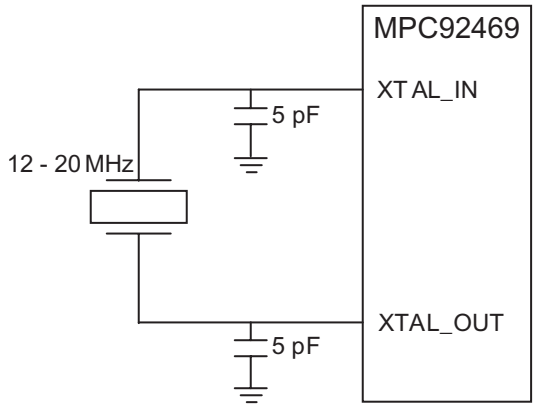

Figure 8. Crystal Oscillator With Trim Capacitor

Figure 9. Package Drawing for 32 Lead LQFP

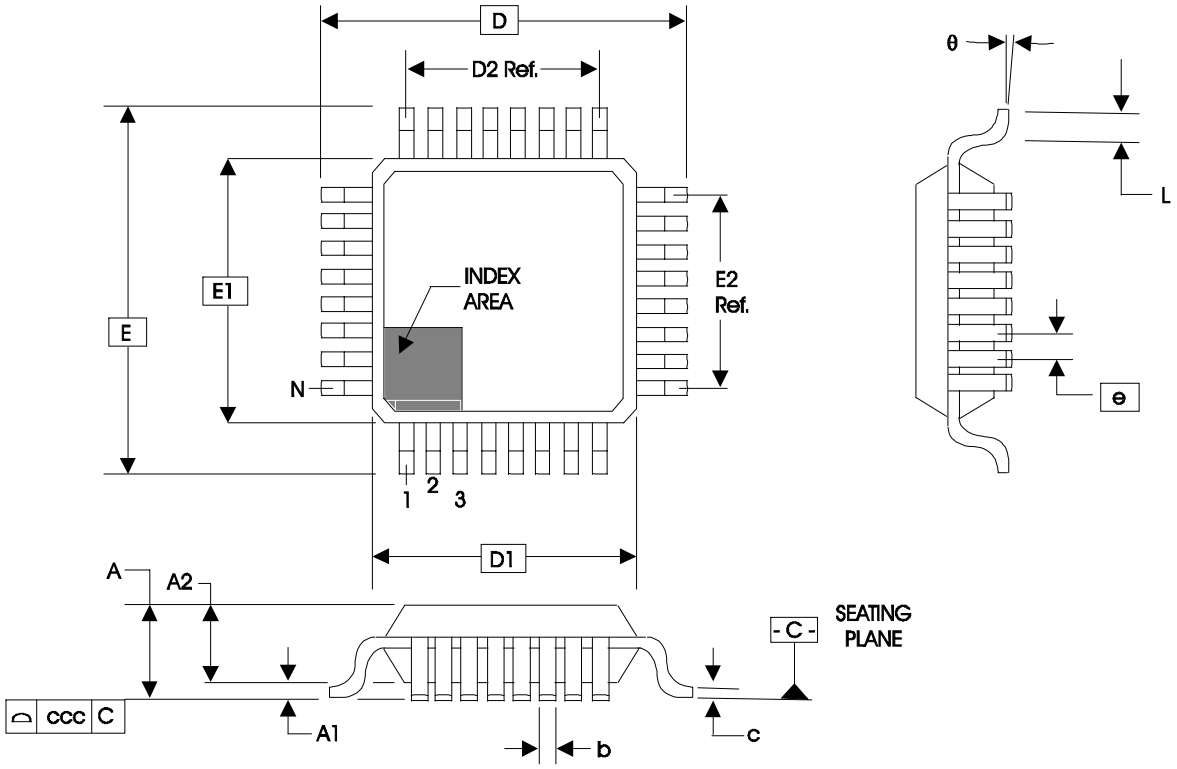

Table 13. Package Dimensions for 32Lead LQFP

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBA		
	MINIMUM	NOMINAL	MAXIMUM
N	32		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.60 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.60 Ref.		
e	0.80 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.10

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