

Product Preview

1360 MHz Dual Output LVPECL Clock Synthesizer

The MPC92432 is a 3.3V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking, and computing applications. With output frequencies from 21.25 MHz to 1360 MHz and the support of two differential PECL output signals, the device meets the needs of the most demanding clock applications.

Features

- 21.25 MHz to 1360 MHz synthesized clock output signal
- Two differential, LVPECL-compatible high-frequency outputs
- Output frequency programmable through 2-wire I²C bus or parallel interface
- On-chip crystal oscillator for reference frequency generation
- Alternative LVCMOS compatible reference clock input
- Synchronous clock stop functionality for both outputs
- LOCK indicator output (LVCMOS)
- LVCMOS compatible control inputs
- Fully integrated PLL
- 3.3-V power supply
- 48-lead LQFP
- SiGe Technology
- Ambient temperature range: -40°C to +85 °C

Applications

- Programmable clock source for server, computing, and telecommunication systems
- Frequency margining
- Oscillator replacement

Functional Description

The MPC92432 is a programmable high-frequency clock source (clock synthesizer). The internal PLL generates a high-frequency output signal based on a low-frequency reference signal. The frequency of the output signal is programmable and can be changed on the fly for frequency margining purpose.

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. Alternatively, a LVCMOS compatible clock signal can be used as a PLL reference signal. The frequency of the internal crystal oscillator is divided by a selectable divider and then multiplied by the PLL. The VCO within the PLL operates over a range of 1360 to 2720 MHz. Its output is scaled by a divider that is configured by either the I²C or parallel interfaces. The crystal oscillator frequency f_{XTAL} , the PLL pre-divider P, the feedback-divider M, and the PLL post-divider N determine the output frequency. The feedback path of the PLL is internal.

The PLL post-divider N is configured through either the I²C or the parallel interfaces, and can provide one of six division ratios (2, 4, 8, 16, 32, 64). This divider extends the performance of the part while providing a 50% duty cycle. The high-frequency outputs, Q_A and Q_B, are differential and are capable of driving a pair of transmission lines terminated 50 Ω to V_{CC} - 2.0 V. The second high-frequency output, Q_B, can be configured to run at either 1x or 1/2x of the clock frequency or the first output (Q_A). The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: I²C and parallel. The parallel interface uses the values at the M[9:0], NA[2:0], NB, and P parallel inputs to configure the internal PLL dividers. The parallel programming interface has priority over the serial I²C interface. The serial interface is I²C compatible and provides read and write access to the internal PLL configuration registers. The lock state of the PLL is indicated by the LVCMOS-compatible LOCK outputs.

This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

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MPC92432

1360 MHz LOW VOLTAGE CLOCK SYNTHESIZER



FA SUFFIX
48-LEAD LQFP PACKAGE
CASE 932

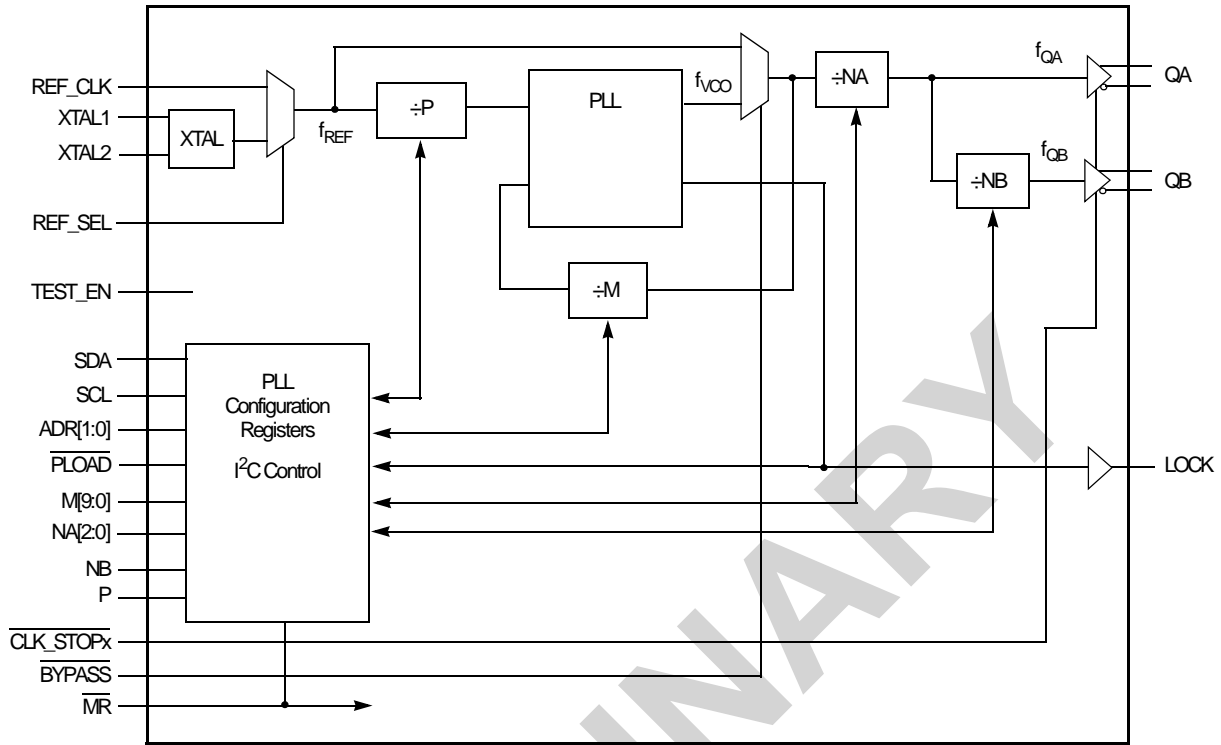


Figure 1. MPC92432 — Generic Logic Diagram

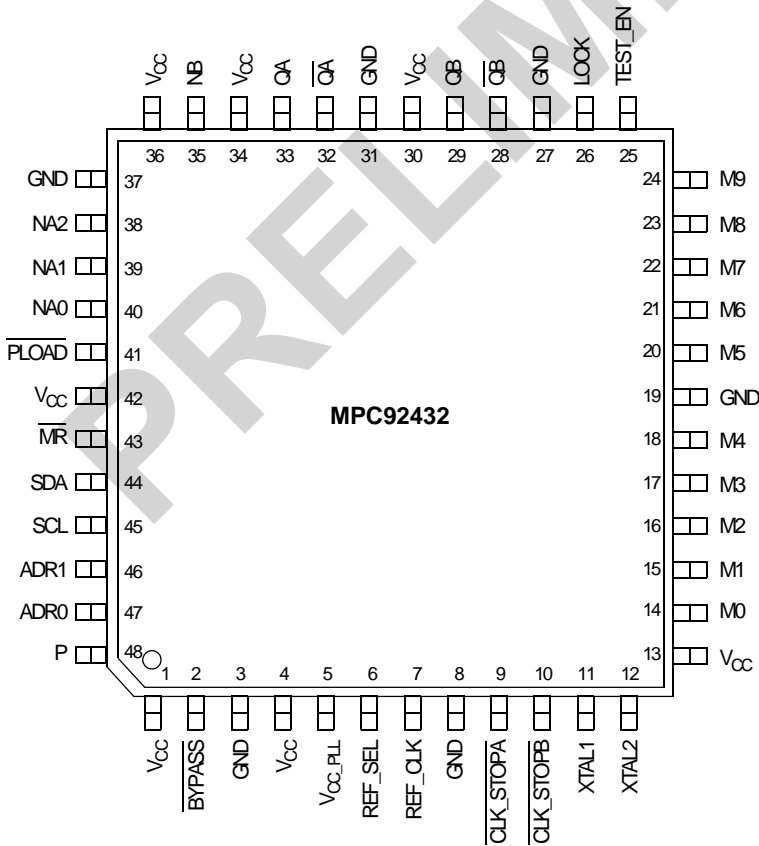


Figure 2. 48-Lead Package Pinout (Top View)

It is recommended to use an external RC filter for the analog V_{CC_PLL} supply pin. Please see the application section for details.

Table 1. Signal Configuration

| Pin | I/O | Type | Function |
|-------------------------|--------|---------------------|---|
| XTAL1, XTAL2 | Input | Analog | Crystal oscillator interface |
| REF_CLK | Input | LVC MOS | PLL external reference input |
| REF_SEL | Input | LVC MOS | Selects the reference clock input |
| QA | Output | Differential LVPECL | High frequency clock output |
| QB | Output | Differential LVPECL | High frequency clock output |
| LOCK | Output | LVC MOS | PLL lock indicator |
| M[9:0] | Input | LVC MOS | PLL feedback divider configuration |
| NA[2:0] | Input | LVC MOS | PLL post-divider configuration for output QA |
| NB | Input | LVC MOS | PLL post-divider configuration for output QB |
| P | Input | LVC MOS | PLL pre-divider configuration |
| $\overline{P_LOAD}$ | Input | LVC MOS | Selects the programming interface |
| SDA | I/O | LVC MOS | I ² C data |
| SCL | Input | LVC MOS | I ² C clock |
| ADR[1:0] | Input | LVC MOS | Selectable two bits of the I ² C slave address |
| \overline{BYPASS} | Input | LVC MOS | Selects the static circuit bypass mode |
| TEST_EN | Input | LVC MOS | Factory test mode enable. This input must be set to logic low level in all applications of the device. |
| $\overline{CLK_STOPx}$ | Input | LVC MOS | Output Qx disable in logic low state |
| \overline{MR} | Input | LVC MOS | Device master reset |
| GND | Supply | Ground | Negative power supply |
| V _{CC_PLL} | Supply | V _{CC} | Positive power supply for the PLL (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V _{CC_PLL} . |
| V _{CC} | Supply | V _{CC} | Positive power supply for I/O and core |

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PRELIMINARY

Table 2. Function Table

| Control | Default ¹ | 0 | 1 |
|--------------------------------|----------------------------|--|---|
| Inputs | | | |
| REF_SEL | 1 | Selects REF_CLK input as PLL reference clock | Selects the XTAL interface as PLL reference clock |
| M[9:0] | 01 1111 0100b ² | PLL feedback divider (10-bit) parallel programming interface | |
| NA[2:0] | 010 | PLL post-divider parallel programming interface. See Table 9 | |
| NB | 0 | PLL post-divider parallel programming interface. See Table 10 | |
| P | 1 | PLL pre-divider parallel programming interface. See Table 8 | |
| $\overline{\text{PLOAD}}$ | 0 | Selects the parallel programming interface. The internal PLL divider settings (M, NA, NB and P) are equal to the setting of the hardware pins. Leaving the M, NA, NB and P pins open (floating) results in a default PLL configuration with $f_{\text{OUT}} = 250$ MHz. See application/programming section. | Selects the serial (I ² C) programming interface. The internal PLL divider settings (M, NA, NB and P) are set and read through the serial interface. |
| ADR[1:0] | 00 | Address bit = 0 | Address bit = 1 |
| SDA, SCL | | See Programming the MPC92432 | |
| BYPASS | 1 | PLL function bypassed $f_{\text{QA}} = f_{\text{REF}} \div N_{\text{A}}$ and $f_{\text{QB}} = f_{\text{REF}} \div (N_{\text{A}} \cdot N_{\text{B}})$ | PLL function enabled $f_{\text{QA}} = (f_{\text{REF}} \div P) \cdot M \div N_{\text{A}}$ and $f_{\text{QB}} = (f_{\text{REF}} \div P) \cdot M \div (N_{\text{A}} \cdot N_{\text{B}})$ |
| TEST_EN | 0 | Application mode. Test mode disabled. | Factory test mode is enabled |
| $\overline{\text{CLK_STOPx}}$ | 1 | Output Qx is disabled in logic low state. Synchronous disable is only guaranteed if NB = 0. | Output Qx is synchronously enabled |
| $\overline{\text{MR}}$ | | The device is reset. The output frequency is zero and the outputs are asynchronously forced to logic low state. After releasing reset (upon the rising edge of $\overline{\text{MR}}$ and independent on the state of $\overline{\text{PLOAD}}$), the MPC92432 reads the parallel interface (M, NA, NB and P) to acquire a valid startup frequency configuration. See application/programming section. | The PLL attempts to lock to the reference signal. The t_{LOCK} specification applies. |
| Outputs | | | |
| LOCK | | PLL is not locked | PLL is frequency locked |

1. Default states are set by internal input pull-up or pull-down resistors of 75 k Ω
2. If $f_{\text{REF}} = 16$ MHz, the default configuration will result in a output frequency of 250 MHz

Table 3. General Specifications

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---------------|---|------|--------------|-----|------|--|
| V_{TT} | Output Termination Voltage | — | $V_{CC} - 2$ | — | V | |
| MM | ESD Protection (Machine model) | 200 | — | — | V | |
| HBM | ESD Protection (Human body model) | 2000 | — | — | V | |
| LU | Latch-Up Immunity | 200 | — | — | mA | |
| C_{IN} | Input Capacitance | — | 4.0 | — | pF | Inputs |
| θ_{JA} | Thermal Resistance Junction to Ambient JESD 51-3, single layer test board JESD 51-6, 2S2P multilayer test board | — | — | TBD | °C/W | Natural convection 100 ft/min 200 ft/min 400 ft/min 800 ft/min Natural convection 100 ft/min 200 ft/min 400 ft/min 800 ft/min |
| θ_{JC} | LQFP 32 Thermal Resistance Junction to Case | — | — | TBD | °C/W | MIL-SPEC 883E Method 1012.1 |

Table 4. Absolute Maximum Ratings¹

| Symbol | Characteristics | Min | Max | Unit | Condition |
|-----------|---------------------|------|----------------|------|-----------|
| V_{CC} | Supply Voltage | -0.3 | 3.9 | V | |
| V_{IN} | DC Input Voltage | -0.3 | $V_{CC} + 0.3$ | V | |
| V_{OUT} | DC Output Voltage | -0.3 | $V_{CC} + 0.3$ | V | |
| I_{IN} | DC Input Current | — | ±20 | mA | |
| I_{OUT} | DC Output Current | — | ±50 | mA | |
| T_S | Storage temperature | -65 | 125 | °C | |

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics ($V_{CC} = 3.3\text{ V} \pm 5\%$, $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|--|-----------------------------|-----------------|-----|-----------------|---------------|--------------------------|
| LVCMOS Control Inputs (M[9:0], N[2:0], ADDR[1:0], NB, P, $\overline{\text{CLK_STOP}}$, $\overline{\text{BYPASS}}$, $\overline{\text{MR}}$, REF_SEL, TEST_EN, $\overline{\text{PLOAD}}$) | | | | | | |
| V_{IH} | Input High Voltage | 2.0 | — | $V_{CC} + 0.3$ | V | LVCMOS |
| V_{IL} | Input Low Voltage | — | — | 0.8 | V | LVCMOS |
| I_{IN} | Input Current ¹ | — | — | ± 200 | μA | $V_{IN} = V_{CC}$ or GND |
| I ² C Inputs (SCL, SDA) | | | | | | |
| V_{IH} | Input High Voltage | 2.0 | — | $V_{CC} + 0.3$ | V | LVCMOS |
| V_{IL} | Input Low Voltage | — | — | 0.8 | V | LVCMOS |
| I_{IN} | Input Current | — | — | ± 10 | μA | |
| LVCMOS Output (LOCK) | | | | | | |
| V_{OH} | Output High Voltage | 2.4 | — | — | V | $I_{OH} = -4\text{ mA}$ |
| V_{OL} | Output Low Voltage | — | — | 0.4 | V | $I_{OL} = 4\text{ mA}$ |
| I ² C Open-Drain Output (SDA) | | | | | | |
| V_{OL} | Input Low Voltage | — | — | 0.4 | V | $I_{OL} = 4\text{ mA}$ |
| Differential Clock Output QA, QB ² | | | | | | |
| V_{OH} | Output High Voltage | $V_{CC} - 1.05$ | — | $V_{CC} - 0.74$ | V | LVPECL |
| V_{OL} | Output Low Voltage | $V_{CC} - 1.95$ | — | $V_{CC} - 1.60$ | V | LVPECL |
| $V_{O(P-P)}$ | Output Peak-to-Peak Voltage | 0.5 | 0.6 | 1.0 | V | |
| Supply current | | | | | | |
| I_{CC_PLL} | Maximum PLL Supply Current | — | — | TBD | mA | V_{CC_PLL} Pins |
| I_{CC} | Maximum Supply Current | — | — | TBD | mA | All V_{CC} Pins |

- Inputs have pull-down resistors affecting the input current.
- Outputs terminated $50\ \Omega$ to $V_{TT} = V_{CC} - 2\text{ V}$

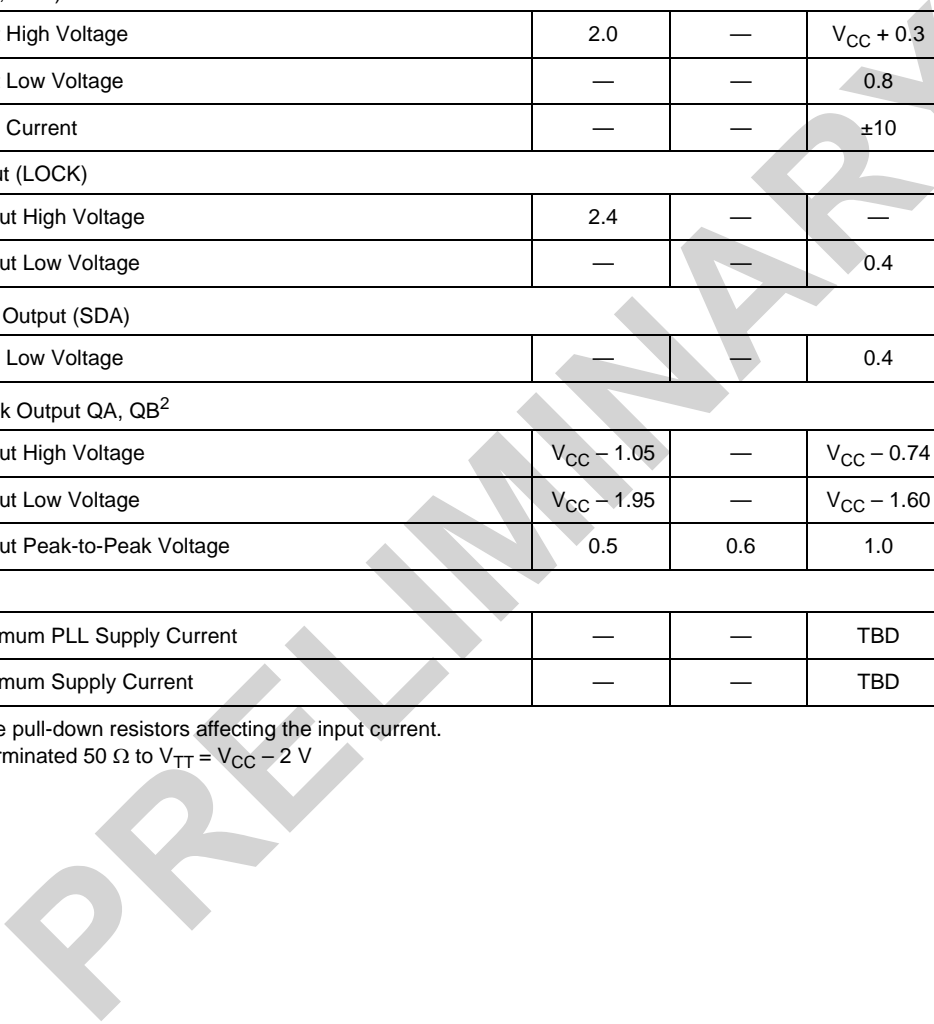


Table 6. AC Characteristics ($V_{CC} = 3.3\text{ V} \pm 5\%$, $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$)^{1 2}

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---------------|--|----------------------------|-------|----------------------|------|-----------------------|
| f_{XTAL} | Crystal Interface Frequency Range | 15 | 16 | 20 | MHz | |
| f_{REF} | FREF_EXT Reference Frequency Range | 15 | — | 20 | MHz | |
| f_{VCO} | VCO Frequency Range ³ | 1360 | — | 2720 | MHz | |
| f_{MAX} | Output Frequency ⁴ | N= ÷2 | 680 | — | 1360 | MHz |
| | | N= ÷4 | 340 | — | 680 | MHz |
| | | N= ÷8 | 170 | — | 340 | MHz |
| | | N= ÷16 | 85 | — | 170 | MHz |
| | | N= ÷32 | 42.5 | — | 85 | MHz |
| | | N= ÷64 | 21.25 | — | 42.5 | MHz |
| f_{SCL} | Serial Interface (I ² C) Clock Frequency | 0 | — | 0.4 | MHz | |
| t_{P_MIN} | Minimum Pulse Width (P_LOAD) | 50 | — | — | ns | |
| DC | Output Duty Cycle | 45 | 50 | 55 | % | |
| $t_{SK(O)}$ | Output-to-Output Skew | Same frequency | — | — | 25 | ps |
| | | Different frequency | — | 50 | — | ps |
| t_r, t_f | Output Rise/Fall Time (QA, QB) | 0.05 | — | 0.3 | ns | 20% to 80% |
| t_r, t_f | Output Rise/Fall Time (SDA) | — | — | 250 | ns | $C_L = 400\text{ pF}$ |
| t_{P_EN} | Output Enable Time ($\overline{\text{CLKSTOPx}}$ to QA, QB) | T_{FOUT} | — | $2 \cdot T_{FOUT}$ | — | T = period of Qx |
| t_{P_DIS} | Output Enable Time ($\overline{\text{CLKSTOPx}}$ to QA, QB) | $0.5 \cdot T_{FOUT}$ | — | $1.5 \cdot T_{FOUT}$ | — | T = period of Qx |
| $t_{JIT(CC)}$ | Cycle-to-Cycle Jitter | N= ÷2 | — | — | TBD | ps |
| | | N= ÷4 | — | — | TBD | ps |
| | | N= ÷8 | — | — | 25 | ps |
| | | N= ÷16 | — | — | 25 | ps |
| | | N= ÷32 | — | — | TBD | ps |
| | | N= ÷64 | — | — | TBD | ps |
| $t_{JIT(CC)}$ | Period Jitter (RMS) | $f_{OUT} = 250\text{ MHz}$ | — | — | 10 | ps |
| | | Any other frequency | — | — | TBD | ps |
| t_{LOCK} | Maximum PLL Lock Time | — | — | 10 | ms | |

- AC specifications are subject to change
- AC characteristics apply for parallel output termination of $50\ \Omega$ to V_{TT}
- The input frequency f_{XTAL} , the PLL divider M and P must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot M \div P$. The feedback divider M is limited to $170 \leq M \leq 340$ (for $P = 2$) and $340 \leq M \leq 680$ (for $P = 4$) for stable PLL operation
- Output frequency for Q_A, Q_B if $N_B=0$. With $N_B=1$ the Q_B output frequency is half of the Q_A output frequency

APPLICATION INFORMATION

Output Frequency Configuration

The MPC92432 is a programmable frequency source (synthesizer) and supports an output frequency range of 21.25 – 1360 MHz. The output frequency f_{OUT} is a function of the reference frequency f_{REF} and the three internal PLL dividers P, M, and N. f_{OUT} can be represented by this formula:

$$f_{OUT} = (f_{REF} \div P) \cdot M \div (N_A \cdot B) \quad (1)$$

The M, N and P dividers require a configuration by the user to achieve the desired output frequency. The output divider, N_A , determines the achievable output frequency range (see **Table 7**). The PLL feedback-divider M is the frequency multiplication factor and the main variable for frequency synthesis. For a given reference frequency f_{REF} , the PLL feedback-divider M must be configured to match the specified VCO frequency range in order to achieve a valid PLL configuration:

$$f_{VCO} = (f_{REF} \div P) \cdot M \text{ and} \quad (2)$$

$$1360 \leq f_{VCO} \leq 2720 \quad (3)$$

The output frequency may be changed at any time by changing the value of the PLL feedback divider M. The smallest possible output frequency change is the synthesizer granularity G (difference in f_{OUT} when incrementing or decrementing M). At a given reference frequency, G is a function of the PLL pre-divider P and post-divider N:

$$G = f_{REF} \div (P \cdot N_{A,B}) \quad (4)$$

The N_B divider configuration determines if the output Q_B generates a 1:1 or 2:1 frequency copy of the Q_A output signal. The purpose of the PLL pre-divider P is to situated the PLL into the specified VCO frequency range f_{VCO} (in combination with M). For a given output frequency, $P = 4$ results in a smaller output frequency granularity G, $P = 2$ results a larger output frequency granularity G and also increases the PLL bandwidth compared to the $P = 2$ setting.

The following example illustrates the output frequency range of the MPC92432 using a 16-MHz reference frequency.

Table 7. Frequency Ranges ($f_{REF} = 16 \text{ MHz}$)

| $f_{OUT} (Q_A)$ [MHz] | N_A | M | P | G [MHz] |
|-----------------------|----------|-----------|---|---------|
| 680 – 1360 | $N_A=2$ | 170 – 340 | 2 | 4 |
| | | 340 – 680 | 4 | 2 |
| 340 – 680 | $N_A=4$ | 170 – 340 | 2 | 2 |
| | | 340 – 680 | 4 | 1 |
| 170 – 340 | $N_A=8$ | 170 – 340 | 2 | 1 |
| | | 340 – 680 | 4 | 0.5 |
| 85 – 170 | $N_A=16$ | 170 – 340 | 2 | 0.5 |
| | | 340 – 680 | 4 | 0.25 |
| 42.5 – 85 | $N_A=32$ | 170 – 340 | 2 | 0.25 |
| | | 340 – 680 | 4 | 0.125 |
| 21.25 – 42.5 | $N_A=64$ | 170 – 340 | 2 | 0.125 |
| | | 340 – 680 | 4 | 0.0625 |

Example Output Frequency Configuration

If a reference frequency of 16 MHz is available, an output frequency at Q_A of 250 MHz and a small frequency granularity is desired, the following steps would be taken to identify the appropriate P, M, and N configuration:

1. Use **Table 7** to select the output divider, N_A , that matches the desired output frequency or frequency range. According to **Table 7**, a target output frequency of 250 MHz falls in the f_{OUT} range of 170 to 340 MHz and requires to set $N_A = 8$
2. Calculate the VCO frequency $f_{VCO} = f_{OUT} \cdot N_A$, which is 2000 MHz in this example.
3. Determine the PLL feedback divider: $M = f_{VCO} \div P$. The smallest possible output granularity in this example calculation is 500 kHz (set $P = 4$). M calculates to a value of $2000 \div 4 = 500$.
4. Configure the MPC92432 with the obtained settings:
 - $M[9:0] = 0111110100b$ (binary number for $M=500$)
 - $N_A[2:0] = 010$ ($\div 8$ divider, see **Table 9**)
 - $P = 1$ ($\div 4$ divider, see **Table 8**)
 - $N_B = 0$ ($f_{OUT, QB} = f_{OUT, QA}$)
5. Use either parallel or serial interface to apply the setting. The I²C configuration byte for this examples are: $PLL_H=01010010b$ and $PLL_L=11110100b$. See **Table 14** and **Table 15** for register maps.

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PLL Divider Configuration

Table 8. Pre-PLL Divider P

| P | Value |
|---|------------------|
| 0 | $f_{REF} \div 2$ |
| 1 | $f_{REF} \div 4$ |

Table 9. Post-PLL Divider N_A

| N _{A0} | N _{A1} | N _{A2} | f _{OUT} (Q _A) |
|-----------------|-----------------|-----------------|------------------------------------|
| 0 | 0 | 0 | $f_{VCO} \div 2$ |
| 0 | 0 | 1 | $f_{VCO} \div 4$ |
| 0 | 1 | 0 | $f_{VCO} \div 8$ |
| 0 | 1 | 1 | $f_{VCO} \div 16$ |
| 1 | 0 | 0 | $f_{VCO} \div 32$ |
| 1 | 0 | 1 | $f_{VCO} \div 64$ |

Table 10. Post-PLL Divider N_B

| N _B | Value |
|----------------|------------------------------------|
| 0 | $f_{OUT, QB} = f_{OUT, QA}$ |
| 1 | $f_{OUT, QB} = f_{OUT, QA} \div 2$ |

Programming the MPC92432

The MPC92432 has a parallel and a serial configuration interface. The purpose of the parallel interface is to directly configure the PLL dividers through hardware pins without the overhead of a serial protocol. At device startup, the device always obtains an initial PLL frequency configuration through the parallel interface. The parallel interface does not support reading the PLL configuration.

The serial interface is I²C compatible. It allows reading and writing device settings by accessing internal device registers. The serial interface is designed for host-controller access to the synthesizer frequency settings for instance in frequency-margining applications.

Using the Parallel Interface

The parallel interface supports write-access to the PLL frequency setting directly through 15 configuration pins (P, M[9:0], NA[2:0], and NB). The parallel interface must be enabled by setting PLOAD to logic low level. During PLOAD = 0, any change of the logical state of the P, M[9:0], NA[2:0], and NB pins will immediately affect the internal PLL divider settings, resulting in a change of the internal VCO-frequency and the output frequency. The parallel interface mode disables the I²C write-access to the internal registers; however, I²C read-access to the internal configuration registers is enabled.

Upon startup, when the device reset signal is released (rising edge of the MR signal), the device reads its startup configuration through the parallel interface and independent on the state of PLOAD. It is recommended to provide a valid PLL configuration for startup. If the parallel interface pins are left open, a default PLL configuration will be loaded. After the low-to-high transition of PLOAD, the configuration pins have no more effect and the configuration registers are made accessible through the serial interface.

Table 11. PLL Feedback-Divider Configuration (M)

| Feedback Divider M | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|----|----|----|----|----|----|----|----|----|----|
| Pin | M9 | M8 | M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 |
| Default | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

Table 12. PLL Pre/Post-Divider Configuration (N, P)

| Post-D. NA | 2 | 1 | 0 | Post-D. NB | NB | Pre-D. P | P |
|------------|-----|-----|-----|------------|----|----------|---|
| Pin | NA2 | NA1 | NA0 | Pin | NB | Pin | P |
| Default | 0 | 1 | 1 | Default | 0 | Default | 1 |

Using the I²C Interface

PLOAD = 1 enables the programming and monitoring of the internal registers through the I²C interface. Device register access (write and read) is possible through the 2-wire interface using SDA (configuration data) and SCL (configuration clock) signals. The MPC92432 acts as a slave device at the I²C bus. For further information on I²C it is recommended to refer to the I²C bus specification (version 2.1).

PLOAD = 0 disables the I²C-write-access to the configuration registers and any data written into the register is ignored. However, the MPC92432 is still visible at the I²C interface and I²C transfers are acknowledged by the device. Read-access to the internal registers during PLOAD = 0 (parallel programming mode) is supported.

Note that the device automatically obtains a configuration using the parallel interface upon the release of the device reset (rising edge of MR) and independent on the state of PLOAD. Changing the state of the PLOAD input is not supported when the device performs any transactions on the I²C interface.

Programming Model and Register Set

The synthesizer contains two fully accessible configuration registers (PLL_L and PLL_H) and a write-only command register (CMD). Programming the synthesizer frequency through the I²C interface requires two steps: 1) writing a valid PLL configuration to the configuration registers and 2) loading the registers into the PLL by an I²C command. The PLL frequency is affected as a result of the second step.

MPC92432

This two-step procedure can be performed by a single I²C transaction or by multiple, independent I²C transactions. An alternative way to achieve small PLL frequency changes is to use the increment or decrement commands of the synthesizer, which have an immediate effect on the PLL frequency.

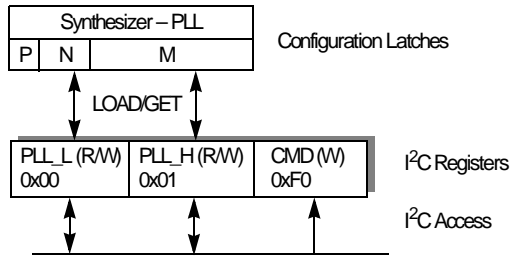


Figure 3. I²C Mode Register Set

Figure 3 illustrates the synthesizer register set. PLL_L and PLL_H store a PLL configuration and are fully accessible (Read/Write) by the I²C bus. CMD (Write only) accepts commands (LOAD, GET, INC, DEC) to update registers and for direct PLL frequency changes.

Set the synthesizer frequency:

- 1) Write the PLL_L and PLL_H registers with a new configuration (see **Table 14** and **Table 15** for register maps)
- 2) Write the LOAD command to update the PLL dividers by the current PLL_L, PLL_H content.

Read the synthesizer frequency:

- 1) Write the GET commands to update the PLL_L, PLL_H registers by the PLL divider setting
- 2) Read the PLL_L, PLL_H registers through I²C

Change the synthesizer frequency in small steps:

- 1) Write the INC or DEC command to change the PLL frequency immediately. Repeat at any time if desired.

LOAD and GET are inverse command to each other. LOAD updates the PLL dividers and GET updates the configuration registers. A fast and convenient way to change the PLL frequency is to use the INC (increment M) and DEC (decrement M) commands of the synthesizer. INC (DEC) directly increments (decrements) the PLL-feedback divider M and immediately changes the PLL frequency by the smallest step G (see **Table 7** for the frequency granularity G). The INC and DEC commands are designed for multiple and rapid PLL frequency changes as required in frequency margining applications. INC and DEC do not require the user to update the PLL dividers by the LOAD command, INC and DEC do not update the PLL_L and PLL_H registers either (use LOAD for an initial PLL divider setting and, if desired, use GET to read the PLL configuration). Note that the synthesizer does not check any boundary

conditions such as the VCO frequency range. Applying the INC and DEC commands could result in invalid VCO frequencies (VCO frequency beyond lock range).

Register Maps

Table 13. Configuration Registers

| Address | Name | Content | Access |
|---------|-------|---|--------|
| 0x00 | PLL_L | Least significant 8 bits of M | R/W |
| 0x01 | PLL_H | Most significant 2 bits of M, P, N _A , N _B , and lock state | R/W |
| 0xF0 | CMD | Command register (write only) | W only |

Register 0x00 (PLL_L) contains the least significant bits of the PLL feedback divider M.

Table 14. PLL_L (0x00, R/W) Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----|----|----|----|----|----|----|----|
| Name | M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 |

Register content:

M[7:0] PLL feedback-divider M, bits 7–0

Register 0x01 (PLL_H) contains the two most significant bits of the PLL feedback divider M, four bits to control the PLL post-dividers N and the PLL pre-divider P. The bit 0 in PLL_H register indicates the lock condition of the PLL and is set by the synthesizer automatically. The LOCK state is a copy of the PLL lock signal output (LOCK). A write-access to LOCK has no effect.

Table 15. PLL_H (0x01, R/W) Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|----|----|-----|-----|-----|----|---|------|
| Name | M9 | M8 | NA2 | NA1 | NA0 | NB | P | LOCK |

Register content:

M[9:8] PLL feedback-divider M, bits 9–8

NA[2:0] PLL post-divider N_A, see **Table 9**

NB PLL post-divider N_B, see **Table 10**

P PLL pre-divider P, see **Table 8**

LOCK Copy of LOCK output signal (read-only)

Note that the LOAD command is required to update the PLL dividers by the content of both PLL_L and PLL_H registers.

Register 0xF0 (CMD) is a write-only command register. The purpose of CMD is to provide a fast way to increase or decrease the PLL frequency and to update the registers. The register accepts four commands, INC (increment M), DEC (decrement M), LOAD and GET (update registers). It is

recommended to write the INC, DEC commands only after a valid PLL configuration is achieved. INC and DEC only affect the M-divider of the PLL (PLL feedback). Applying INC and DEC commands can result in a PLL configuration beyond the specified lock range and the PLL may lose lock. The MPC92432 does not verify the validity of any commands such as LOAD, INC, and DEC. The INC and DEC commands change the PLL feedback divider without updating PLL_L and PLL_H.

Table 16. CMD (0xF0): PLL Command (Write-Only)

| Command | Op-Code | Description |
|---------|---------------------|---|
| INC | xxxx0001b (0x01) | Increase internal PLL frequency M:=M+1 |
| DEC | xxxx0010b (0x02) | Decrease internal PLL frequency M:=M-1 |
| LOAD | xxxx0100b (0x04) | Update the PLL divider config. PLL divider M, N, P:=PLL_L, PLL_H |
| GET | xxxx1000b (0x08) | Update the configuration registers PLL_L, PLL_H:=PLL divider M, N, P |

I²C — Register Access in Parallel Mode

The MPC92432 supports the configuration of the synthesizer through the parallel interface (PLOAD = 0) and serial interface (PLOAD = 1). Register contents and the divider configurations are not changed when the user switches from parallel mode to serial mode. However, when switching from serial mode to parallel mode, the PLL dividers immediately reflect the logical state of the hardware pins M[9:0], NA[2:0], NB, and P.

Applications using the parallel interface to obtain a PLL configuration can use the serial interface to verify the divider settings. In parallel mode (PLOAD = 0), the MPC92432 allows read-access to PLL_L and PLL_H through I²C (if PLOAD = 0, the current PLL configuration is stored in PLL_L, PLL_H. The GET command is not necessary and also not supported in parallel mode). After changing from parallel to serial mode (PLOAD = 1), the last PLL configuration is still stored in PLL_L, PLL_H. The user now has full write and read access to both configuration registers through the I²C bus and can change the configuration at any time.

Table 19. Complete Configuration Register Write Transfer

| 1 bit | 7 bits | 1 bit | 1 bit | 8 bits | 1 bit | 8 bits | 1 bit | 8 bits | 1 bit | 8 bits | 1 bit | 1 bit |
|--------|----------------------|-------|-------|--------|-------|---------------|-------|--------|-------|---------------|-------|-------|
| Start | Slave address | R/W | ACK | &PLL_H | ACK | Config-Byte 1 | ACK | &PLL_L | ACK | Config-Byte 2 | ACK | Stop |
| | 10110xx ¹ | 0 | | 0x01 | | Data | | 0x00 | | Data | | |
| Master | Master | Mast | Slave | Master | Slave | Master | Slave | Master | Slave | Master | Slave | Mast |

1. xx = state of ADR1, ADR0 pins

Table 17. PLL Configuration in Parallel and Serial Modes

| PLL Configuration | Parallel | Serial (Registers PLL_L, PLL_H) |
|-------------------|--------------------|---------------------------------|
| M[9:0] | Set pins M9–M0 | M[9:0] (R/W) |
| NA[2:0] | Set pins NA2...NA0 | NA[2:0] (R/W) |
| NB | Set pin NB | NB (R/W) |
| P | Set bit P in PLL_H | P (R/W) |
| LOCK status | LOCK pin 26 | LOCK (Read only) |

Programming the I²C Interface

Table 18. I²C Slave Address

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|---|---|---|---|---|----------|----------|-----|
| Value | 1 | 0 | 1 | 1 | 0 | Pin ADR1 | Pin ADR0 | R/W |

The 7-bit I²C slave address of the MPC92432 synthesizer is a combination of a 5-bit fixed addresses and two variable bits which are set by the hardware pins ADR[1:0]. Bit 0 of the MPC92432 slave address is used by the bus controller to select either the read or write mode. '0' indicates a transmission (I²C-WRITE) to the MPC92432. '1' indicates a request for data (I²C-READ) from the synthesizer. The hardware pins ADR1 and ADR0 and should be individually set by the user to avoid address conflicts of multiple MPC92432 devices on the same I²C bus.

Write Mode (R/W = 0)

The configuration registers are written by the bus controller by the initiation of a write transfer with the MPC92432 slave address (first byte), followed by the address of the configuration register (second byte: 0x00, 0x01 or 0xF0), and the configuration data byte (third byte). This transfer may be followed by writing more registers by sending the configuration register address followed by one data byte. Each byte sent by the bus controller is acknowledged by the MPC92432. The transfer ends by a stop bit sent by the bus controller. The number of configuration data bytes and the write sequence are not restricted.

MPC92432

Read Mode (R/W = 1)

The configuration registers are read by the bus controller by the initiation of a read transfer. The MPC92432 supports read transfers immediately after the first byte without a change in the transfer direction. Immediately after the bus controller sends the slave address, the MPC92432 acknowledges and then sends both configuration register PLL_L and PLL_H (back-to-back) to the bus controller. The CMD register cannot be read. In order to read the two synthesizer registers and the current PLL configuration setting, the user can 1) read PLL_L, PLL_H, write

the GET command (loads the current configuration into PLL_L, PLL_H) and read PLL_L, PLL_H again. Note that the PLL_L, PLL_H registers and divider settings may not be equivalent after the following cases:

- a. Writing the INC command
- b. Writing the DEC command
- c. Writing PLL_L, PLL_H registers with a new configuration and not writing the LOAD command.

Table 20. Configuration Register Read Transfer

| | | | | | | | | |
|--------|----------------------|-------|-------|--------|-------|--------|--------|-------|
| 1 bit | 7 bits | 1 bit | 1 bit | 8 bits | 1 bit | 8 bits | 1 bit | 1 bit |
| Start | Slave address | R/W | ACK | PLL_L | ACK | PLL_H | ACK | Stop |
| | 10110xx ¹ | 1 | | Data | | Data | | |
| Master | Master | Mast | Slave | Slave | Mast | Slave | Master | Slave |

1. xx = state of ADR1, ADR0 pins

Device Startup

General Device Configuration

It is recommended to reset the MPC92432 during or immediately after the system powers up (MR = 0). The device acquires an initial PLL divider configuration through the parallel interface pins M[9:0], NA[2:0], N, and P¹ with the low-to-high transition of MR². PLL frequency lock is achieved within the specified lock time (t_{LOCK}) and is indicated by an assertion of the LOCK signal which completes the startup procedure. It is recommended to disable the outputs (CLK_STOPx = 0) until PLL lock is achieved to suppress output frequency transitions. The output frequency can be reconfigured at any time through either the parallel or the serial interface.

Note that a PLL configuration obtained by the parallel interface can be read through I²C independent on the current programming mode (parallel or serial). Refer to **I²C — Register Access in Parallel Mode** for additional information on how to read a PLL startup configuration through the I²C interface.

Starting-Up Using the Parallel Interface

The simplest way to use the MPC92432 is through the parallel interface. The serial interface pins (SDA, SDL, and ADDR[1:0]) can be left open and PLOAD is set to logic low. After the release of MR and at any other time the PLL/output frequency configuration is directly set to through the M[9:0], NA[2:0], NB, and P pins.

Start-Up Using the Serial (I²C) Interface

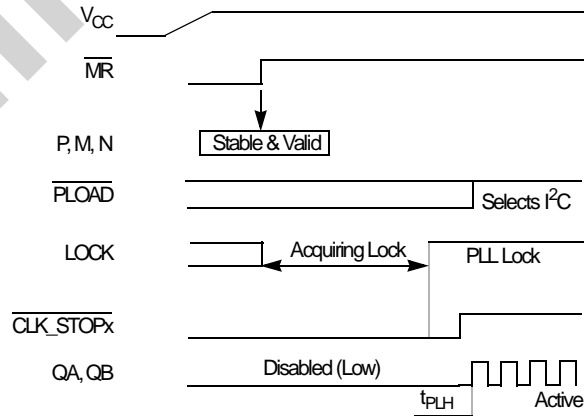


Figure 4. Start-Up Using I²C Interface

Set PLOAD = 1, CLK_STOPx = L and leave the parallel interface pins (M[9:0], NA[2:0], N, and P) open. The PLL dividers are configured by the default configuration at the low-to-high transition of MR. This initial PLL configuration can be re-programmed to the final VCO frequency at any time through the serial interface. After the PLL achieved lock at the desired VCO frequency, enable the outputs by setting CLK_STOPx = H. PLL lock and re-lock (after any configuration change through M or P) is indicated by LOCK being asserted.

1. The parallel interface pins M[9:0], NA[2:0], N, and P may be left open (floating). In this case the initial PLL configuration will have the default setting of M = 500, P = 1, NA[2:0] = 010, NB = 0, resulting in an internal VCO frequency of 2000 MHz (f_{ref} = 16 MHz) and an output frequency of 250 MHz.
 2. The initial PLL configuration is independent on the selected programming mode (PLOAD low or high)

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LOCK Detect

The LOCK detect circuitry indicates the frequency-lock status of the PLL by setting and resetting the pin LOCK and register bit LOCK simultaneously. The LOCK status is asserted after the PLL acquired frequency lock during the startup and is immediately deasserted when the PLL lost lock, for instance when the reference clock is removed. The PLL may also loose lock when the PLL feedback-divider M or pre-divider P is changed or the DEC/INC command is issued. The PLL may not loose lock as a result of slow reference frequency changes. In any case of loosing LOCK, the PLL attempts to re-lock to the reference frequency. LOCK and re-lock of the PLL is indicated by the LOCK signal after a delay of TBD cycles to prevent signaling temporary PLL locks during frequency transitions.

Output Clock Stop

Asserting $\overline{\text{CLK_STOPx}}$ will stop the respective output clock in logic low state. The $\overline{\text{CLK_STOPx}}$ control is internally synchronized to the output clock signal, therefore, enabling and disabling outputs does not produce runt pulses. See **Figure 5**. The clock stop controls of the QA and QB outputs are independent on each other. If the QB runs at half of the QA output frequency and both outputs are enabled at the same time, the first clock pulse of QA may not appear at the same time of the first QB output. (See **Figure 6**.) Coincident rising edges of QA and QB stay synchronous after the assertion and de-assertion of the $\overline{\text{CLK_STOPx}}$ controls. Asserting $\overline{\text{MR}}$ always resets the output divider to a logic low output state, with the risk of producing an output runt pulse.

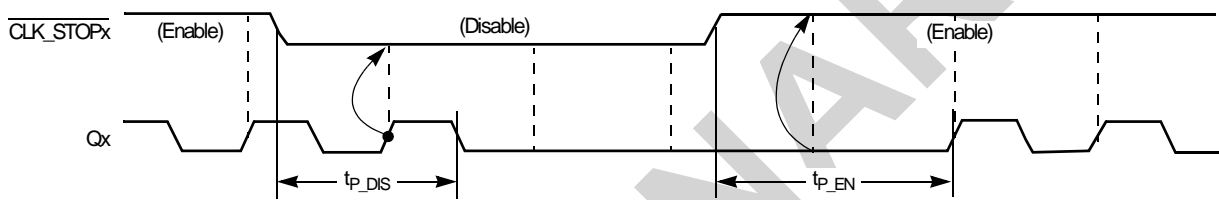


Figure 5. Clock Stop Timing for NB = 0 ($f_{QA} = f_{QB}$)

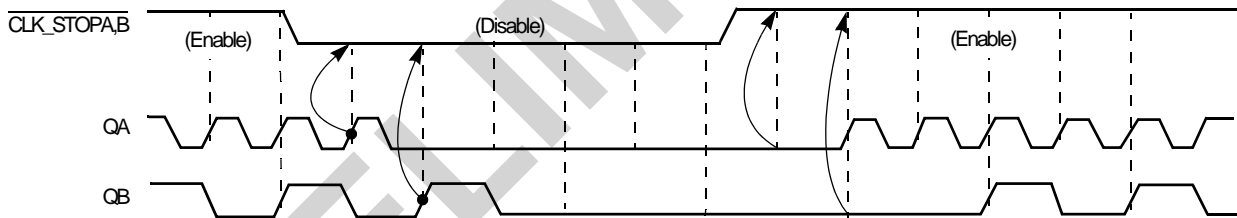


Figure 6. Clock Stop Timing for NB = 1 ($f_{QA} = 2 f_{QB}$)

MPC92432

Frequency Operating Range

Table 21. MPC92432 Frequency Operating Range for P = 2

| M | M[9:0] | f _{VCO} [MHz] (Parameter: f _{REF} in MHz) | | | | Output Frequency for f _{XTAL} = 16 MHz (Parameter N) | | | | | |
|-----|------------|---|------|------|------|---|-----|-----|-----|-------|-------|
| | | 15 | 16 | 18 | 20 | 2 | 4 | 8 | 16 | 32 | 64 |
| 170 | 0010101010 | | 1360 | 1530 | 1700 | 680 | 340 | 170 | 85 | 42.50 | 21.25 |
| 180 | 0010110100 | | 1440 | 1620 | 1800 | 720 | 360 | 180 | 90 | 45.00 | 22.50 |
| 190 | 0010111110 | 1425 | 1520 | 1710 | 1900 | 760 | 380 | 190 | 95 | 47.50 | 23.75 |
| 200 | 0011001000 | 1500 | 1600 | 1800 | 2000 | 800 | 400 | 200 | 100 | 50.00 | 25.00 |
| 210 | 0011010010 | 1575 | 1680 | 1890 | 2100 | 840 | 420 | 210 | 105 | 52.50 | 26.25 |
| 220 | 0011011100 | 1650 | 1760 | 1980 | 2200 | 880 | 440 | 220 | 110 | 55.00 | 27.50 |
| 230 | 0011100110 | 1725 | 1840 | 2070 | 2300 | 920 | 460 | 230 | 115 | 57.50 | 28.75 |
| 240 | 0011110000 | 1800 | 1920 | 2160 | 2400 | 960 | 480 | 240 | 120 | 60.00 | 30.00 |
| 250 | 0011111010 | 1875 | 2000 | 2250 | 2500 | 1000 | 500 | 250 | 125 | 62.50 | 31.25 |
| 260 | 0100000100 | 1950 | 2080 | 2340 | 2600 | 1040 | 520 | 260 | 130 | 65.00 | 32.50 |
| 270 | 0100001110 | 2025 | 2160 | 2430 | 2700 | 1080 | 540 | 270 | 135 | 67.50 | 33.75 |
| 280 | 0100011000 | 2100 | 2240 | 2520 | | 1120 | 560 | 280 | 140 | 70.00 | 35.00 |
| 290 | 0100100010 | 2175 | 2320 | 2610 | | 1160 | 580 | 290 | 145 | 72.50 | 36.25 |
| 300 | 0100101100 | 2250 | 2400 | 2700 | | 1200 | 600 | 300 | 150 | 75.00 | 37.50 |
| 310 | 0100110110 | 2325 | 2480 | | | 1240 | 620 | 310 | 155 | 77.50 | 38.75 |
| 320 | 0101000000 | 2400 | 2560 | | | 1280 | 640 | 320 | 160 | 80.00 | 40.00 |
| 330 | 0101001010 | 2475 | 2640 | | | 1320 | 660 | 330 | 165 | 82.50 | 41.25 |
| 340 | 0101010100 | 2550 | 2720 | | | 1360 | 680 | 340 | 170 | 85.00 | 42.50 |

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Table 22. MPC92432 Frequency Operating Range for P = 4

| M | M[9:0] | f _{VCO} [MHz] (Parameter: f _{REF} in MHz) | | | | Output Frequency for f _{X TAL} = 16 MHz (Parameter N) | | | | | |
|-----|------------|---|------|------|------|--|-----|-----|-------|--------|--------|
| | | 15 | 16 | 18 | 20 | 2 | 4 | 8 | 16 | 32 | 64 |
| 340 | 0101010100 | | 1360 | 1530 | 1700 | 680 | 340 | 170 | 85.0 | 42.50 | 21.25 |
| 350 | 0101011110 | | 1400 | 1575 | 1750 | 700 | 350 | 175 | 87.5 | 43.75 | 21.875 |
| 360 | 0101101000 | | 1440 | 1620 | 1800 | 720 | 360 | 180 | 90.0 | 45.00 | 22.50 |
| 370 | 0101110010 | 1387.5 | 1480 | 1665 | 1850 | 740 | 370 | 185 | 92.5 | 46.25 | 23.125 |
| 380 | 0101111100 | 1425.0 | 1520 | 1710 | 1900 | 760 | 380 | 190 | 95.0 | 47.50 | 23.75 |
| 390 | 0110000110 | 1462.5 | 1560 | 1755 | 1950 | 780 | 390 | 195 | 97.5 | 48.75 | 24.375 |
| 400 | 0110010000 | 1500.0 | 1600 | 1800 | 2000 | 800 | 400 | 200 | 100.0 | 50.00 | 25.00 |
| 410 | 0110110010 | 1537.5 | 1640 | 1845 | 2050 | 820 | 410 | 205 | 102.5 | 51.25 | 25.625 |
| 420 | 0110100100 | 1575.0 | 1680 | 1890 | 2100 | 840 | 420 | 210 | 105.0 | 52.50 | 26.25 |
| 430 | 0110101110 | 1612.5 | 1720 | 1935 | 2150 | 860 | 430 | 215 | 107.5 | 53.75 | 26.875 |
| 440 | 0110111000 | 1650.0 | 1760 | 1980 | 2200 | 880 | 440 | 220 | 110.0 | 55.00 | 27.50 |
| 450 | 0111000010 | 1687.5 | 1800 | 2025 | 2250 | 900 | 450 | 225 | 112.5 | 56.25 | 28.125 |
| 460 | 0111001100 | 1725.0 | 1840 | 2070 | 2300 | 920 | 460 | 230 | 115.0 | 57.50 | 28.75 |
| 470 | 0111010110 | 1762.5 | 1880 | 2115 | 2350 | 940 | 470 | 235 | 117.5 | 58.75 | 29.375 |
| 480 | 0111100000 | 1800.0 | 1920 | 2160 | 2400 | 960 | 480 | 240 | 120.0 | 60.00 | 30.00 |
| 490 | 0111101010 | 1837.5 | 1960 | 2205 | 2450 | 980 | 490 | 245 | 122.5 | 61.25 | 30.625 |
| 500 | 0111110100 | 1875.0 | 2000 | 2250 | 2500 | 1000 | 500 | 250 | 125.0 | 62.50 | 31.25 |
| 510 | 0111111110 | 1912.5 | 2040 | 2295 | 2550 | 1020 | 510 | 255 | 127.5 | 63.75 | 31.875 |
| 520 | 1000001000 | 1950.0 | 2080 | 2340 | 2600 | 1040 | 520 | 260 | 130.0 | 65.00 | 32.50 |
| 530 | 1000010010 | 1987.5 | 2120 | 2475 | 2650 | 1060 | 530 | 265 | 132.5 | 66.25 | 33.125 |
| 540 | 1000011100 | 2025.0 | 2160 | 2520 | 2700 | 1080 | 540 | 270 | 135.0 | 67.50 | 33.75 |
| 550 | 1000100110 | 2062.5 | 2200 | 2565 | | 1100 | 550 | 285 | 137.5 | 68.75 | 34.375 |
| 560 | 1000110000 | 2100.0 | 2240 | 2610 | | 1120 | 560 | 280 | 140.0 | 70.00 | 35.00 |
| 570 | 1000111010 | 2137.5 | 2280 | 2700 | | 1140 | 570 | 285 | 142.5 | 71.25 | 35.625 |
| 580 | 1001000100 | 2175.0 | 2320 | | | 1160 | 580 | 290 | 145.0 | 72.50 | 36.25 |
| 590 | 1001001110 | 2212.5 | 2360 | | | 1180 | 590 | 295 | 147.5 | 73.75 | 36.875 |
| 600 | 1001011000 | 2250.0 | 2400 | | | 1200 | 600 | 300 | 150.0 | 75.00 | 37.50 |
| 610 | 1001100010 | 2287.5 | 2440 | | | 1220 | 610 | 305 | 152.5 | 76.25 | 38.125 |
| 620 | 1001101100 | 2325.0 | 2480 | | | 1240 | 620 | 310 | 155.0 | 77.50 | 38.75 |
| 630 | 1001110110 | 2362.5 | 2520 | | | 1260 | 630 | 315 | 157.5 | 78.75^ | 39.375 |
| 640 | 1010000000 | 2400.0 | 2560 | | | 1280 | 640 | 320 | 160.0 | 80.00 | 40.00 |
| 650 | 1010001010 | 2437.5 | 2600 | | | 1300 | 650 | 325 | 162.5 | 81.25 | 40.625 |
| 660 | 0010010100 | 2475.0 | 2640 | | | 1320 | 660 | 330 | 165 | 82.5 | 41.25 |
| 670 | 1010011110 | 2512.5 | 2680 | | | 1340 | 670 | 335 | 167.5 | 83.75 | 41.875 |
| 680 | 1010101000 | 2550.0 | 2720 | | | 1360 | 680 | 340 | 170 | 85.00 | 42.50 |

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MPC92432

V_{CC_PLL} Filter

The MPC92432 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} pin impacts the device AC characteristics. The MPC92432 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In digital system environments where it is more difficult to minimize noise on the power supplies a second level of isolation is recommended: a power supply filter on the V_{CC_PLL} pin for the MPC92432.

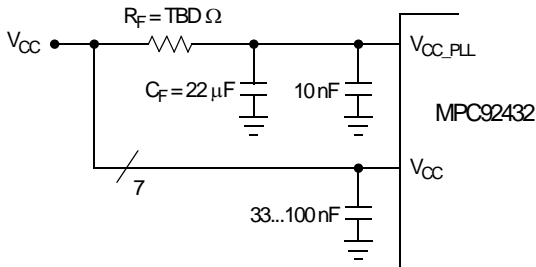


Figure 7. V_{CC_PLL} Power Supply Filter

Figure 7 illustrates a recommended power supply filter scheme.

The MPC9230 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CC_PLL} pin of the

MPC92432. From the data sheet, the V_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is maximum TBD mA, assuming that a minimum of TBD V must be maintained on the V_{CC_PLL} pin. The resistor shown in Figure 8 must have a resistance of TBD Ω to meet the voltage drop criteria. The minimum values for R_F and the filter capacitor C_F are defined by the filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above TBD kHz. In the recommended filter shown in Figure 7 the filter cut-off frequency is around 4.5 TBD and the noise attenuation at TBD KHz is better than TBD dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

AC Test Reference and Output Termination

The MPC92432 LVPECL outputs are designed to drive 50 transmission lines and require a DC termination to V_{TT} = V_{CC} - 2 V. Figure 8 illustrates the AC test reference for the MPC92432 as used in characterization and test of this circuit. If a separate termination voltage (V_{TT}) is not available, applications may use alternative output termination methods such as shown in Figure 9 and Figure 10.

The high-speed differential output signals of the MPC92432 are incompatible to single-ended LVCMOS signals. In order to use the synthesizer in LVCMOS clock signal environments, the dual-channel translator device MC100ES60T23 provides the necessary level conversion. The MC100ES60T23 has been specifically designed to interface with the MPC92432 and supports clock frequency up to 180 MHz

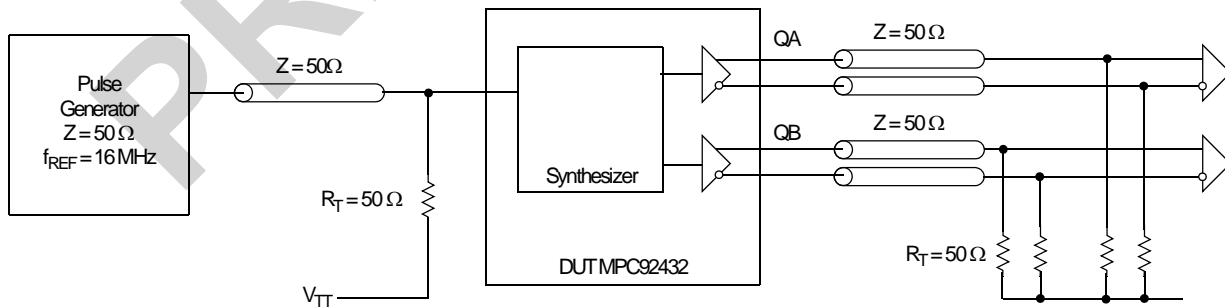


Figure 8. MPC92432 AC Test Reference

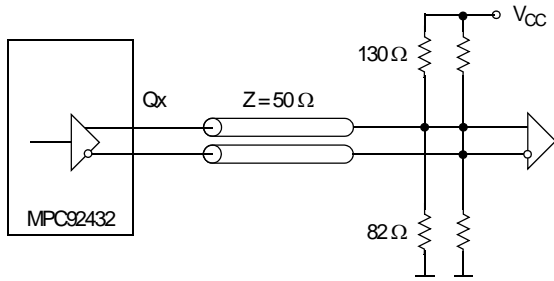


Figure 9. Thevenin Termination

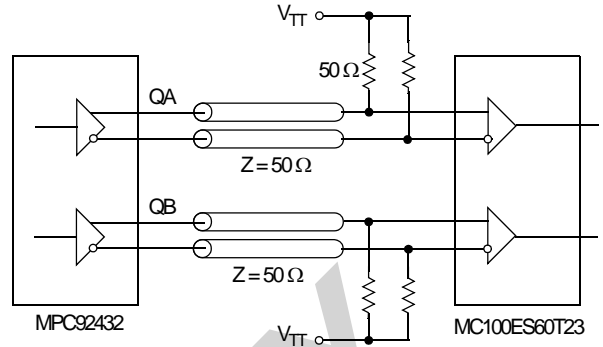


Figure 11. Interfacing with LVCMOS Logic for Frequency < 180 MHz

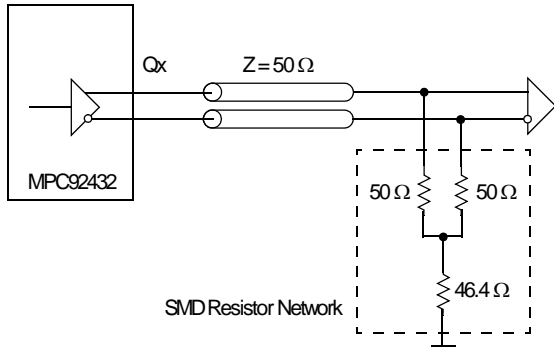


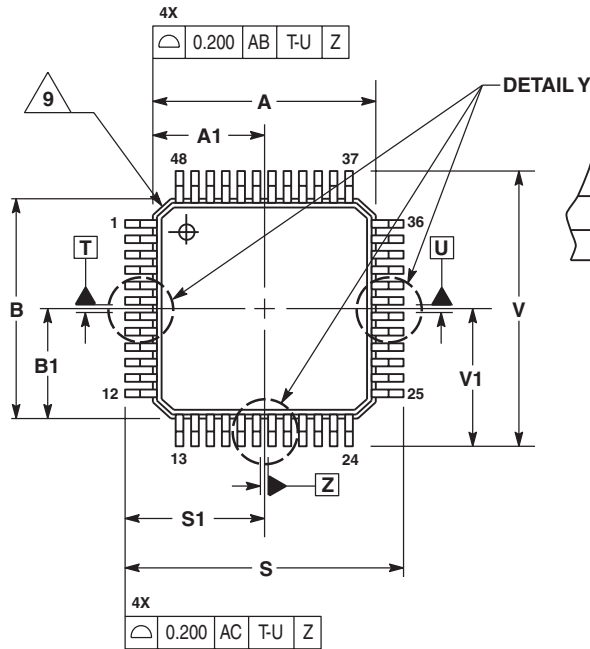
Figure 10. Resistor Network Termination

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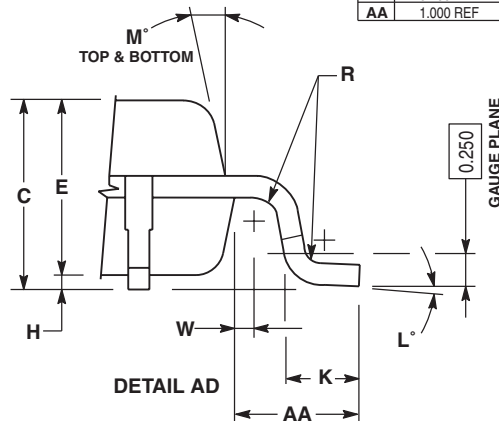
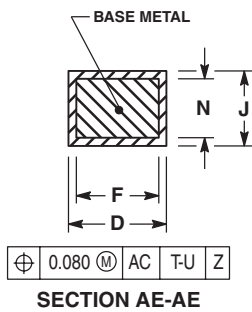
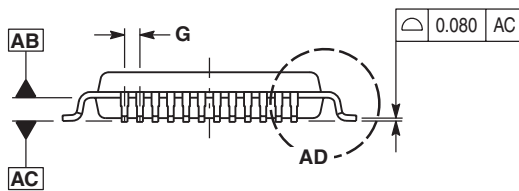
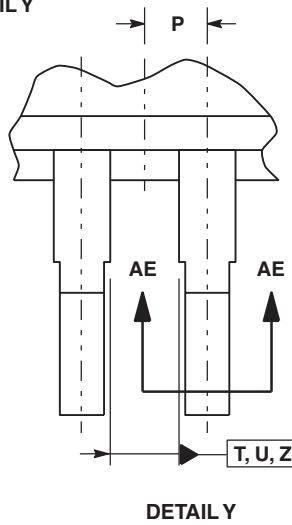
OUTLINE DIMENSIONS

FA SUFFIX 48-LEAD LQFP PACKAGE CASE 932-03 ISSUE F



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5m, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLAN AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.



| MILLIMETERS | | |
|-------------|-----------|-------|
| DIM | MIN | MAX |
| A | 7.000 BSC | |
| A1 | 3.500 BSC | |
| B | 7.000 BSC | |
| B1 | 3.500 BSC | |
| C | 1.400 | 1.600 |
| D | 0.170 | 0.270 |
| E | 1.350 | 1.450 |
| F | 0.170 | 0.230 |
| G | 0.500 BSC | |
| H | 0.050 | 0.150 |
| J | 0.090 | 0.200 |
| K | 0.500 | 0.700 |
| L | 0" | 7" |
| M | 12" REF | |
| N | 0.090 | 0.160 |
| P | 0.250 BSC | |
| R | 0.150 | 0.250 |
| S | 9.000 BSC | |
| S1 | 4.500 BSC | |
| V | 9.000 BSC | |
| V1 | 4.500 BSC | |
| W | 0.200 REF | |
| AA | 1.000 REF | |

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