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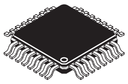
# Low Voltage PLL Clock Driver

# MPC9952

**LOW VOLTAGE**
**PLL CLOCK DRIVER**

The MPC9952 is a 3.3V compatible, PLL based clock driver device targeted for high performance clock tree applications. The device features a fully integrated PLL with no external components required. With output frequencies of up to 180MHz and eleven low skew outputs the MPC9952 is well suited for high performance designs. The device employs a fully differential PLL design to optimize jitter and noise rejection performance. Jitter is an increasingly important parameter as more microprocessors and ASiC's are employing on chip PLL clock distribution.

- Fully Integrated PLL
- Output Frequency up to 180MHz
- High Impedance Disabled Outputs
- Compatible with PowerPC™, Intel and High Performance RISC Microprocessors
- Output Frequency Configurable
- LQFP Packaging
- ±100ps Cycle–to–Cycle Jitter



**FA SUFFIX**
LQFP PACKAGE
CASE 873A-02

The MPC9952 features three banks of individually configurable outputs. The banks contain 5 outputs, 4 outputs and 2 outputs. The internal divide circuitry allows for output frequency ratios of 1:1, 2:1, 3:1 and 3:2:1. The output frequency relationship is controlled by the fsel frequency control pins. The fsel pins as well as the other inputs are LVCMOS/LVTTL compatible inputs.

The MPC9952 uses external feedback to the PLL. This features allows for the use of the device as a "zero delay" buffer. Any of the eleven outputs can be used as the feedback to the PLL. The VCO_Sel pin allows for the choice of two VCO ranges to optimize PLL stability and jitter performance. The MR/OE pin allows the user to force the outputs into high impedance for board level test.

For system debug the PLL of the MPC9952 can be bypassed. When forced to a logic HIGH, the PLLEN input will route the signal on the RefClk input around the PLL directly to the internal dividers. Because the signal is routed through the dividers, it may take several transitions of the RefClk to affect a transition on the outputs. This features allows a designer to single step the design for debug purposes.

The outputs of the MPC9952 are LVCMOS outputs. The outputs are optimally designed to drive terminated transmission lines. For applications using series terminated transmission lines each MPC9952 output can drive two lines. This capability provides an effective fanout of 22, more than enough clocks for most clock tree designs. For more information on driving transmission lines consult the applications section of this data sheet.

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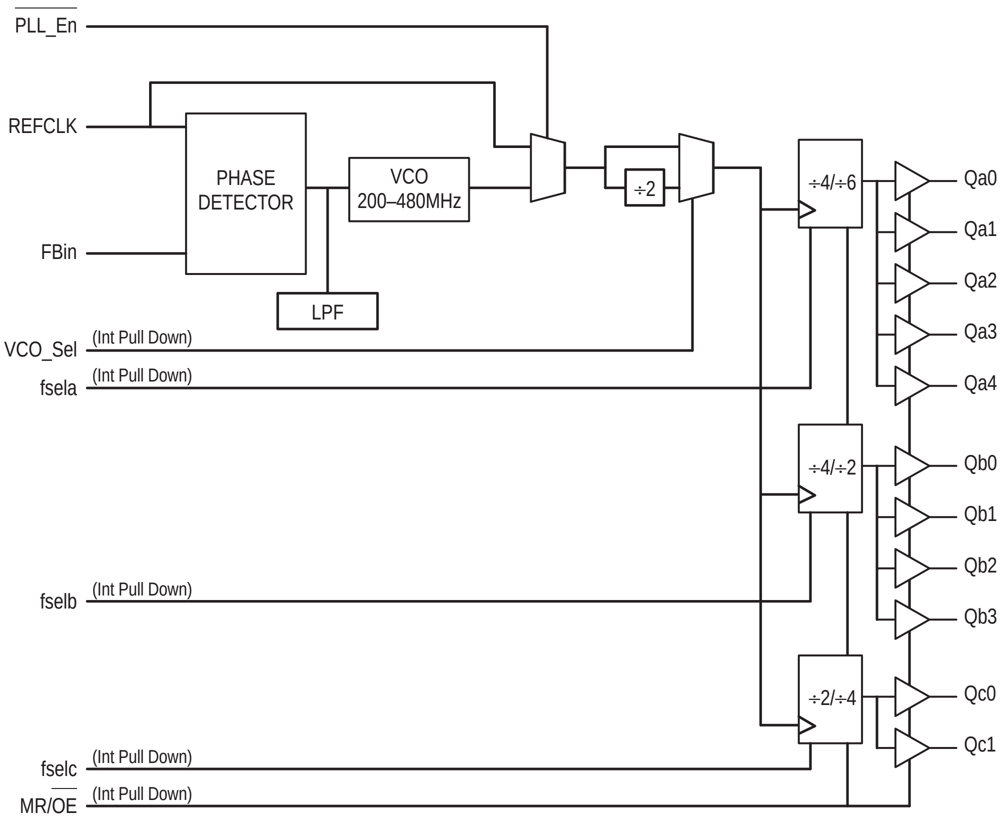
**Figure 1. MPC9952 Logic Diagram**



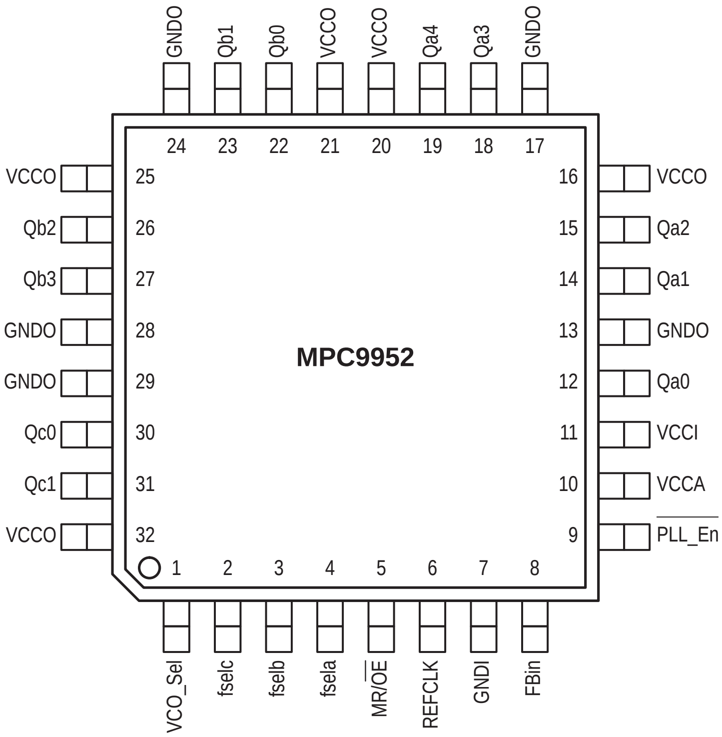


**Figure 2. 32–Lead Pinout** (Top View)

## FUNCTION TABLES

| fsela | Qan | fselb | Qbn | fselc | Qcn |
|---|---|---|---|---|---|
| 0 | ÷4 | 0 | ÷4 | 0 | ÷2 |
| 1 | ÷6 | 1 | ÷2 | 1 | ÷4 |

| Control Pin | Logic ‘0’ | Logic ‘1’ |
|---|---|---|
| VCO_Sel | fVCO | fVCO/2 |
| MR/OE | Output Enable | High Z |
| PLL_En | Enable PLL | Disable PLL |

| Pin Name | Description |
|---|---|
| VCCA | PLL Power Supply |
| VCCO | Output Buffer Power Supply |
| VCCI | Internal Core Logic Power Supply |
| GNDI | Internal Ground |
| GNDO | Output Buffer Ground |

## ABSOLUTE MAXIMUM RATINGS*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 4.6 | V |
| $V_I$ | Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V |
| $I_{IN}$ | Input Current | | ±20 | mA |
| $T_{Stor}$ | Storage Temperature Range | –40 | 125 | °C |

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

## THERMAL CHARACTERISTICS

Proper thermal management is critical for reliable system operation. This is especially true for high fanout and high drive capability products. Generic thermal information is available for the Motorola Clock Driver products. The means of calculating die power, the corresponding die temperature and the relationship to longterm reliability is addressed in the Motorola application note AN1545.

## DC CHARACTERISTICS ($T_A$ = 0° to 70°C, $V_{CCO} = V_{CCI} = V_{CCA}$ = 3.3V ± 5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | 3.6 | V | |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | |
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | | V | $I_{OH}$ = –20mA (Note 1.) |
| $V_{OL}$ | Output LOW Voltage | | | 0.5 | V | $I_{OL}$ = 20mA (Note 1.) |
| $I_{IN}$ | Input Current | | | ±120 | μA | Note 2. |
| $C_{IN}$ | Input Capacitance | | 2.7 | 4.0 | pF | |
| $C_{pd}$ | Power Dissipation Capacitance | | 25 | | pF | |
| $I_{CC}$ | Maximum Quiescent Supply Current | | | 160 | mA | Total ICC Static Current |
| $I_{CCA}$ | PLL Supply Current | | 15 | 20 | mA | |

1. The MPC9952 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CCO}/2$) transmission lines on the incident edge (see Applications Info section).
2. Inputs have pull–up, pull–down resistors which affect input current.

## PLL INPUT REFERENCE CHARACTERISTICS ($T_A$ = 0 to 70°C)

| Symbol | Characteristic | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $t_r$, $t_f$ | TCLK Input Rise/Falls | | 3.0 | ns | |
| $f_{ref}$ | Reference Input Frequency | | 100 | MHz | Note 3. |
| $f_{refDC}$ | Reference Input Duty Cycle | 25 | 75 | % | |

3. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider.

**AC CHARACTERISTICS** ($T_A$ = 0° to 70°C, $V_{CC}$ = 3.3V ±5%)

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $t_r$, $t_f$ | Output Rise/Fall Time (Note 4.) | 0.10 | | 1.0 | ns | 0.8 to 2.0V |
| $t_{pw}$ | Output Pulse Width (Note 4.) | $t_{CYCLE}/2$ –750 | $t_{CYCLE}/2$ ±500 | $t_{CYCLE}/2$ +750 | ps | |
| $t_{os}$ | Output-to-Output Skew (Note 4.) Excluding Qa0<br>All Outputs<br>All Outputs | | | 350<br>450<br>550 | ps | Same Frequencies<br>Same Frequencies<br>Different Frequencies |
| $f_{VCO}$ | PLL VCO Lock Range | 200 | | 480 | MHz | Note 6. |
| $f_{max}$ | Maximum Output Frequency Qc,Qb (÷2)<br>Qa,Qb,Qc (÷4)<br>Qa (÷6) | 180<br>120<br>80 | | | MHz | Note 4. |
| $t_{pd}$ | REFCLK to FBIN Delay | –200 | 0 | 200 | ps | Notes 4., 5. |
| $t_{PLZ}$, $t_{PHZ}$ | Output Disable Time | 2 | | 8 | ns | Note 4. |
| $t_{PZL}$, $t_{PLH}$ | Output Enable Time | 2 | | 10 | ns | Note 4. |
| $t_{jit(cc)}$ | Cycle–to–Cycle Jitter | | ±100 | | ps | |
| $t_{lock}$ | Maximum PLL Lock Time | | | 10 | ms | |

4. Termination of 50Ω to $V_{CCO}/2$.
5. $t_{pd}$ is specified for 50MHz input ref, the window will shrink/grow proportionally from the minimum limit with shorter/longer input reference periods. The $t_{pd}$ does not include jitter.
6. The PLL may be unstable with a divide by 2 feedback ratio.

## APPLICATIONS INFORMATION

### Driving Transmission Lines

The MPC9952 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 7Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091.

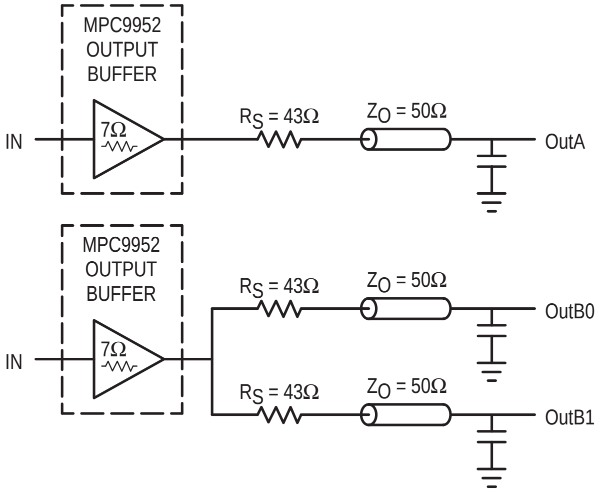


**Figure 3. Single versus Dual Transmission Lines**

In most high performance clock networks point–to–point distribution of signals is the method of choice. In a point–to–point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CCO}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9952 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9952 clock driver is effectively doubled due to its capability to drive multiple lines.

The waveform plots of Figure 4 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC9952 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output–to–output skew of the MPC9952. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$VL = VS (Zo / Rs + Ro + Zo) = 3.0 (25/53.5) = 1.40V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

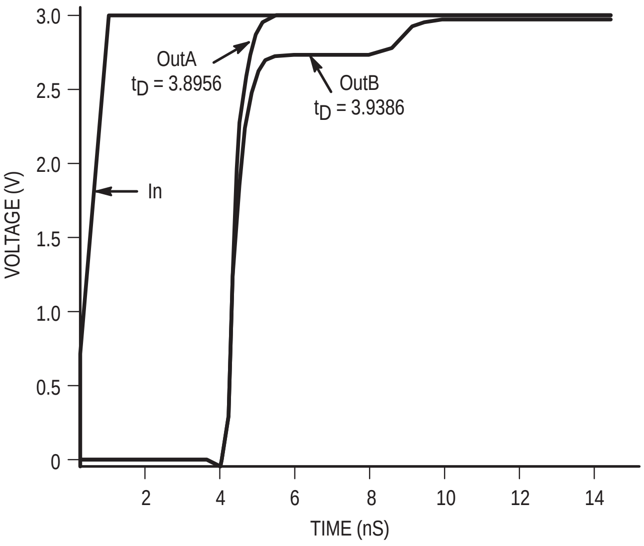
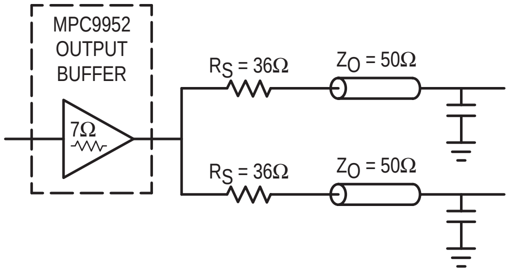


**Figure 4. Single versus Dual Waveforms**

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$$7\Omega + 36\Omega \parallel 36\Omega = 50\Omega \parallel 50\Omega$$
$$25\Omega = 25\Omega$$

**Figure 5. Optimized Dual Line Termination**

### Power Supply Filtering

The MPC9952 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC9952 provides separate power supplies for the output buffers ($V_{CCO}$) and the internal PLL (VCCA) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase–locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the VCCA pin for the MPC9952.

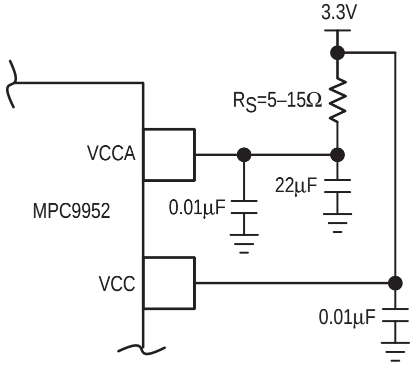


**Figure 6. Power Supply Filter**

Figure 6 illustrates a typical power supply filter scheme. The MPC9952 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the $V_{CC}$ supply and the VCCA pin of the MPC9952. From the data sheet the $I_{VCCA}$ current (the current sourced through the VCCA pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.3V – 5% must be maintained on the VCCA pin very little DC voltage drop can be tolerated when a 3.3V $V_{CC}$ supply is used. The resistor shown in Figure 6 must have a resistance of 5–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

Although the MPC9952 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

## OUTLINE DIMENSIONS

### FA SUFFIX
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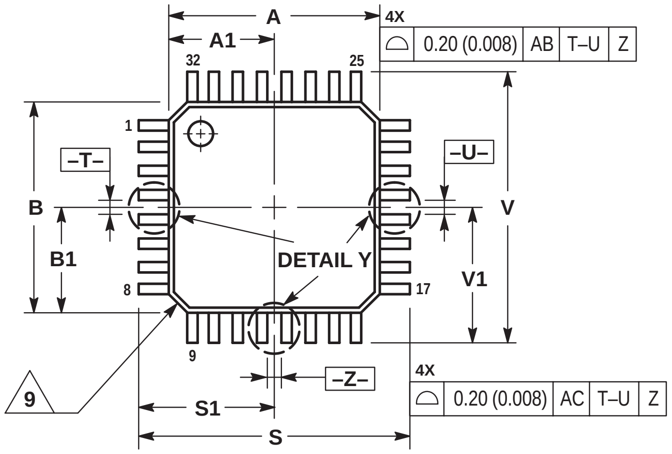
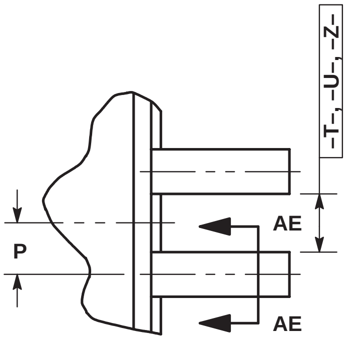
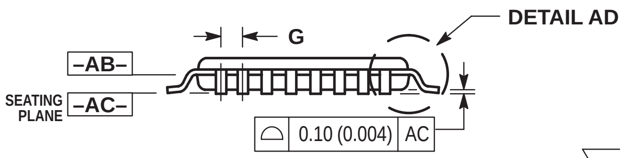
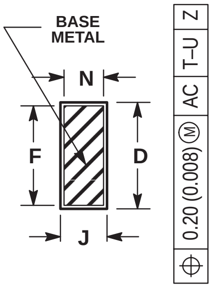
ISSUE A



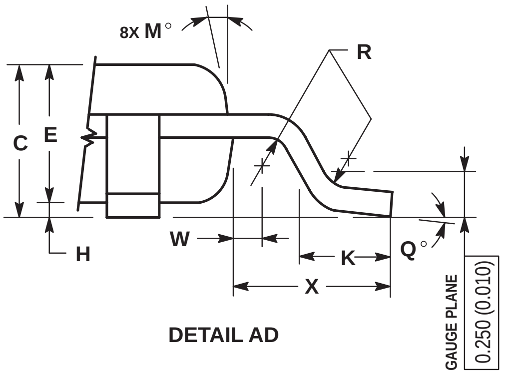


DETAIL Y





SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 7.000 BSC | | 0.276 BSC | |
| A1 | 3.500 BSC | | 0.138 BSC | |
| B | 7.000 BSC | | 0.276 BSC | |
| B1 | 3.500 BSC | | 0.138 BSC | |
| C | 1.400 | 1.600 | 0.055 | 0.063 |
| D | 0.300 | 0.450 | 0.012 | 0.018 |
| E | 1.350 | 1.450 | 0.053 | 0.057 |
| F | 0.300 | 0.400 | 0.012 | 0.016 |
| G | 0.800 BSC | | 0.031 BSC | |
| H | 0.050 | 0.150 | 0.002 | 0.006 |
| J | 0.090 | 0.200 | 0.004 | 0.008 |
| K | 0.500 | 0.700 | 0.020 | 0.028 |
| M | 12° REF | | 12° REF | |
| N | 0.090 | 0.160 | 0.004 | 0.006 |
| P | 0.400 BSC | | 0.016 BSC | |
| Q | 1° | 5° | 1° | 5° |
| R | 0.150 | 0.250 | 0.006 | 0.010 |
| S | 9.000 BSC | | 0.354 BSC | |
| S1 | 4.500 BSC | | 0.177 BSC | |
| V | 9.000 BSC | | 0.354 BSC | |
| V1 | 4.500 BSC | | 0.177 BSC | |
| W | 0.200 REF | | 0.008 REF | |
| X | 1.000 REF | | 0.039 REF | |

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