DATA SHEET

3.3V 1:12 LVCMOS PLL Clock Generator

MPC97H73

The MPC97H73 is a 3.3V compatible, 1:12 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance networking, computing and telecom applications. With output frequencies up to 240 MHz and output skews less than 250 ps the device meets the needs of the most demanding clock applications.

3.3V 1:12 LVCMOS PLL CLOCK GENERATOR

FA SUFFIX
52 LEAD LQFP PACKAGE
CASE 848D

Features

- 1:12 PLL based low-voltage clock generator
- 3.3V power supply
- Internal power–on reset
- Generates clock signals up to 240 MHz
- Maximum output skew of 250 ps
- Differential PECL reference clock input
- Two LVCMOS PLL reference clock inputs
- External PLL feedback supports zero-delay capability
- Various feedback and output dividers (see application section)
- Supports up to three individual generated output clock frequencies
- Synchronous output clock stop circuitry for each individual output for power down support
- Drives up to 24 clock lines
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MPC973

Functional Description

The MPC97H73 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC97H73 requires the connection of the PLL feedback output QFB to feedback input FB_IN to close the PLL feedback path. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. The MPC97H73 features an extensive level of frequency programmability between the 12 outputs as well as the output to input relationships, for instance 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 5:1, 5:2, 5:3, 5:4, 5:6, 6:1, 8:1 and 8:3.

The QSYNC output will indicate when the coincident rising edges of the above relationships will occur. The selectability of the feedback frequency is independent of the output frequencies. This allows for very flexible programming of the input reference versus output frequency relationship. The output frequencies can be either odd or even multiples of the input reference. In addition the output frequency can be less than the input frequency for applications where a frequency needs to be reduced by a non–binary factor. The MPC97H73 also supports the 180° phase shift of one of its output banks with respect to the other output banks. The QSYNC outputs reflects the phase relationship between the QA and QC outputs and can be used for the generation of system baseline timing signals.

The REF_SEL pin selects the LVPECL or the LVCMOS compatible inputs as the reference clock signal. Two alternative LVCMOS compatible clock inputs are provided for clock redundancy support. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The outputs can be individually disabled (stopped in logic low state) by programming the serial CLOCK_STOP interface of the MPC97H73. The MPC97H73 has an internal power–on reset.

The MPC97H73 is fully 3.3V compatible and requires no external loop filter components. All inputs (except PCLK) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC97H73 outputs can drive one or two traces giving the devices an effective fanout of 1:24. The device is pin and function compatible to the MPC973 and is packaged in a 52-lead LQFP package.

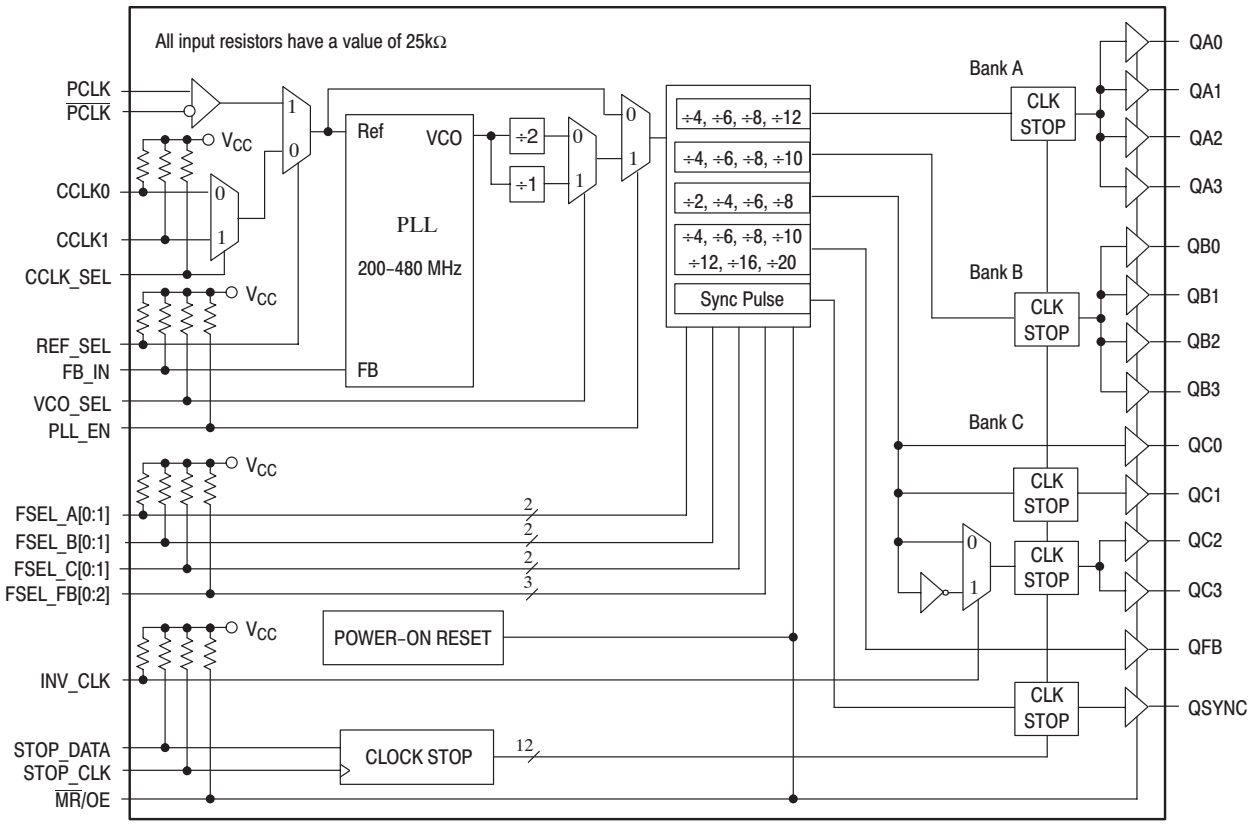


Figure 1. MPC97H73 Logic Diagram

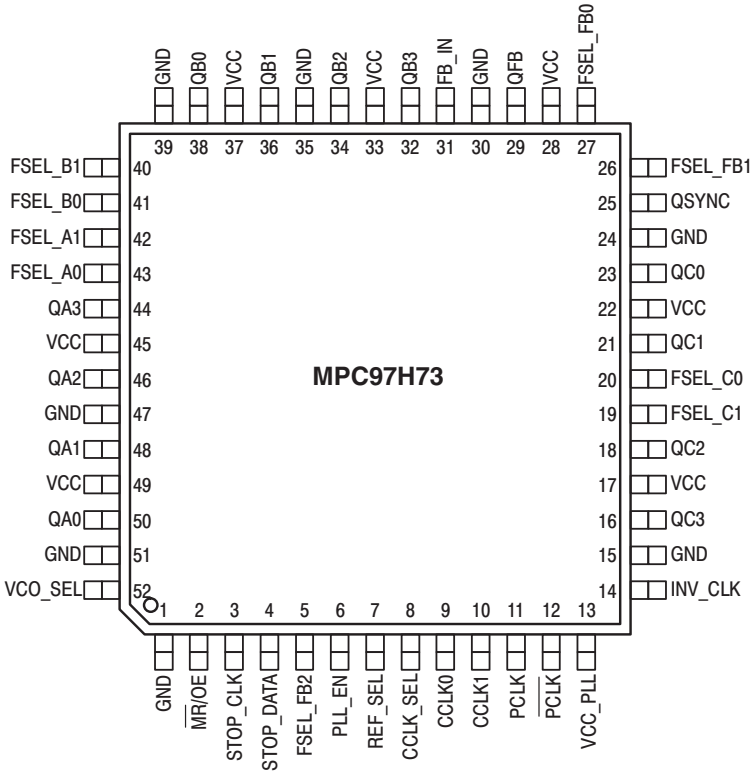


Figure 2. MPC97H73 52–Lead Package Pinout (Top View)

Table 1. PIN CONFIGURATION

Pin	I/O	Type	Function
CCLK0	Input	LVCMOS	PLL reference clock
CCLK1	Input	LVCMOS	Alternative PLL reference clock
PCLK, $\overline{\text{PCLK}}$	Input	LVPECL	Differential LVPECL reference clock
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to an QFB
CCLK_SEL	Input	LVCMOS	LVCMOS clock reference select
REF_SEL	Input	LVCMOS	LVCMOS/PECL reference clock select
VCO_SEL	Input	LVCMOS	VCO operating frequency select
PLL_EN	Input	LVCMOS	PLL enable/PLL bypass mode select
$\overline{\text{MR}}$/OE	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
FSEL_A[0:1]	Input	LVCMOS	Frequency divider select for bank A outputs
FSEL_B[0:1]	Input	LVCMOS	Frequency divider select for bank B outputs
FSEL_C[0:1]	Input	LVCMOS	Frequency divider select for bank C outputs
FSEL_FB[0:2]	Input	LVCMOS	Frequency divider select for the QFB output
INV_CLK	Input	LVCMOS	Clock phase selection for outputs QC2 and QC3
STOP_CLK	Input	LVCMOS	Clock input for clock stop circuitry
STOP_DATA	Input	LVCMOS	Configuration data input for clock stop circuitry
QA[0-3]	Output	LVCMOS	Clock outputs (Bank A)
QB[0-3]	Output	LVCMOS	Clock outputs (Bank B)
QC[0-3]	Output	LVCMOS	Clock outputs (Bank C)
QFB	Output	LVCMOS	PLL feedback output. Connect to FB_IN.
QSYNC	Output	LVCMOS	Synchronization pulse output
GND	Supply	Ground	Negative power supply
VCC_PLL	Supply	VCC	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}. Please see applications section for details.
VCC	Supply	VCC	Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation

Table 2. FUNCTION TABLE (Configuration Controls)

Control	Default	0	1
REF_SEL	1	Selects CCLKx as the PLL reference clock	Selects the LVPECL inputs as the PLL reference clock
CCLK_SEL	1	Selects CCLK0	Selects CCLK1
VCO_SEL	1	Selects VCO÷2. The VCO frequency is scaled by a factor of 2 (low VCO frequency range).	Selects VCO÷1. (high VCO frequency range)
PLL_EN	1	Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC97H73 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Normal operation mode with PLL enabled.
INV_CLK	1	QC2 and QC3 are in phase with QC0 and QC1	QC2 and QC3 are inverted (180° phase shift) with respect to QC0 and QC1
$\overline{\text{MR}}$/OE	1	Outputs disabled (high-impedance state) and device is reset. During reset/output disable the PLL feedback loop is open and the internal VCO is tied to its lowest frequency. The MPC97H73 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLKx). The device is reset by the internal power–on reset (POR) circuitry during power–up.	Outputs enabled (active)
VCO_SEL, FSEL_A[0:1], FSEL_B[0:1], FSEL_C[0:1], FSEL_FB[0:2] control the operating PLL frequency range and input/output frequency ratios. See Table 3 to Table 6 and the applications section for supported frequency ranges and output to input frequency ratios.			

Table 3. Output Divider Bank A (N_A)

VCO_SEL	FSEL_A1	FSEL_A0	QA[0:3]
0	0	0	VCO÷8
0	0	1	VCO÷12
0	1	0	VCO÷16
0	1	1	VCO÷24
1	0	0	VCO÷4
1	0	1	VCO÷6
1	1	0	VCO÷8
1	1	1	VCO÷12

Table 4. Output Divider Bank B (N_B)

VCO_SEL	FSEL_B1	FSEL_B0	QB[0:3]
0	0	0	VCO÷8
0	0	1	VCO÷12
0	1	0	VCO÷16
0	1	1	VCO÷20
1	0	0	VCO÷4
1	0	1	VCO÷6
1	1	0	VCO÷8
1	1	1	VCO÷10

Table 5. Output Divider Bank C (N_C)

VCO_SEL	FSEL_C1	FSEL_C0	QC[0:3]
0	0	0	VCO÷4
0	0	1	VCO÷8
0	1	0	VCO÷12
0	1	1	VCO÷16
1	0	0	VCO÷2
1	0	1	VCO÷4
1	1	0	VCO÷6
1	1	1	VCO÷8

Table 6. Output Divider PLL Feedback (M)

VCO_SEL	FSEL_FB2	FSEL_FB1	FSEL_FB0	QFB
0	0	0	0	VCO÷8
0	0	0	1	VCO÷12
0	0	1	0	VCO÷16
0	0	1	1	VCO÷20
0	1	0	0	VCO÷16
0	1	0	1	VCO÷24
0	1	1	0	VCO÷32
0	1	1	1	VCO÷40
1	0	0	0	VCO÷4
1	0	0	1	VCO÷6
1	0	1	0	VCO÷8
1	0	1	1	VCO÷10
1	1	0	0	VCO÷8
1	1	0	1	VCO÷12
1	1	1	0	VCO÷16
1	1	1	1	VCO÷20

Table 7. GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch–Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		12		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 8. ABSOLUTE MAXIMUM RATINGS[a]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.9	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 9. DC CHARACTERISTICS (V_{CC} = 3.3V ± 5%, T_A = 0°C to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{CC_PLL}	PLL Supply Voltage	3.0		V_{CC}	V	LVCMOS
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{PP}	Peak–to–peak Input Voltage PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}[a]	Common Mode Range PCLK, $\overline{PCLK}$	1.0		V_{CC} – 0.6	V	LVPECL
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-24 mA[b]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL}= 24 mA I_{OL}= 12 mA
Z_{OUT}	Output Impedance		8 - 11		Ω	
I_{IN}	Input Current[c]			±200	µA	V_{IN} = V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current		8.0	13.5	mA	V_{CC_PLL} Pin
I_{CCQ}	Maximum Quiescent Supply Current			35	mA	All V_{CC} Pins

a. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
b. The MPC97H73 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
c. Inputs have pull–down resistors affecting the input current.

Table 10. AC CHARACTERISTICS (V_{CC} = 3.3V ± 5%, T_A = 0°C to 70°C)[a b]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{REF}	Input reference frequency	÷4 feedback	50.0		120.0	MHz	PLL locked
		÷6 feedback	33.3		80.0	MHz	
		÷8 feedback	25.0		60.0	MHz	
		÷10 feedback	20.0		48.0	MHz	
		÷12 feedback	16.6		40.0	MHz	
		÷16 feedback	12.5		30.0	MHz	
		÷20 feedback	10.0		24.0	MHz	
		÷24 feedback	8.33		20.0	MHz	
		÷32 feedback	6.25		15.0	MHz	
		÷40 feedback	5.00		12.0	MHz	
	Input reference frequency in PLL bypass mode				250	MHz	PLL bypass
f_{VCO}	VCO frequency range[c]		200		480	MHz	
f_{MAX}	Output Frequency	÷2 output	100.0		240.0	MHz	PLL locked
		÷4 output	50.0		120.0	MHz	
		÷6 output	33.3		80.0	MHz	
		÷8 output	25.0		60.0	MHz	
		÷10 output	20.0		48.0	MHz	
		÷12 output	16.6		40.0	MHz	
		÷16 output	12.5		30.0	MHz	
		÷20 output	10.0		24.0	MHz	
		÷24 output	8.33		20.0	MHz	
f_{STOP_CLK}	Serial interface clock frequency				20	MHz	
V_{PP}	Peak-to-peak input voltage	PCLK, $\overline{PCLK}$	400		1000	mV	LVPECL
V_{CMR}[d]	Common Mode Range	PCLK, $\overline{PCLK}$	1.2		V_{CC}-0.9	V	LVPECL
$t_{PW,MIN}$	Input Reference Pulse Width[d]		2.0			ns	
t_R, t_F	CCLKx Input Rise/Fall Time[e]				1.0	ns	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay (static phase offset)[f]						PLL locked
	6.25 MHz < f_{REF} < 65.0 MHz		-3		+3	°	
	65.0 MHz < f_{REF} < 125 MHz		-4		+4	°	
	f_{REF}=50 MHz and feedback=÷8		-166		+166	ps	
$t_{SK(O)}$	Output-to-output Skew[g]	within QA outputs			100	ps	
		within QB outputs			100	ps	
		within QC outputs			100	ps	
		all outputs			250	ps	
DC	Output Duty Cycle[h]		(T÷2) - 200	T÷2	(T÷2) +200	ps	
t_R, t_F	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time				8.0	ns	
$t_{PZL, LZ}$	Output Enable Time				8.0	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter[i]			150	200	ps	
$t_{JIT(PER)}$	Period Jitter[j]				150	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter RMS (1 σ)[k]	÷4 feedback			11	ps	(VCO=400 MHz)
		÷6 feedback			86	ps	
		÷8 feedback			13	ps	
		÷10 feedback			88	ps	
		÷12 feedback			16	ps	
		÷16 feedback			19	ps	
		÷20 feedback			21	ps	
		÷24 feedback			22	ps	
		÷32 feedback			27	ps	
		÷40 feedback			30	ps	

Table 10. AC CHARACTERISTICS (V_{CC} = 3.3V ± 5%, T_A = 0°C to 70°C)[a b]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
BW	PLL closed loop bandwidth[l]	÷4 feedback		1.20 - 3.50		MHz	
		÷6 feedback		0.70 - 2.50		MHz	
		÷8 feedback		0.50 - 1.80		MHz	
		÷10 feedback		0.45 - 1.20		MHz	
		÷12 feedback		0.30 - 1.00		MHz	
		÷16 feedback		0.25 - 0.70		MHz	
		÷20 feedback		0.20 - 0.55		MHz	
		÷24 feedback		0.17 - 0.40		MHz	
		÷32 feedback		0.12 - 0.30		MHz	
		÷40 feedback		0.11 - 0.28		MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

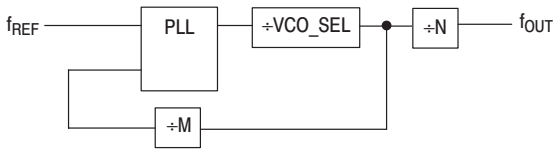
a AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
b The input reference frequency must match the VCO lock range divided by the feedback divider ratio: $f_{REF} = f_{VCO} \div (M \cdot VCO\_SEL)$.
c V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\varnothing)}$.
d Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% - DC_{REF,\ MIN}$.
e The MPC97H73 will operate with input rise/fall times up to 3.0 ns, but the A.C. characteristics, specifically $t_{(\varnothing)}$, $t_{PW,MIN}$, DC and f_{MAX} can only be guaranteed if t_R, t_F are within the specified range.
f CCLKx or PCLK to FB_IN. Static phase offset depends on the reference frequency. $t_{(\varnothing)}$ [s] = $t_{(\varnothing)}$ [°] ÷ ($f_{REF} \cdot 360°$).
g Excluding QSYNC output. See application section for part-to-part skew calculation.
h Output duty cycle is DC = (0.5 ± 200 ps · f_{OUT}) . 100%. E.g. the DC range at f_{OUT}=100MHz is 48%<DC<52%. T = output period.
i Cycle jitter is valid for all outputs in the same divider configuration. See application section for more details.
j Period jitter is valid for all outputs in the same divider configuration. See application section for more details.
k I/O jitter is valid for a VCO frequency of 400 MHz. See application section for I/O jitter vs. VCO frequency.
l -3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

MPC97H73 Configurations

Configuring the MPC97H73 amounts to properly configuring the internal dividers to produce the desired output frequencies. The output frequency can be represented by this formula:

$$f_{OUT} = f_{REF} \cdot M \div N$$



where f_{REF} is the reference frequency of the selected input clock source (CCLKO, CCLK1 or PCLK), M is the PLL feedback divider and N is a output divider. The PLL feedback divider is configured by the FSEL_FB[2:0] and the output dividers are individually configured for each output bank by the FSEL_A[1:0], FSEL_B[1:0] and FSEL_C[1:0] inputs.

The reference frequency f_{REF} and the selection of the feedback-divider M is limited by the specified VCO frequency range. f_{REF} and M must be configured to match the VCO frequency range of 200 to 480 MHz in order to achieve stable PLL operation:

$$f_{VCO,MIN} \leq (f_{REF} \cdot VCO\_SEL \cdot M) \leq f_{VCO,MAX}$$

The PLL post-divider VCO_SEL is either a divide-by-one or a divide-by-two and can be used to situate the VCO into the specified frequency range. This divider is controlled by the VCO_SEL pin. VCO_SEL effectively extends the usable input frequency range while it has no effect on the output to reference frequency ratio.

The output frequency for each bank can be derived from the VCO frequency and output divider:

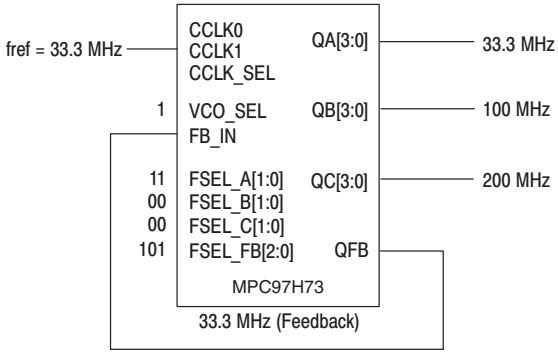
$$f_{QA[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_A)$$
$$f_{QB[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_B)$$
$$f_{QC[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_C)$$

Table 11. MPC97H73 Divider

Divider	Function	VCO_SEL	Values
M	PLL feedback FSEL_FB[0:3]	÷1	4, 6, 8, 10, 12, 16
		÷2	8, 12, 16, 20, 24, 32, 40
N_A	Bank A Output Divider FSEL_A[0:1]	÷1	4, 6, 8, 12
		÷2	8, 12, 16, 24
N_B	Bank B Output Divider FSEL_B[0:1]	÷1	4, 6, 8, 10
		÷2	8, 12, 16, 20
N_C	Bank C Output Divider FSEL_C[0:1]	÷1	2, 4, 6, 8
		÷2	4, 8, 12, 16

Table 11 shows the various PLL feedback and output dividers and Figure 3. and Figure 4. display example configurations for the MPC97H73:

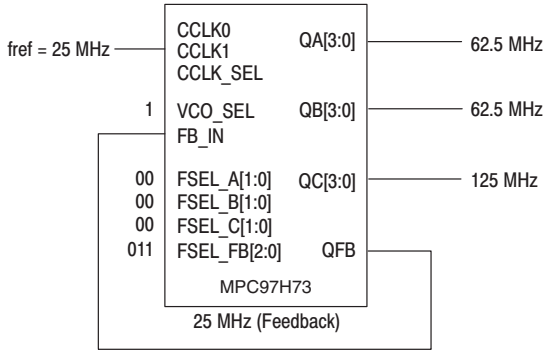
Figure 3. Example Configuration



MPC97H73 example configuration (feedback of QFB = 33.3 MHz, f_{VCO}=400 MHz, VCO_SEL=÷1, M=12, N_A=12, N_B=4, N_C=2).

Frequency range	Min	Max
Input	16.6 MHz	40 MHz
QA outputs	16.6 MHz	40 MHz
QB outputs	50 MHz	120 MHz
QC outputs	100 MHz	240 MHz

Figure 4. Example Configuration



MPC97H73 example configuration (feedback of QFB = 25 MHz, f_{VCO}=250 MHz, VCO_SEL=÷1, M=10, N_A=4, N_B=4, N_C=2).

Frequency range	Min	Max
Input	20 MHz	48 MHz
QA outputs	50 MHz	120 MHz
QB outputs	50 MHz	120 MHz
QC outputs	100 MHz	240 MHz

MPC97H73 Individual Output Disable (Clock Stop) Circuitry

The individual clock stop (output enable) control of the MPC97H73 allows designers, under software control, to implement power management into the clock distribution design. A simple serial interface and a clock stop control logic provides a mechanism through which the MPC97H73 clock outputs can be individually stopped in the logic '0' state: The clock stop mechanism allows serial loading of a 12–bit serial input register. This register contains one programmable clock stop bit for 12 of the 14 output clocks. The QC0 and QFB outputs cannot be stopped (disabled) with the serial port.

The user can program an output clock to stop (disable) by writing logic '0' to the respective stop enable bit. Likewise, the user may programmably enable an output clock by writing logic '1' to the respective enable bit. The clock stop logic enables or disables clock outputs during the time when the output would be in normally in logic low state, eliminating the possibility of short or 'runt' clock pulses.

The user can write to the serial input register through the STOP_DATA input by supplying a logic '0' start bit followed serially by 12 NRZ disable/enable bits. The period of each STOP_DATA bit equals the period of the free–running STOP_CLK signal. The STOP_DATA serial transmission should be timed so the MPC97H73 can sample each STOP_DATA bit with the rising edge of the free–running STOP_CLK signal. (see Figure 5.)

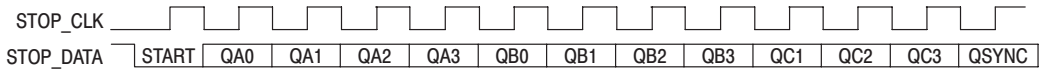


Figure 5. Clock Stop Circuit Programming

SYNC Output Description

The MPC97H73 has a system synchronization pulse output QSYNC. In configurations with the output frequency relationships are not integer multiples of each other QSYNC provides a signal for system synchronization purposes. The MPC97H73 monitors the relationship between the A bank and the B bank of outputs. The QSYNC output is asserted (logic low) one period in duration and one period prior to the coincident rising edges of the QA and QC outputs. The duration and the placement of the pulse is dependent QA and QC output frequencies: the QSYNC pulse width is equal to the period of the higher of the QA and QC output frequencies. Figure 6. shows various waveforms for the QSYNC output. The QSYNC output is defined for all possible combinations of the bank A and bank C outputs.

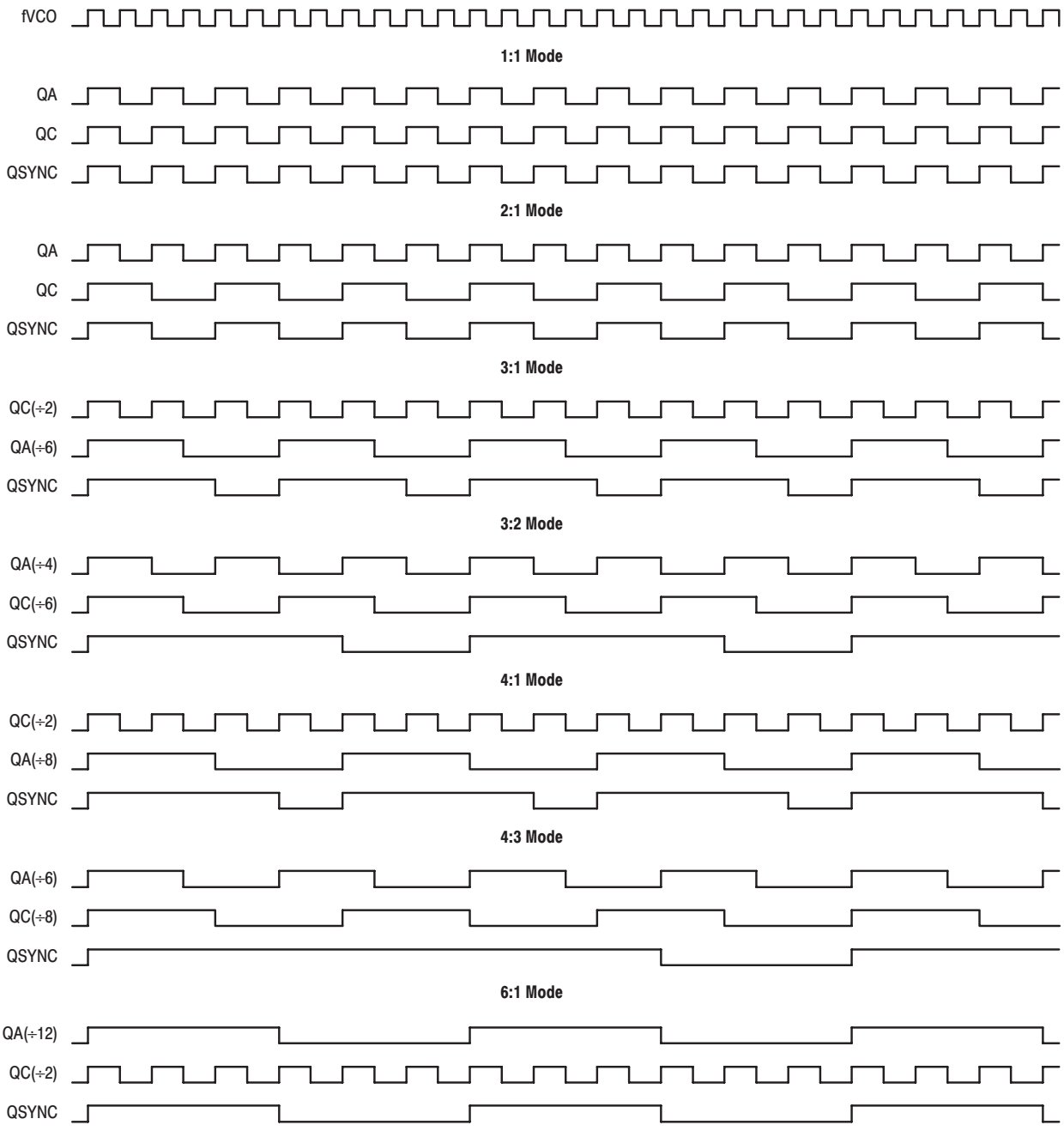


Figure 6. QSYNC Timing Diagram

Power Supply Filtering

The MPC97H73 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC97H73 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA_PLL} pin for the MPC97H73. Figure 7. illustrates a typical power supply filter scheme. The MPC97H73 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 8 mA (13.5 mA maximum), assuming that a minimum of 3.0V must be maintained on the V_{CC_PLL} pin. The resistor R_F shown in Figure 7. "V_{CC_PLL} Power Supply Filter" must have a resistance of 5-10Ω to meet the voltage drop criteria.

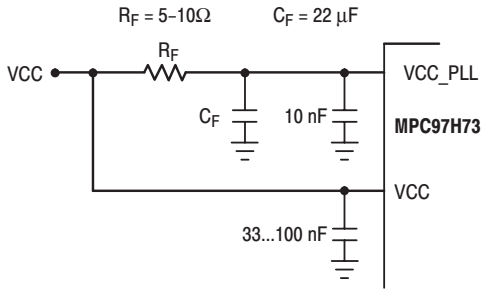


Figure 7. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 7. "V_{CC_PLL} Power Supply Filter", the filter cut-off frequency is around 4.5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC97H73 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC97H73 in zero–delay applications

Nested clock trees are typical applications for the MPC97H73. Designs using the MPC97H73 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC97H73 clock driver allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of part-to-part skew

The MPC97H73 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC97H73 are connected together, the maximum overall timing uncertainty from the common CCLKx input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

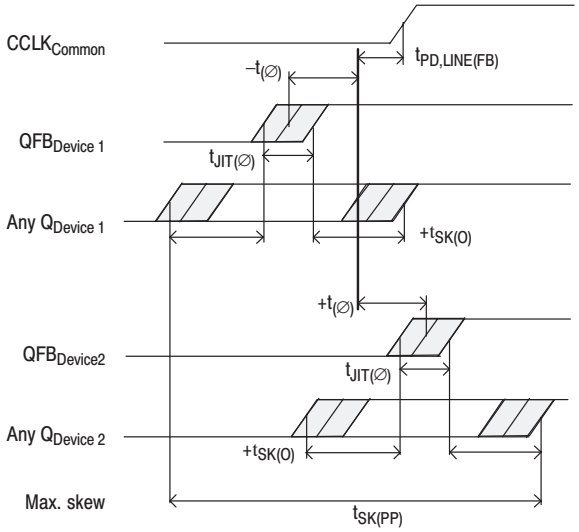


Figure 8. MPC97H73 max. device-to-device skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 12.

Table 12. Confidence Facter CF

CF	Probability of clock edge within the distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device.

Due to the frequency dependence of the static phase offset and I/O jitter, using Figure 9. to Figure 11. to predict a maximum I/O jitter and the specified $t_{(\varnothing)}$ parameter relative to the input reference frequency results in a precise timing performance analysis.

In the following example calculation an I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from the common input reference clock to any output of -455 ps to +455 ps relative to CCLK (PLL feedback = ÷8, reference frequency = 50 MHz, VCO frequency = 400 MHz, I/O jitter = 13 ps rms max., static phase offset $t_{(\varnothing)}$ = ± 166 ps):

$$t_{SK(PP)} = [–166ps...166ps] + [–250ps...250ps] + [(13ps \cdot –3)...(13ps \cdot 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [–455ps...455ps] + t_{PD,\ LINE(FB)}$$

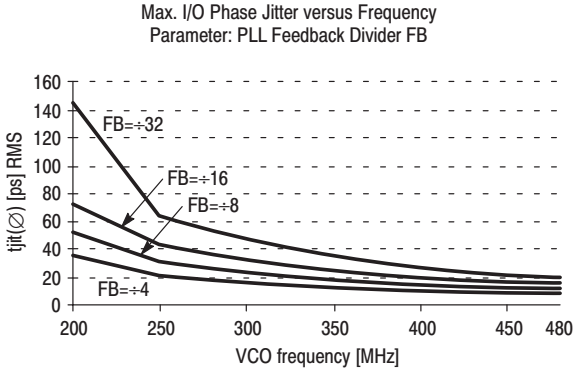


Figure 9. MPC9772 I/O Jitter

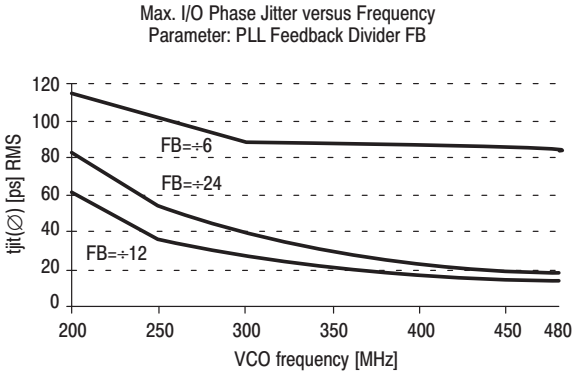


Figure 10. MPC9772 I/O Jitter

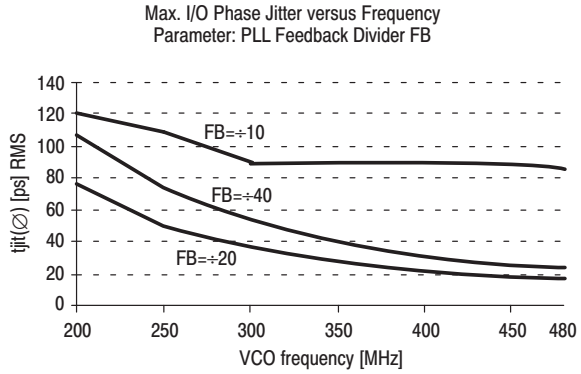


Figure 11. MPC9772 I/O Jitter

Driving Transmission Lines

The MPC97H73 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC97H73 clock driver. For the series terminated case however there is no DC current draw, thus

the outputs can drive multiple series terminated lines. Figure 12. “Single versus Dual Transmission Lines” illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC97H73 clock driver is effectively doubled due to its capability to drive multiple lines.

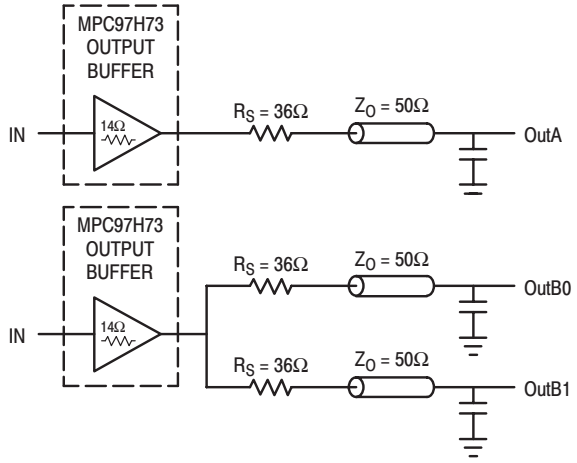


Figure 12. Single versus Dual Transmission Lines

The waveform plots in Figure 13. “Single versus Dual Line Termination Waveforms” show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC97H73 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC97H73. The output waveform in Figure 13. “Single versus Dual Line Termination Waveforms” shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S+R_0 +Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 36\Omega \parallel 36\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0 (25 \div (18+17+25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

1. Final skew data pending specification.

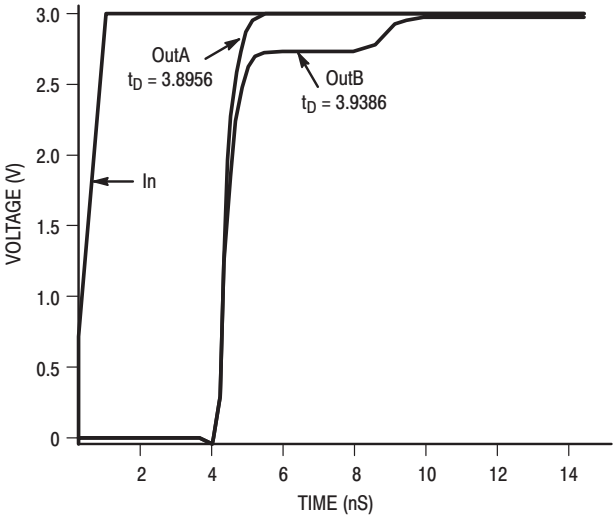
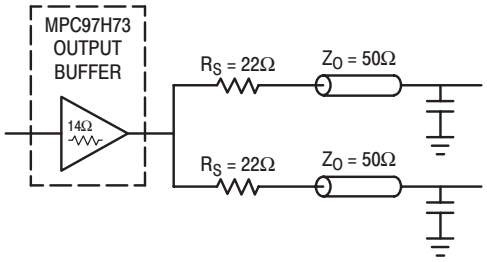


Figure 13. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 14. “Optimized Dual Line Termination” should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

Figure 14. Optimized Dual Line Termination

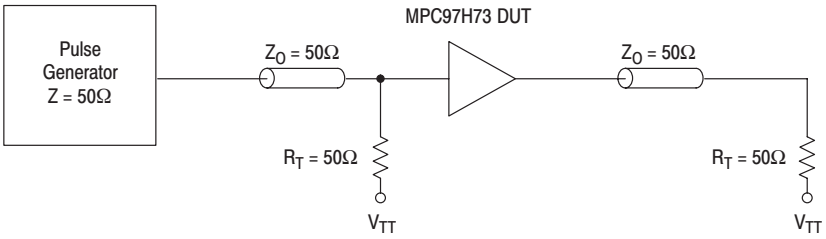


Figure 15. CCLK MPC97H73 AC test reference

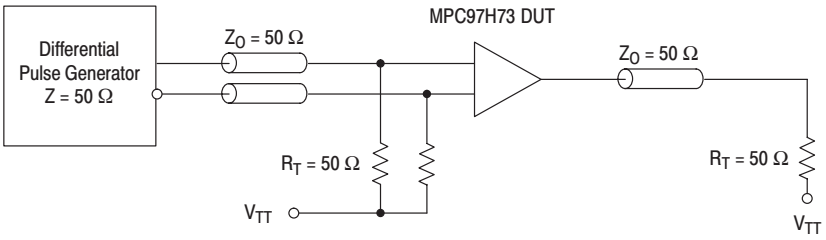
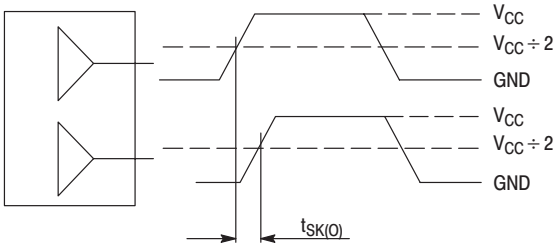


Figure 16. PCLK MPC97H73 AC test reference



The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 17. Output–to–output Skew $t_{SK(O)}$

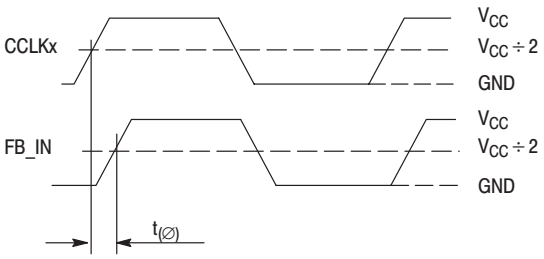
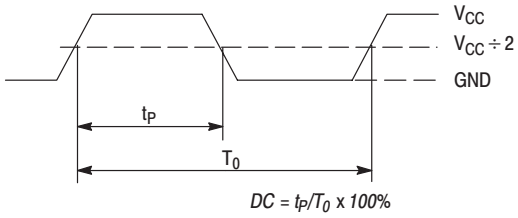
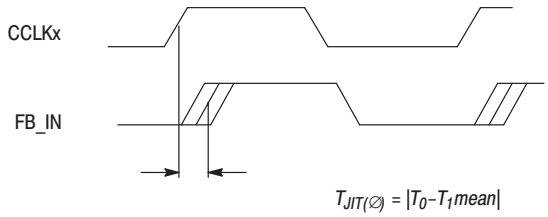


Figure 18. Propagation delay ($t_{(\varnothing)}$, static phase offset) test reference



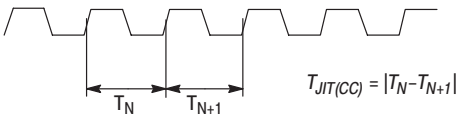
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 19. Output Duty Cycle (DC)



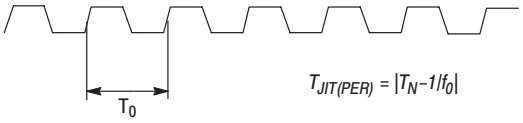
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 20. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 21. Cycle–to–cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 22. Period Jitter

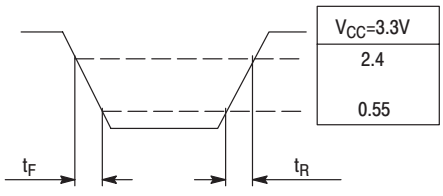
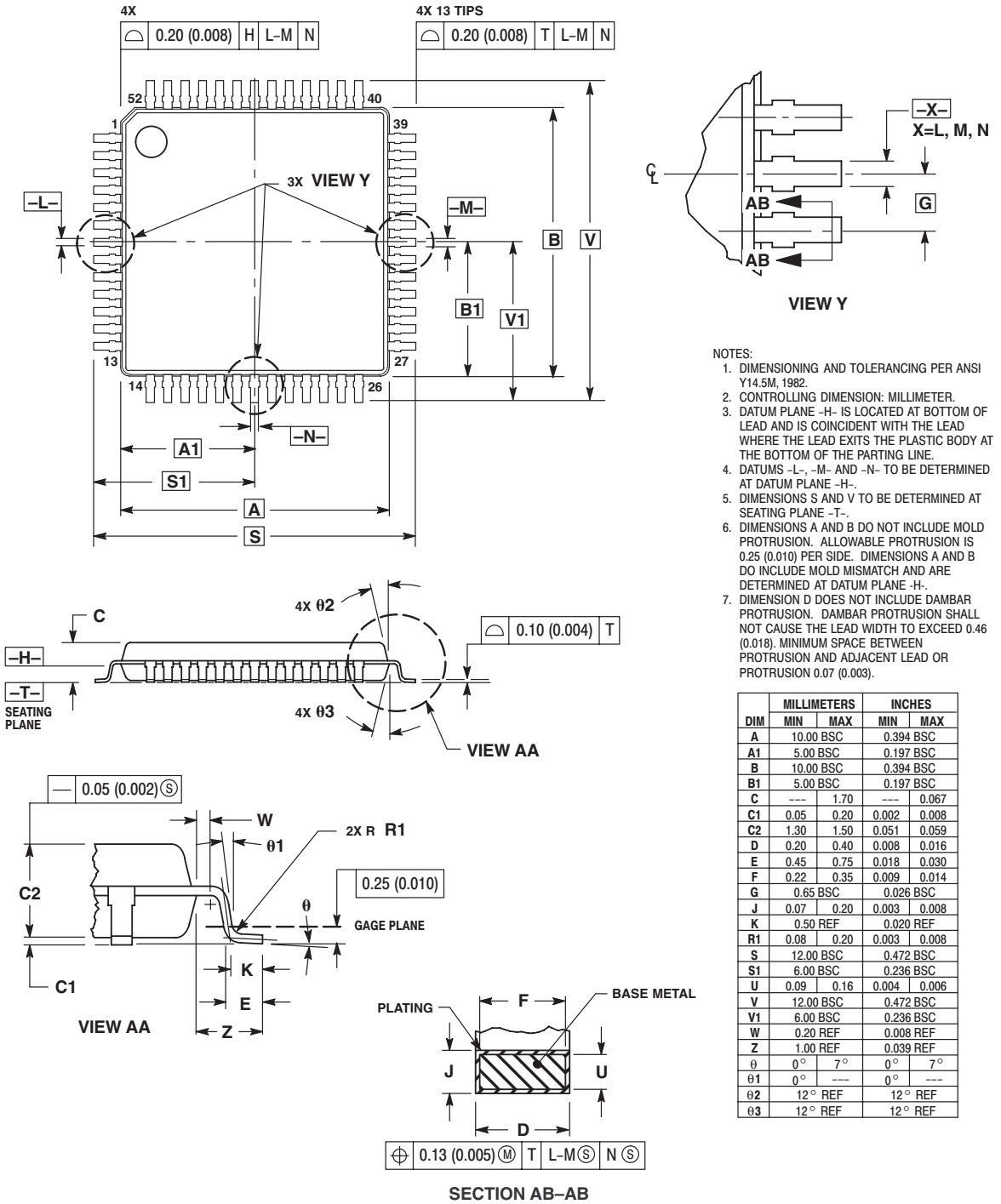


Figure 23. Output Transition Time Test Reference

OUTLINE DIMENSIONS

FA SUFFIX
52 LEAD LQFP PACKAGE
CASE 848D-03
ISSUE D



SECTION AB–AB
ROTATED 90° CLOCKWISE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -L-, -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	---	1.70	---	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	---	0°	---
θ2	12° REF		12° REF	
θ3	12° REF		12° REF	

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