DATA SHEET

Low Voltage PLL Clock Driver

MPC9350

The MPC9350 is a 2.5 V and 3.3 V compatible, PLL-based clock generator targeted for high performance clock distribution systems. With output frequencies of up to 200 MHz and maximum output skews of 150 ps, the MPC9350 is ideal for the most demanding clock tree designs. The device offers 9 low skew clock outputs, with each one configurable to support the clocking needs of the various high-performance microprocessors, including the PowerQUICC II integrated communication microprocessor. The extended temperature range of the MPC9350 supports telecommunication and networking requirements. The device employs a fully differential PLL design to minimize cycle-to-cycle and long-term jitter.

LOW VOLTAGE
3.3 V AND 2.5 V PLL
CLOCK GENERATOR

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

AC SUFFIX
32-LEAD LQFP PACKAGE
Pb-FREE PACKAGE
CASE 873A-03

Features

- 9 output LVCMOS PLL clock generator
- 25 – 200 MHz output frequency range
- 2.5 V and 3.3 V compatible
- Compatible to various microprocessors such as PowerQuicc II
- Supports networking, telecommunications and computer applications
- Fully integrated PLL
- Configurable outputs: divide-by-2, 4 and 8 of VCO frequency
- Selectable output to input frequency ratio of 8:1, 4:1, 2:1 or 1:1
- Oscillator or crystal reference inputs
- Internal PLL feedback
- Output disable
- PLL enable/disable
- Low skew characteristics: maximum 150 ps output-to-output
- 32-lead LQFP package
- 32-lead Pb-free Package Available
- Temperature range –40°C to +85°C

Functional Description

The MPC9350 generates high frequency clock signals and provides nine exact frequency-multiplied copies of the reference clock signal. The internal PLL allows the MPC9350 to operate in frequency locked condition and to multiply the input reference clock. The reference clock frequency and the divider in the internal feedback path determine the VCO frequency. Two selectable PLL feedback frequency ratios are available on the MPC9350 to provide input frequency range flexibility. The FBSEL pin selects between divide-by-16 or divide-by-32 of the VCO frequency for PLL feedback. This feedback divider must be selected to match the VCO frequency range. With the available feedback output dividers, the internal VCO of the MPC9350 is running at either 16x or 32x of the reference clock frequency. The frequency of the QA, QB, QC and QD outputs is either one half, one fourth or one eighth of the selected VCO frequency and can be configured for each output bank using the FSELA, FSELB, FSELC and FSELD pins, respectively. The available output to input frequency ratios are 16:1, 8:1, 4:1 and 2:1. The REF_SEL pin selects the crystal oscillator input or the LVCMOS compatible reference input (TCLK). TCLK also provides an external test clock in static test mode when the PLL enable pin (PLL_EN) is pulled to logic low state. In test mode, the selected input reference clock is routed directly to the output dividers without using the PLL. The test mode is intended for system diagnostics, test and debug purposes. This test mode is fully static and the minimum clock frequency specification does not apply. The outputs can be disabled by deasserting the $\overline{OE}$ pin (logic high state). In PLL mode, deasserting $\overline{OE}$ maintains PLL lock due to the internal feedback path. The MPC9350 is fully 2.5 V and 3.3 V compatible and requires no external loop filter components. The on-chip crystal oscillator requires no external components beyond a series resonant crystal. All inputs except the crystal oscillator interface accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9350 outputs can drive one or two traces giving the device an effective fanout of 1:18. The device is packaged in a 7x7 mm^2 32-lead LQFP package.

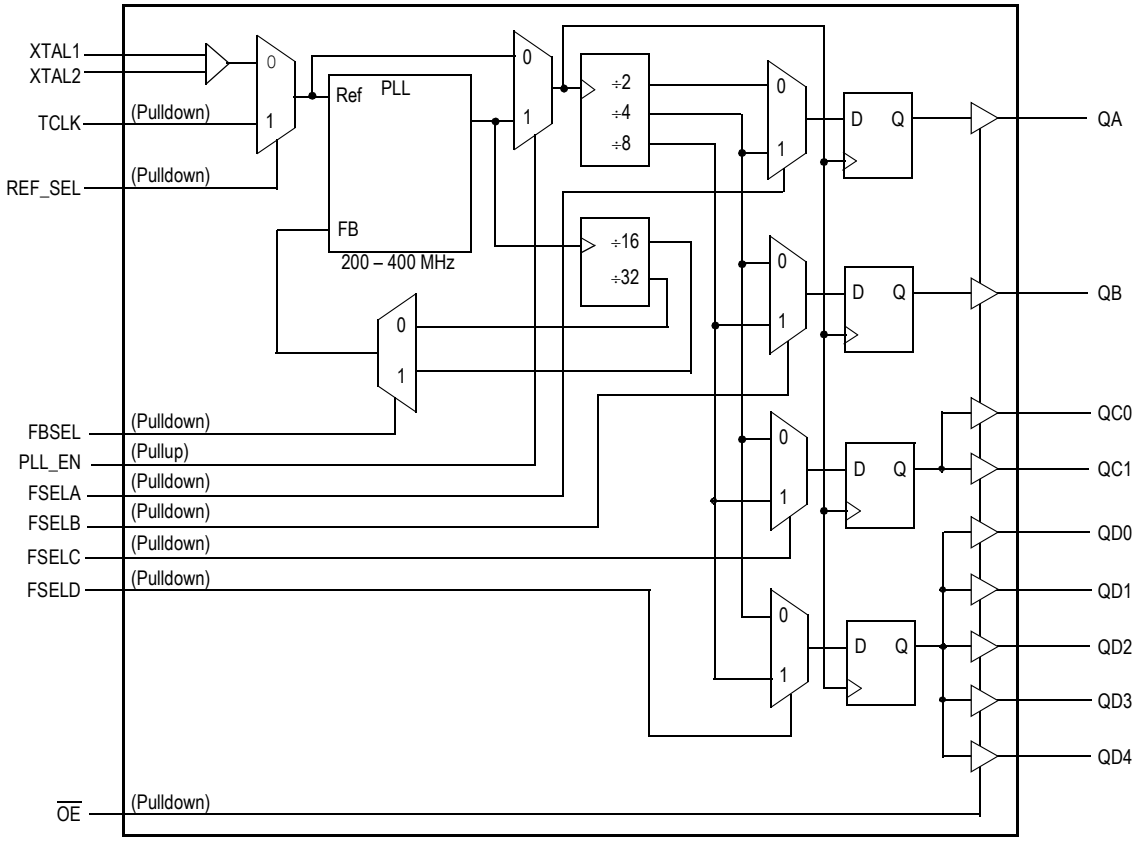


Figure 1. MPC9350 Logic Diagram

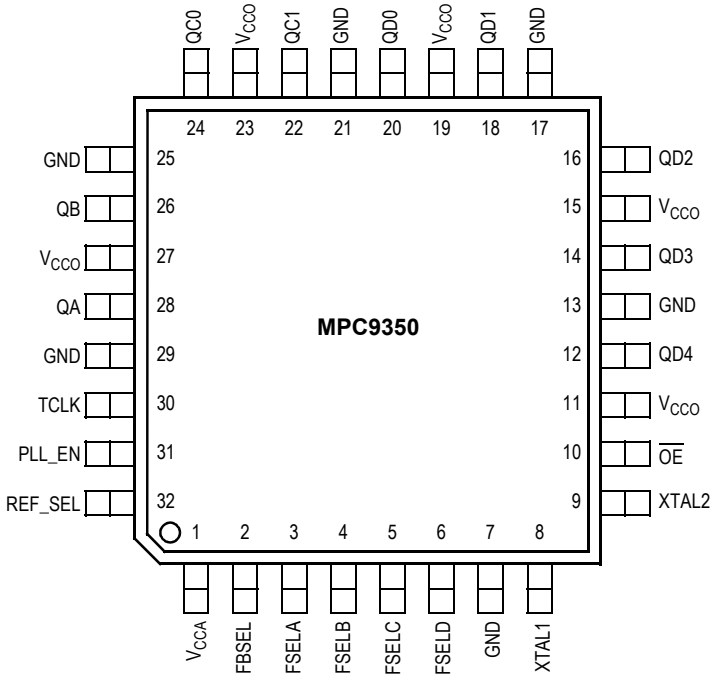


Figure 2. Pinout: 32-Lead Package Pinout (Top View)

Table 1. Pin Description

Number	Name	Type	Description
XTAL1, XTAL2	Input	Analog	Crystal oscillator terminals
TCLK	Input	LVCMOS	Single ended reference clock signal or test clock
FBSEL	Input	LVCMOS	Selects feedback divider ratio
REF_SEL	Input	LVCMOS	Selects input reference source
FSELA	Input	LVCMOS	Output A divider selection
FSELB	Input	LVCMOS	Output B divider selection
FSELC	Input	LVCMOS	Outputs C divider selection
FSELD	Input	LVCMOS	Outputs D divider selection
OE	Input	LVCMOS	Output enable/disable
QA	Output	LVCMOS	Bank A clock output
QB	Output	LVCMOS	Bank B clock output
QC0, QC1	Output	LVCMOS	Bank C clock outputs
QD0 – QD4	Output	LVCMOS	Bank D clock outputs
GND	Supply	Ground	Negative power supply
V_{CCA}	Supply	V_{CC}	Positive power supply for the PLL
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core

Table 2. Function Table

Control	Default	0	1
REF_SEL	0	Selects XTAL	Selects TCLK
PLL_EN	1	Test mode with PLL disabled. The input clock is directly routed to the output dividers	PLL enabled. The VCO output is routed to the output dividers
FBSEL	0	Selects feedback divider ÷ 32 VCO = 32 * Input reference clock	Selects feedback divider ÷ 16 VCO = 16 * Input reference clock
$\overline{OE}$	0	Outputs enabled	Outputs disabled
FSELA	0	QA = VCO ÷ 2	QA = VCO ÷ 4
FSELB	0	QB = VCO ÷ 4	QB = VCO ÷ 8
FSELC	0	QC = VCO ÷ 4	QC = VCO ÷ 8
FSELD	0	QD = VCO ÷ 4	QD = VCO ÷ 8

Table 3. Absolute Maximum Ratings(1)

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	4.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage temperature	–40	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 4. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = -40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input low voltage	–0.3		0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –24 mA(1)
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
I_{IN}	Input Current			200	µA	V_{IN} = 0 V or V_{IN} = V_{CC}
Z_{OUT}	Output impedance		14 – 17		Ω	
C_{IN}	Input capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		10		pF	Per Output
I_{CCA}	Maximum PLL Supply Current			10	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins
V_{TT}	Output termination voltage		V_{CC}÷2		V	

1. The MPC9350 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.

Table 5. AC Characteristics (V_{CC} = 3.3 V ± 5% or V_{CC} = 2.5 V ± 5%, T_A = -40° to 85°C)(1)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency ÷ 16 feedback ÷ 32 feedback Static Test Mode	 12.5 6.25 0		 25 12.5 300	 MHz MHz MHz	 FBSEL = 1 FBSEL = 0 PLL_EN = 0
f_{XTAL}	Crystal Oscillator Frequency	10		25	MHz	XTAL inputs
f_{VCO}	VCO Frequency	200		400	MHz	PLL_EN = 1
f_{MAX}	Maximum Output Frequency ÷ 2 output ÷ 4 output ÷ 8 output	 100 50 25		 200 100 50	 MHz MHz MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
t_r, t_f	TLCK Input Rise/Fall Time V_{CC} = 2.5 V V_{CC} = 3.3 V			1.0 1.0	ns ns	0.7 V to 1.7 V 0.8 V to 2.0 V
$t_{sk(o)}$	Output-to-output Skew		45	150	ps	
t_{PW}	Output Duty Cycle	45	50	55	ps	T=Clock period
t_r, t_f	Output Rise/Fall Time	0.1	0.5	1.0	ns	see **Figure 10**
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
BW	PLL closed loop bandwidth ÷ 16 feedback (V_{CC} = 3.3 V) ÷ 16 feedback (V_{CC} = 2.5 V) ÷ 32 feedback (V_{CC} = 3.3 V) ÷ 32 feedback (V_{CC} = 2.5 V)		 2.0 – 8.0 1.0 – 4.0 1.5 – 3.5 0.7 – 2.0		 MHz MHz MHz MHz	
$t_{JIT(CC)}$	Cycle-to-cycle jitter single frequency multiple frequencies		30 100	200 300	ps ps	
$t_{JIT(PER)}$	Period Jitter ÷ 16 feedback ÷ 32 feedback		30 80	150 200	ps ps	
t_{LOCK}	Maximum PLL Lock Time			1	ms	
$t_{JIT(∅)}$	I/O Phase Jitter (RMS)		5 – 20		ps	RMS value

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.

Table 6. DC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = -40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input low voltage	–0.3		0.7	V	LVCMOS
V_{OH}	Output High Voltage	1.8			V	I_{OH} = –15 mA(1)
V_{OL}	Output Low Voltage			0.6	V	I_{OL} = 15 mA
Z_{OUT}	Output impedance		17 – 20		Ω	
I_{IN}	Input Current			200	µA	V_{IN} = 0 V or V_{IN} = V_{CC}
C_{IN}	Input capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		10		pF	Per Output
I_{CCA}	Maximum PLL Supply Current			10	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins
V_{TT}	Output termination voltage		V_{CC}÷2		V	

1. The MPC9350 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines per output.

APPLICATIONS INFORMATION

Programming the MPC9350

The MPC9350 clock driver outputs can be configured into several divider modes. In addition, the internal feedback of the device allows for flexibility in establishing two input to output frequency relationships. The output division settings establish the output frequency relationship. The output divider of the four output groups allows the user to configure the outputs into 1:1, 2:1, 4:1 and 4:2:1 frequency ratios. The use of even dividers ensures that the output duty cycle is always 50%. Table 7 and Table 8 illustrate the various output configurations. The tables describe the outputs using the input clock frequency CLK as a reference.

In addition, it must be ensured that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL supports output frequencies from 25 MHz to 200 MHz while the VCO frequency range is specified from 200 MHz to 400 MHz and should not be exceeded for stable operation.

Table 7. Output Frequency Relationship(1) FBSEL = 0, (VC0 = 32 * CLK)

Inputs				Outputs			
FSELA	FSELB	FSELC	FSELD	QA	QB	QC0, QC1	QD0–QD4
0	0	0	0	16 * CLK	8 * CLK	8 * CLK	8 * CLK
0	0	0	1	16 * CLK	8 * CLK	8 * CLK	4 * CLK
0	0	1	0	16 * CLK	8 * CLK	4 * CLK	8 * CLK
0	0	1	1	16 * CLK	8 * CLK	4 * CLK	4 * CLK
0	1	0	0	16 * CLK	4 * CLK	8 * CLK	8 * CLK
0	1	0	1	16 * CLK	4 * CLK	8 * CLK	4 * CLK
0	1	1	0	16 * CLK	4 * CLK	4 * CLK	8 * CLK
0	1	1	1	16 * CLK	4 * CLK	4 * CLK	4 * CLK
1	0	0	0	8 * CLK	8 * CLK	8 * CLK	8 * CLK
1	0	0	1	8 * CLK	8 * CLK	8 * CLK	4 * CLK
1	0	1	0	8 * CLK	8 * CLK	4 * CLK	8 * CLK
1	0	1	1	8 * CLK	8 * CLK	4 * CLK	4 * CLK
1	1	0	0	8 * CLK	4 * CLK	8 * CLK	8 * CLK
1	1	0	1	8 * CLK	4 * CLK	8 * CLK	4 * CLK
1	1	1	0	8 * CLK	4 * CLK	4 * CLK	8 * CLK
1	1	1	1	8 * CLK	4 * CLK	4 * CLK	4 * CLK

1. Output frequency relationship with respect to input reference frequency CLK. Consult the MPC9351 data sheet for more input to output relationships in external feedback mode.

Table 8. Output Frequency Relationship(1) FBSEL = 1, (VC0 = 16 * CLK)

Inputs				Outputs			
FSELA	FSELB	FSELC	FSELD	QA	QB	QC0, QC1	QD0–QD4
0	0	0	0	8 * CLK	4 * CLK	4 * CLK	4 * CLK
0	0	0	1	8 * CLK	4 * CLK	4 * CLK	2 * CLK
0	0	1	0	8 * CLK	4 * CLK	2 * CLK	4 * CLK
0	0	1	1	8 * CLK	4 * CLK	2 * CLK	2 * CLK
0	1	0	0	8 * CLK	2 * CLK	4 * CLK	4 * CLK
0	1	0	1	8 * CLK	2 * CLK	4 * CLK	2 * CLK
0	1	1	0	8 * CLK	2 * CLK	2 * CLK	4 * CLK
0	1	1	1	8 * CLK	2 * CLK	2 * CLK	2 * CLK
1	0	0	0	4 * CLK	4 * CLK	4 * CLK	4 * CLK
1	0	0	1	4 * CLK	4 * CLK	4 * CLK	2 * CLK
1	0	1	0	4 * CLK	4 * CLK	2 * CLK	4 * CLK
1	0	1	1	4 * CLK	4 * CLK	2 * CLK	2 * CLK
1	1	0	0	4 * CLK	2 * CLK	4 * CLK	4 * CLK
1	1	0	1	4 * CLK	2 * CLK	4 * CLK	2 * CLK
1	1	1	0	4 * CLK	2 * CLK	2 * CLK	4 * CLK
1	1	1	1	4 * CLK	2 * CLK	2 * CLK	2 * CLK

1. Output frequency relationship with respect to input reference frequency CLK. Consult the MPC9351 data sheet for more input to output relationships in external feedback mode.

Power Supply Filtering

The MPC9350 is a mixed analog/digital product and as such, it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC9350 provides separate power supplies for the output buffers (V_{CCO}) and the phase-locked loop (V_{CCA}) of the device.

The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient; however, in a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC9350. Figure 3 illustrates a typical power supply filter scheme. The MPC9350 is most susceptible to noise with spectral content in the 10 kHz to 5 MHz range; therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC9350. From the data sheet the I_{VCCA} current (the current sourced through the V_{CCA} pin) is typically 10 mA (15 mA maximum), assuming that a minimum of 3.0 V must be maintained on the V_{CCA} pin. Very little DC voltage drop can be tolerated when a 3.3 V V_{CC} supply is used. The resistor shown in Figure 3 must have a resistance of 10–15 Ω to meet the voltage drop criteria for V_{CC} = 3.3 V. For V_{CC} = 2.5 V operation, R_S must be selected to maintain the minimum V_{CC} specification of 2.375 V for the PLL supply pin for proper operation. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor, its overall impedance begins to look inductive and, thus, increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10 Ω resistor to avoid potential V_{CC} drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

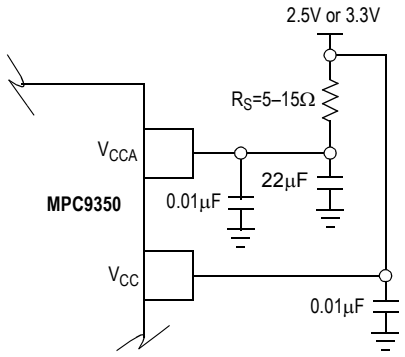


Figure 3. Power Supply Filter

Although the MPC9350 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC9350 clock driver was designed to drive high-speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 15 Ω, the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Freescale application note AN1091. In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current, and thus, only a single terminated line can be driven by each output of the MPC9350 clock driver. For the series terminated case, however, there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the MPC9350 clock driver is effectively doubled due to its capability to drive multiple lines.

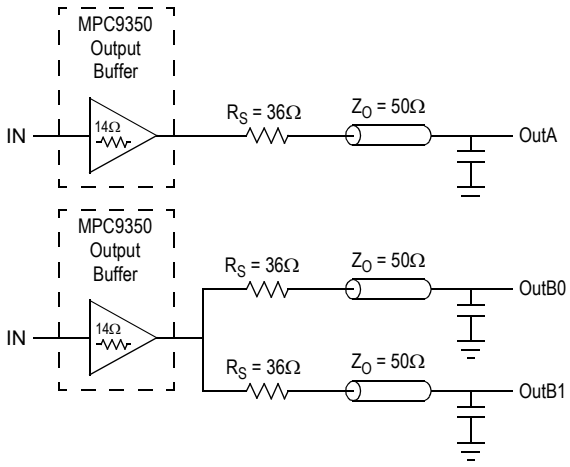


Figure 4. Single versus Dual Transmission Lines

The waveform plots in Figure 5 show the simulation results of an output driving a single line versus two lines. In both cases, the drive capability of the MPC9350 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations, a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight

output-to-output skew of the MPC9350. The output waveform in Figure 5 shows a step in the waveform. This step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\ \Omega \parallel 50\ \Omega$$
$$R_S = 36\ \Omega \parallel 36\ \Omega$$
$$R_0 = 17\ \Omega$$
$$V_L = 3.0\ (25 \div (18+17+25))$$
$$= 1.25\ V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5 V. It will then increment toward the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

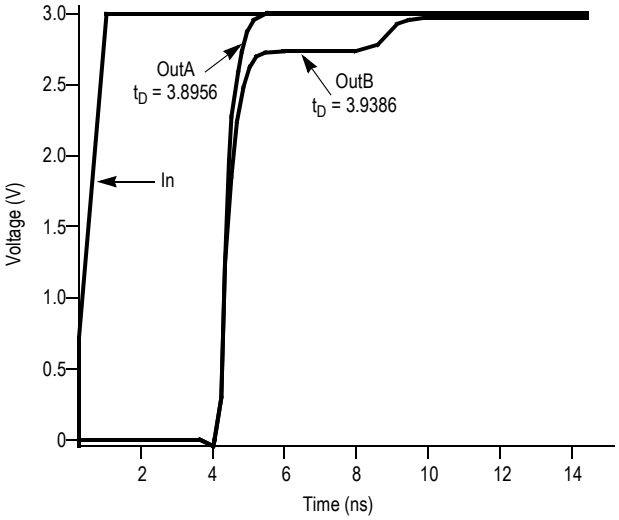
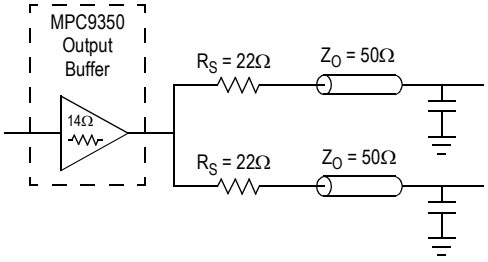


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region, it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance, the line impedance is perfectly matched.



$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

Figure 6. Optimized Dual Line Termination

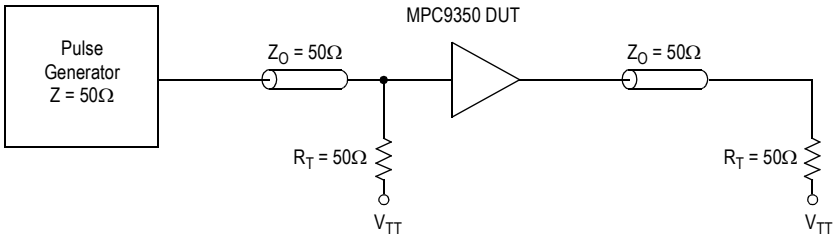
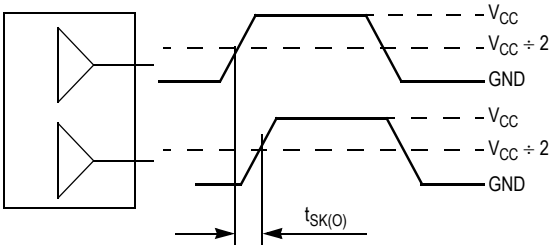
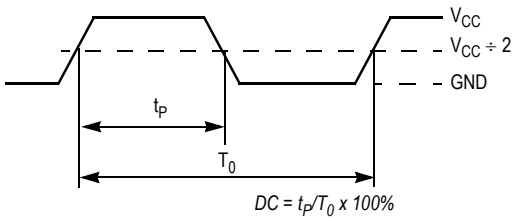


Figure 7. TCLK MPC9350 AC Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V



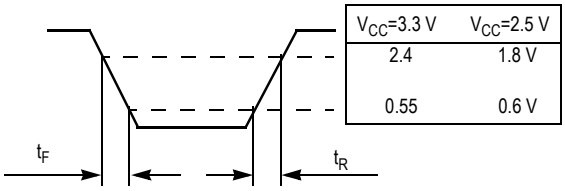
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device.

Figure 8. Output-to-Output Skew $t_{SK(O)}$



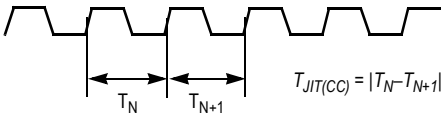
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage.

Figure 9. Output Duty Cycle (DC)



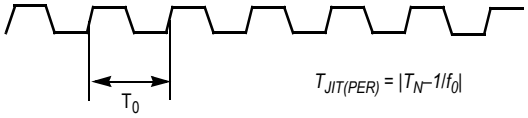
The time from the maximum low level voltage to minimum high level of a clock signal, expressed in ns.

Figure 10. Transition Time Test Reference



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs.

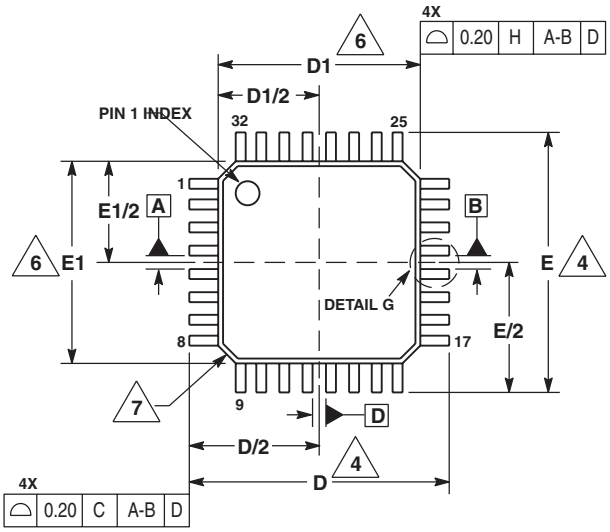
Figure 11. Cycle-to-Cycle Jitter

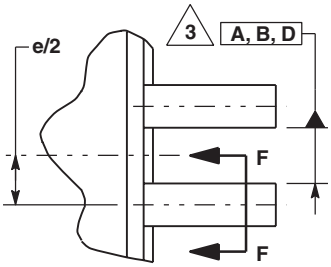


The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles.

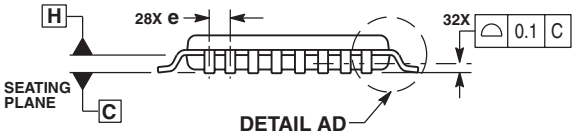
Figure 12. Period Jitter

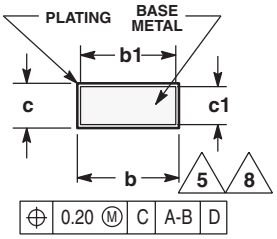
PACKAGE DIMENSIONS



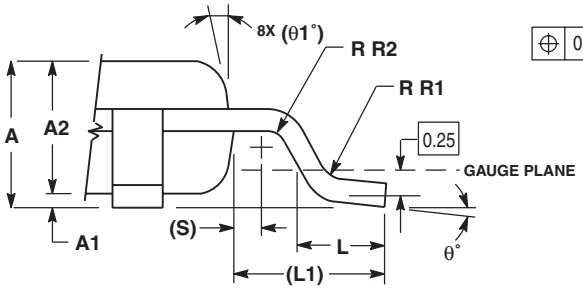


DETAIL G





SECTION F-F



DETAIL AD

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08-mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07-mm.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25-mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1-mm AND 0.25-mm FROM THE LEAD TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	1.40	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.30	0.45
b1	0.30	0.40
c	0.09	0.20
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
e	0.80 BSC	
E	9.00 BSC	
E1	7.00 BSC	
L	0.50	0.70
L1	1.00 REF	
q	0°	7°
q1	12 REF	
R1	0.08	0.20
R2	0.08	---
S	0.20 REF	

CASE 873A-03
ISSUE B
32-LEAD LQFP PACKAGE

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