SPREAD SPECTRUM CLOCK GENERATOR

MK1493-14

Description

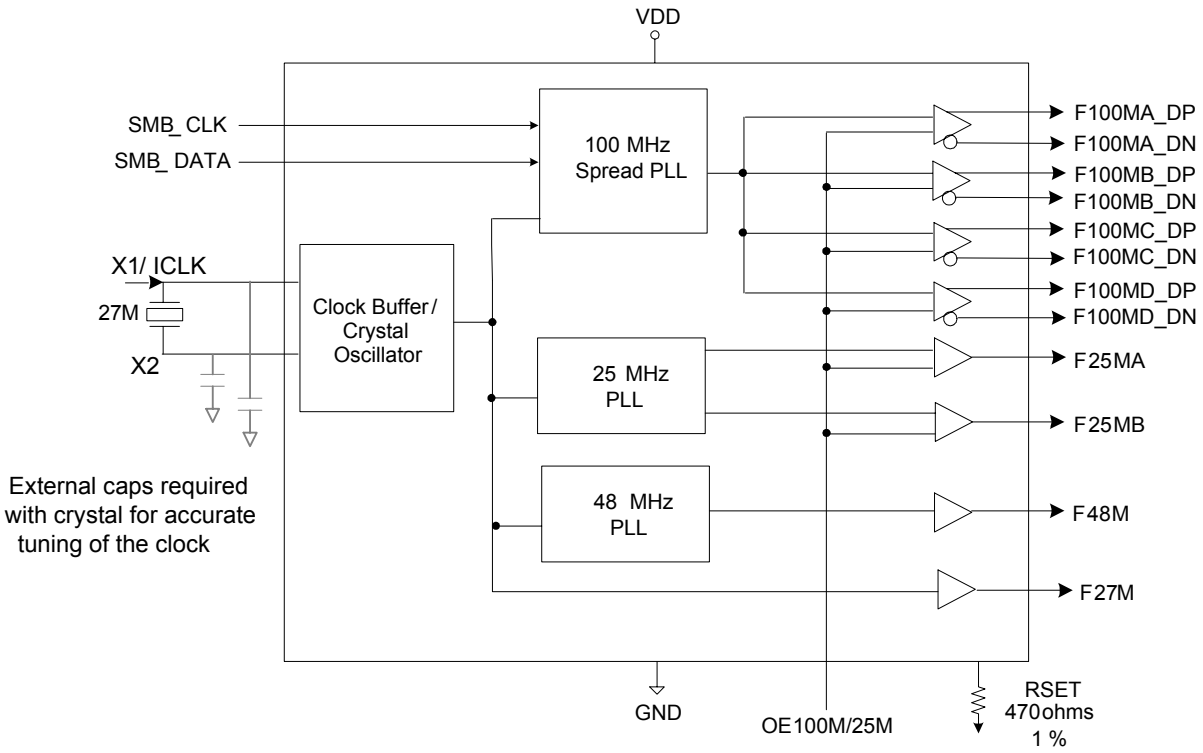
The MK1493-14 is a spread spectrum clock designed for embedded applications. The device takes a reference clock or crystal input of 27 MHz and provides four differential HCSL outputs at 100 MHz for Serial ATA and PCI-Express. The current mode differential outputs comply directly with HCSL (0.7 V) norms. In addition, a 27 MHz video reference clock, two 25 MHz Ethernet clocks and one 48 MHz USB clock are generated at single-ended CMOS levels.

The MK1493-14 includes an SMBus interface to control the spread and drive strength of the 100 MHz HCSL outputs. The reference current, IREF, is set by a 475 ohm resistor on the RSET pin, and the drive strength of each 100 MHz output can be programmed as 4X, 5X, 6X or 7X IREF.

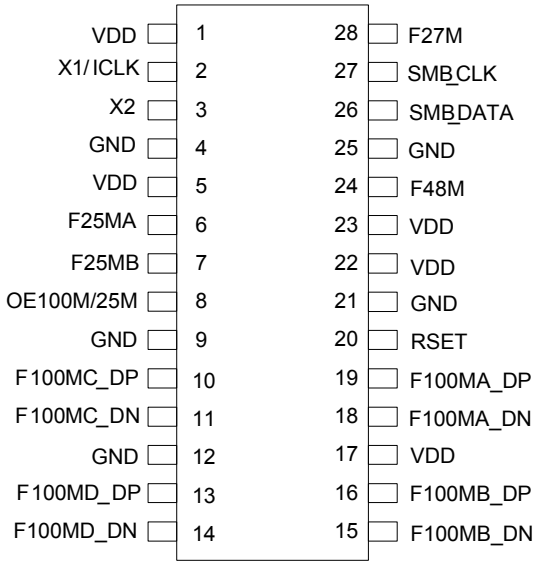
Features

- Single-ended clock or crystal input of 27 MHz
- Four pairs of 100 MHz outputs, (HCSL, 0.7 V current mode differential pair) with selectable spread
- Two 25 MHz Ethternet clock outputs (LVCMOS)
- One 48 MHz USB clock output (LVCMOS)
- One 27 MHz video reference output (LVCMOS)
- ±125 ps peak-to-peak max jitter on 100 MHz clocks
- ±200 ps peak-to-peak max jitter on 27 MHz reference and 25 MHz clocks
- Packaged in 28-pin TSSOP Pb (lead) free package
- Operating voltage of 3.3 V
- Low power consumption

Block Diagram



Pin Assignment



Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	VDD	Power	Connect to voltage supply +3.3 V.
2	X1/ICLK	Input	Crystal or clock input. Connect to a 27 MHz crystal or single ended clock.
3	X2	Output	Crystal connection. Leave unconnected for clock input.
4	GND	Power	Connect to ground.
5	VDD	Power	Connect to voltage supply +3.3 V.
6	F25MA	Output	25 MHz Ethernet clock output. Internal pull-down resistor.
7	F25MB	Output	25 MHz Ethernet clock output. Internal pull-down resistor.
8	OE100M/25M	Input	Output Enable for F100Mx and F25Mx clocks. Internal pull-down resistor. OE100M/25M = 1 enables all outputs. See Table 1.
9	GND	Power	Connect to ground.
10	F100MC_DP	Output	100 MHz differential clock (+), small spread.
11	F100MC_DN	Output	100 MHz differential clock (-), small spread.
12	GND100M	Power	Connect to ground.
13	F100MD_DP	Output	100 MHz differential clock (+), small spread.
14	F100MD_DN	Output	100 MHz differential clock (-), small spread.
15	F100MB_DN	Output	100 MHz differential clock (-), small spread.
16	F100MB_DP	Output	100 MHz differential clock (+), small spread.
17	VDD	Power	Connect to voltage supply +3.3 V
18	F100MA_DN	Output	100 MHz differential clock (-), small spread.
19	F100MA_DP	Output	100 MHz differential clock (+), small spread.

Pin Number	Pin Name	Pin Type	Pin Description
20	RSET	Input	Current set for all Differential clock drivers, attach 475 Ω resistor.
21	GND	Power	Connect to ground.
22	VDD	Power	Connect to voltage supply +3.3 V.
23	VDD	Power	Connect to voltage supply +3.3 V.
24	F48M	Output	48 MHz reference clock output.
25	GND	Power	Connect to ground.
26	SMB_DATA	Input	SMBus data input.
27	SMB_CLK	Input	SMBus clock input.
28	F27M	Output	27 MHz reference clock output.

Output Enable Control (Table 1)

OE100M/25M	F100Mx	F25Mx
0	Hi-Z	Low
1	ON	ON

General SMBus Serial Interface

How to Write:

- Controller (host) sends a start bit
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will *acknowledge*
- Controller (host) sends the beginning byte location =N
- ICS clock will *acknowledge*
- Controller (host) sends the data byte count = X
- ICS clock will *acknowledge*
- Controller (host) starts sending *Byte N through Byte N + X - 1* (see Note 2)
- ICS clock will *acknowledge* each byte *one at a time*
- Controller (host) sends a Stop bit

Index Block Write Operation

Controller (Host)			ICS(Slave/Receiver)
T	starTbit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte = N		.	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

How to Read:

- Controller (host) sends a start bit
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will *acknowledge*
- Controller (host) sends the beginning byte location =N
- ICS clock will *acknowledge*
- Controller (host) will send a separate start bit
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will *acknowledge*
- Controller (host) sends the data byte count = X
- ICS clock sends *Byte N + X - 1*
- ICS clock sends *Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)*
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation

Controller (Host)			ICS(Slave/Receiver)
T	starTbit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
			ACK
			Data Bye Count = X
ACK			
		.	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Address

The MK1493-14 is a slave-only device that supports block read and block write protocol using a single 7 bit address and read/write bit. A block write (D2h) or block read (D3h) is made up of seven (7) bits and one (1) read/write bit.

A6	A5	A4	A3	A2	A1	A0	R/W#
1	1	0	1	0	1	0	X

In applications where the indexed block write and block read are used, the dummy byte (bit 11-18) functions as a register-offset (8 bits) pointer.

Byte 0: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	F100MD Current Multiplier Control Bit S3	RW	1	F100MD_DP F100MD_DN	S3:S0=Multiplier 0011=4xIREF 0111=5xIREF 1011=6xIREF 1111=7xIREF
6	F100MD Current Multiplier Control Bit S2	RW	0	F100MD_DP F100MD_DN	
5	F100MD Current Multiplier Control Bit S1	RW	1	F100MD_DP F100MD_DN	
4	F100MD Current Multiplier Control Bit S0	RW	1	F100MD_DP F100MD_DN	
3	F100MC Current Multiplier Control Bit S3	RW	1	F100MC_DP F100MC_DN	S3:S0=Multiplier 0011=4xIREF 0111=5xIREF 1011=6xIREF 1111=7xIREF
2	F100MC Current Multiplier Control Bit S2	RW	0	F100MC_DP F100MC_DN	
1	F100MC Current Multiplier Control Bit S1	RW	1	F100MC_DP F100MC_DN	
0	F100MC Current Multiplier Control Bit S0	RW	1	F100MC_DP F100MC_DN	

Byte 1: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	F100MB Current Multiplier Control Bit S3	RW	1	F100MB_DP F100MB_DN	S3:S0=Multiplier 0011=4xIREF 0111=5xIREF 1011=6xIREF 1111=7xIREF
6	F100MB Current Multiplier Control Bit S2	RW	0	F100MB_DP F100MB_DN	
5	F100MB Current Multiplier Control Bit S1	RW	1	F100MB_DP F100MB_DN	
4	F100MB Current Multiplier Control Bit S0	RW	1	F100MB_DP F100MB_DN	
3	F100MA Current Multiplier Control Bit S3	RW	1	F100MA_DP F100MA_DN	S3:S0=Multiplier 0011=4xIREF 0111=5xIREF 1011=6xIREF 1111=7xIREF
2	F100MA Current Multiplier Control Bit S2	RW	0	F100MA_DP F100MA_DN	
1	F100MA Current Multiplier Control Bit S1	RW	1	F100MA_DP F100MA_DN	
0	F100MA Current Multiplier Control Bit S0	RW	1	F100MA_DP F100MA_DN	

Byte 2: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Spread Select for F100Mx clocks	RW	0	F100Mx_DP F100Mx_DN	0=spread off 1 = -0.5% down spread
6	Reserved	R	Undefined	Not applicable	
5	Reserved	R	Undefined	Not applicable	
4	Reserved	R	Undefined	Not applicable	
3	Reserved	R	Undefined	Not applicable	
2	Reserved	R	Undefined	Not applicable	
1	Reserved	R	Undefined	Not applicable	
0	Reserved	R	Undefined	Not applicable	

Byte 3 through 5: Control

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7 to 0	Reserved	R	Undefined	Not applicable	

Byte 6: Control Register

Bit	Description	Type	Power Up Condition	Output(s) Affected	Notes
7	Revision ID bit 3	R	0	Not applicable	
6	Revision ID bit 2	R	0	Not applicable	
5	Revision ID bit 1	R	0	Not applicable	
4	Revision ID bit 0	R	0	Not applicable	
3	Vendor ID bit 3	R	0	Not applicable	
2	Vendor ID bit 2	R	0	Not applicable	
1	Vendor ID bit 1	R	0	Not applicable	
0	Vendor ID bit 0	R	1	Not applicable	

External Components

A minimum number of external components are required for proper operation. Decoupling capacitors of 0.01 µF should be connected between VDD and GND pairs. The capacitors should be placed between pins VDD and GND pins as close to the device as possible. A 33Ω series terminating resistor should be used on each clock output if the trace is longer than 1 inch.

Crystal Information

The crystal used should be a fundamental mode, parallel resonant crystal. Do not use third overtone. Crystal capacitors should be connected from pins X1 to ground and from X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation:

Crystal caps (pF) = (C_L - 6) x 2

In the equation, C_L is the crystal load capacitance. So for a crystal with 18 pF load capacitance, two 24 pF [(18-6) x 2] capacitors should be used.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1493-14. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

DC Electrical Characteristics

Unless otherwise specified, **VDD=3.3 V ±10%**, Ambient Temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
DC Operating Voltage	VDD		3.0		3.6	V
Input High Voltage	V_{IH}	ICLK, SMB_CLK, SMB_DATA, OE100M/25M,	2			V
Input Low Voltage	V_{IL}	ICLK, SMB_CLK, SMB_DATA, OE100M/25M			0.8	V
Operating Supply Current	IDD			165	210	mA
IDD at Output Disable Condition		No load, OE100M/25M=0		90		mA
Short Circuit Current	I_{OS}	Single-ended clocks		±35		mA
Internal Pull-down Resistor	R_{PD}	OE100M/25M/F25MX		110		kΩ
Input Capacitance	C_{IN}	All input pins		6		pF

Note: 1. Nominal switching threshold is VDD/2.

AC Electrical Characteristics F27M

VDD = 3.3 V ±10%, C_L=15 pF Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Clock Frequency				27		MHz
Output Rise Time	t_{OR}	0.4 V to 2.4 V, 15 pF load	1		3	ns
Output Fall Time	t_{OF}	2.4 V to 0.4 V, 15 pF load	1		3	ns
Output Clock Duty Cycle		At VDD/2	45	50	55	%
High-Level Output Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V
High-Level Output Current	I_{OH}	Vout = 1.0 V	-29			
High-Level Output Current	I_{OH}	Vout = 3.135 V			-23	
Low-Level Output Current	I_{OL}	Vout = 1.95 V	29			
Low-Level Output Current	I_{OL}	Vout = 0.4 V			27	
Period jitter		Variation from mean		±200		ps
Cycle-to-cycle Jitter				±200		ps
Long-term Jitter		Measured at 10 µs		±400		ps
Clock Stabilization Time from Power Up					2	ms

AC Electrical Characteristics F25Mx

VDD = 3.3 V ±10%, C_L=15 pF Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Clock Frequency				25		MHz
Output Rise Time	t_{OR}	0.4V to 2.4V, 15 pF load	1		3	ns
Output Fall Time	t_{OF}	2.4V to 0.4V, 15 pF load	1		3	ns
Output Clock Duty Cycle		At VDD/2	45	50	55	%
High-Level Output Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V
High-Level Output Current	I_{OH}	Vout = 1.0 V	-29			mA
High-Level Output Current	I_{OH}	Vout = 3.135 V			-23	mA
Low-Level Output Current	I_{OL}	Vout = 1.95 V	29			mA
Low-Level Output Current	I_{OL}	Vout = 0.4 V			27	mA
Period Jitter		Variation from mean		±200		ps
Cycle-to-Cycle Jitter				±200		ps
Long-term Jitter		Measured at 10 µs		±400		ps
Clock Stabilization Time from Power Up					2	ms

AC Electrical Characteristics F48M

VDD = 3.3 V ±10%, C_L=15 pF Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Clock Frequency				48		MHz
Output Rise Time	t_{OR}	0.4 V to 2.4 V, 15 pF load	1		2	ns
Output Fall Time	t_{OF}	2.4 V to 0.4 V, 15 pF load	1		2	ns
Output Clock Duty Cycle		At VDD/2	45	50	55	%
High-Level Output Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V
High-Level Output Current	I_{OH}	Vout = 1.0 V	-29			mA
High-Level Output Current	I_{OH}	Vout = 3.135 V			-23	mA
Low-Level Output Current	I_{OL}	Vout = 1.95 V	29			mA
Low-Level Output Current	I_{OL}	Vout = 0.4 V			27	mA
Period Jitter		Variation from mean		±200		ps

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Cycle-to-Cycle Jitter				±200		ps
Long-term Jitter		Measured at 10 µs		±400		ps
Clock Stabilization Time from Power Up					2	ms

AC Electrical Characteristics F100M/F100MA/F100MB/F100MC Clock, 0.7V Current Mode Differential Pairs

Unless stated otherwise, **VDD = 3.3 V ±10%**, Ambient Temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Clock Frequency				100		MHz
Jitter, Cycle to Cycle				±85		ps
Period Jitter				±85		ps
Long-Term Jitter		Note 2, Measured at 10µs		±500		ps
Spread Range		Note 3	-0.5		0	%
Spread Rate		Note 3		31		KHz
Clock Period	T_{Period}	Note 4, 5, 6 without spread and without jitter with 0.0, -0.5% spread and jitter	 10 9.915	 10.025	 10.136	 ns
Duty Cycle	T_{DC}	Measurement from differential wave forms	45	50	55	%
Clock Stabilization from Power-up					2	ms
Rise Time	T_R	Note 7, V_{OL} = 0.175 V, V_{OH} = 0.525 V	175		700	ps
Fall Time	T_F	Note 7, V_{OL} = 0.175 V, V_{OH} = 0.525 V	175		700	ps
Rise/Fall Matching		Note 7, 8			20%	—
Output Skew	T_{OSKEW}	V_T = 50% (measurement threshold)			50	ps
Transmission Line Characteristic Impedance(Zo)	Z_O			50		Ω
Driver Output Current Impedance, Single-ended				3000		Ω
High-Level Output Voltage	V_{OH}	Output single-ended voltage, Note 9, (R_S=33 Ω , R_T=50Ω)	0.65	0.71	0.85	V
Low-Level Output Voltage	V_{OL}		-0.20	0	0.05	V
I_{OH} @6*I_R	I_{OH}		-13	-14.2	-17	mA
Output Common Mode Voltage	[V_{OCM}] $V_{OCM(DC)}$ $V_{OCM(AC)}$	Note 10, 11, R_{LOAD}=100Ω between outputs). Peak Change in Output Common mode voltage when driving logic 0 and when driving logic1 under DC and AC conditions	0.25 -0.015 -0.050		0.55 0.015 0.050	V
Output Enable Time		OE going high to valid differential outputs			180	ns
Output Disable Time		OE going low to differential outputs becoming invalid (tri-state)			180	ns

IREF

If board target trace impedance (Z) is 50Ω, then RSET = 475Ω (1%), providing IREF of 2.32 mA, output current (I_{OH}) is equal to 6*IREF.

Notes

1) The typical frequency is not specified since this is a spread clock.

2) Measured at 10 µs.

3) This spread range and rate result in a cycle-to-cycle jitter 0f 0.1 ps.

4) Longest period including jitter and spread minus shortest period including jitter and spread equals 301 ps.

5) longest period including jitter and spread minus shortest period including jitter and spread equals 352 ps.

6) Longest period including jitter and spread – shortest period including jitter and spread equals 403.

7) When the output is transitioning between logic 0 and logic 1 or logic 1 and logic 0, the outputs shall monotonically transition between V_{OL} and V_{OH}, V_{OH} and V_{OL} respectively.

8) Calculated as $2*(T_R-T_F)/(T_R+T_F)$.

9) Measured across R_T(R_T is termination, 50 ohm load).

10) Peak change in output differential voltage when driving a logic 0 and when driving a logic 1 under DC conditions.

11) Peak change in output differential voltage when driving a logic 0 and when driving a logic 1 under AC conditions.

Clock Details and Topology

The topology of each 100 MHz circuit is shown for reference in Fig 1.

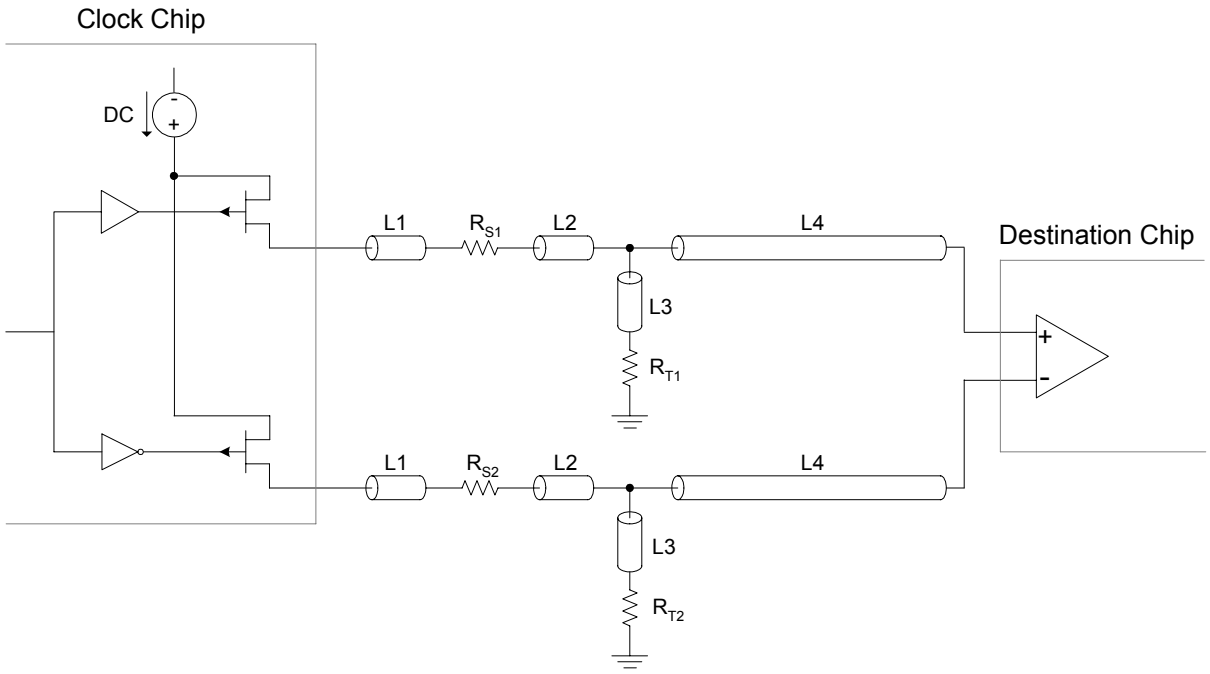


Fig 1: Clock chip Outputs current and translation to voltage is done on the motherboard for destination chip.

Topology Details

L1= 0.5”

L2, L3 =0.25”

L4=8”

R_{S1},R_{S2} = 33 Ω ±5%

R_{T1}, R_{T2} = 49.9 Ω ±1%

Receiver has no internal termination.

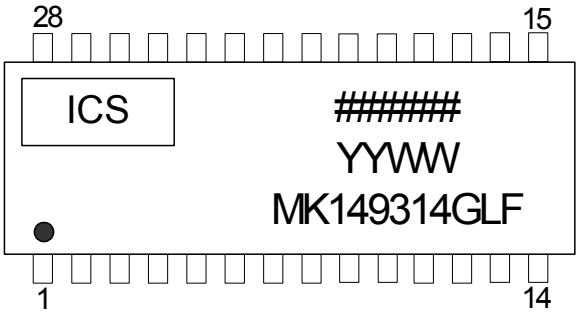
Length of L3 should be minimized to improve signal integrity.

L4 will have two to a maximum of four vias.

Thermal Characteristics (28-pin TSSOP)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		83		°C/W
	θ_{JA}	1 m/s air flow		75		°C/W
	θ_{JA}	2 m/s air flow		61		°C/W
Thermal Resistance Junction to Case	θ_{JC}			60		°C/W

Marking Diagram

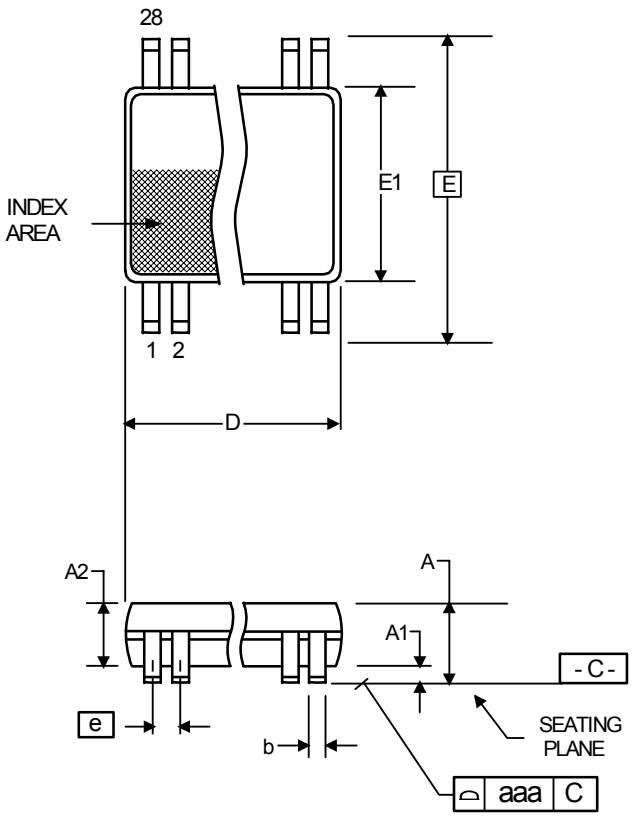


Notes:

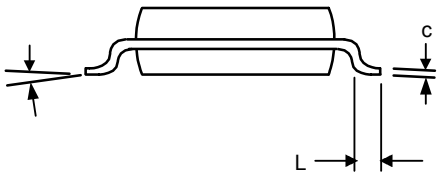
1. ###### is the lot code.
2. YYWW is the last two digits of the year, and the week number that the part was assembled.
3. “LF” denotes Pb free package.
4. Bottom marking: (origin). Origin = country of origin if not USA.

Package Outline and Package Dimensions (28-pin TSSOP, 173 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153



	Millimeters		Inche
Symbol	Min	Max	Min
A	--	1.20	--
A1	0.05	0.15	0.002
A2	0.80	1.05	0.032
b	0.19	0.30	0.007
C	0.09	0.20	0.0035
D	9.60	9.80	0.378
E	6.40 BASIC		0.252 BA
E1	4.30	4.50	0.169
e	0.65 Basic		0.0256 E
L	0.45	0.75	0.018
α	0°	8°	0°
aaa	--	0.10	--



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK1493-14GLF	see page 14	Tubes	28-pin TSSOP	0 to +70° C
MK1493-14GLFT		Tape and Reel	28-pin TSSOP	0 to +70° C

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
A	P. Griffith	08/22/05	Released from custom to general purpose device.

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