IS61LV3216



32K x 16 LOW VOLTAGE CMOS STATIC RAM

NOVEMBER 1997

FEATURES

- High-speed access time: 10, 12, 15, and 20 ns
- CMOS low power operation
 - 150 mW (typical) operating
 - 150 µW (typical) standby
- TTL compatible interface levels
- Single 3.3V ± 10% power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Industrial temperature available
- Available in 44-pin 400-mil SOJ package and 44-pin TSOP (Type 2)

DESCRIPTION

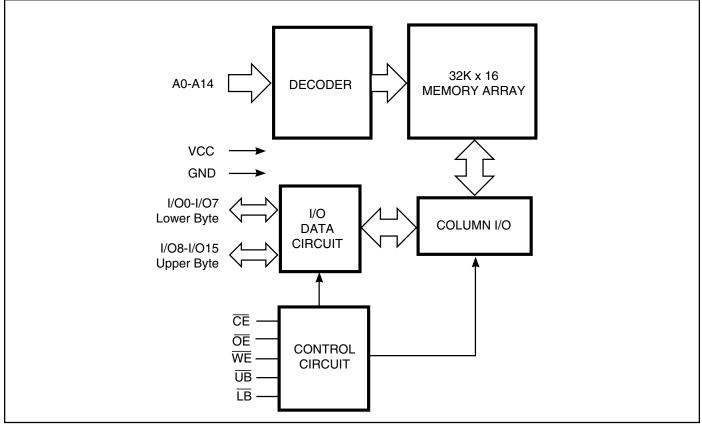
The *ISSI* IS61LV3216 is a high-speed, 512K static RAM organized as 32,768 words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields fast access times with low power consumption.

When \overline{CE} is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, \overline{CE} and \overline{OE} . The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory.A data byte allows Upper Byte (\overline{UB}) and Lower Byte (\overline{LB}) access.

The IS61LV3216 is packaged in the JEDEC standard 44-pin 400-mil SOJ and 44-pin TSOP (Type 2).





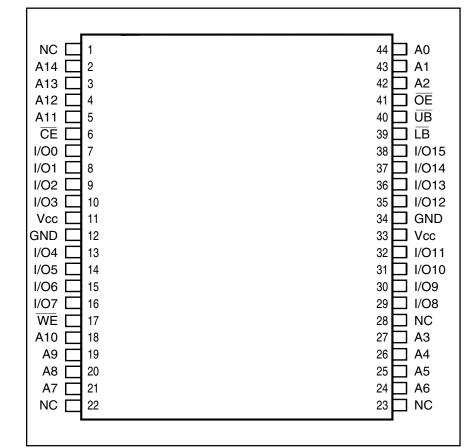
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IS61LV3216

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PIN CONFIGURATIONS 44-Pin SOJ

NC [1	44 🗌 A0
A14 🔲 2	43 🗌 A1
A13 🔲 3	42 🗖 A2
A12 🚺 4	41 🗌 🖸
A11 🚺 5	40 🗌 ŪB
	39 🗌 🗔
I/O0 🔲 7	38 🗍 I/O15
I/O1 🛛 8	37 🗌 1/014
I/O2 🗌 9	36 🗍 I/O13
I/O3 🔲 10	35 🗍 I/O12
Vcc 🚺 11	34 🗌 GND
GND [12	33 🗌 Vcc
I/O4 🔲 13	32 🗍 I/O11
I/O5 🔲 14	31 🗍 I/O10
I/O6 🔲 15	30 🗌 I/O9
I/O7 🔲 16	29 🗍 I/O8
WE [17	28 🗌 NC
A10 🔲 18	27 🗋 A3
A9 🔲 19	26 🗌 A4
A8 🗖 20	25 🗍 A5
A7 🗖 21	24 🗋 A6
NC 🛛 22	23 🗍 NC



PIN DESCRIPTIONS

A0-A14	Address Inputs	LB	Lower-byte Control (I/O0-I/O7)
I/O0-I/O15	Data Inputs/Outputs	UB	Upper-byte Control (I/O8-I/O15)
CE	Chip Enable Input	NC	No Connection
ŌĒ	Output Enable Input	Vcc	Power
WE	Write Enable Input	GND	Ground

TRUTH TABLE

						I/O	PIN	
Mode	WE	CE	ŌĒ	LB	UB	I/00-I/07	I/O8-I/O15	Vcc Current
Not Selected	Х	Н	Х	Х	Х	High-Z	High-Z	ISB1, ISB2
Output Disabled	Н	L	Н	Х	Х	High-Z	High-Z	lcc
	Х	L	Х	Н	Н	High-Z	High-Z	
Read	Н	L	L	L	Н	Dout	High-Z	lcc
	Н	L	L	Н	L	High-Z	DOUT	
	Н	L	L	L	L	Dout	Dout	
Write	L	L	Х	L	Н	DIN	High-Z	lcc
	L	L	Х	Н	L	High-Z	DIN	
	L	L	Х	L	L	DIN	DIN	

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
Vcc	Supply Voltage with Respect to GND	–0.5 to +4.6	V
VTERM	Terminal Voltage with Respect to GND	-0.5 to Vcc + 0.5	V
Tstg	Storage Temperature	-65 to +150	°C
Рт	Power Dissipation	1.0	W
Ιουτ	DC Output Current (LOW)	20	mA

Note:

 Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc	
Commercial	0°C to +70°C	3.3V ± 10%	

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
Vон	Output HIGH Voltage	Vcc = Min., Iон = -4.0 mA	2.4	_	V
Vol	Output LOW Voltage	Vcc = Min., IoL = 8.0 mA		0.4	V
Vih	Input HIGH Voltage		2.2	Vcc + 0.3	V
VIL	Input LOW Voltage ⁽¹⁾		-0.3	0.8	V
L	Input Leakage	GND - VIN - Vcc	-2	2	μA
Ilo	Output Leakage	GND - VOUT - VCC, Outputs Disabled	-2	2	μA

Notes:

1. VIL (min.) = -3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

				-1() ns	-12	ns	-15	ns	-20	ns	
Symbol	Parameter	Test Conditions		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
lcc	Vcc Dynamic Operating Supply Current	Vcc = Max., lout = 0 mA, f = fmax	Com. Ind.	_	220 —	_	200 230	_	180 200	_	160 180	mA
ISB1	TTL Standby Current (TTL Inputs)	$\label{eq:Vcc} \begin{array}{l} Vcc = Max., \\ V_{IN} = V_{IH} \text{ or } V_{IL} \\ \hline \hline \hline CE \bullet V_{IH} \ , \ f = 0 \end{array}$	Com. Ind.	_	10 	_	10 20	_	10 20	_	10 20	mA
ISB2	CMOS Standby Current (CMOS Inputs)	$\label{eq:constraint} \begin{array}{l} V_{CC} = Max., \\ \hline CE \bullet V_{CC} - 0.2V, \\ V_{IN} \bullet V_{CC} - 0.2V, \mbox{ or } \\ V_{IN} \bullet 0.2V, \mbox{ f} = 0 \end{array}$	Com. Ind.	_	5	_	5 10	_	5 10	_	5 10	mA

Note:

1. At $f = f_{MAX}$, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

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CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions	Max.	Unit
CIN	Input Capacitance	$V_{IN} = 0V$	6	pF
Соит	Input/Output Capacitance	Vout = 0V	8	pF

Note:

1. Tested initially and after any design or process changes that may affect these parameters.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

		-10	0	-1	2	-1	5	-20)	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
trc	Read Cycle Time	10	_	12	_	15	_	20	_	ns
taa	Address Access Time	_	10	_	12	—	15	_	20	ns
tона	Output Hold Time	3	_	3	_	3	—	3	_	ns
t ACE	CE Access Time	_	10	_	12	_	15	—	20	ns
t DOE	OE Access Time	_	5	_	6	_	7	_	8	ns
thzoe ⁽²⁾	OE to High-Z Output	0	5	0	6	0	7	0	8	ns
tlzoe ⁽²⁾	OE to Low-Z Output	0	_	0	_	0	_	0	_	ns
tHZCE ⁽²	CE to High-Z Output	0	5	0	6	0	7	0	8	ns
tlzce ⁽²⁾	CE to Low-Z Output	4	_	4	_	4	_	4	_	ns
tва	LB, UB Access Time	_	5	_	6	_	7	_	8	ns
tнzв	$\overline{\text{LB}}$, $\overline{\text{UB}}$ to High-Z Output	0	5	0	6	0	7	0	8	ns
t LZB	LB, UB to Low-Z Output	5		5	_	5	_	5	_	ns

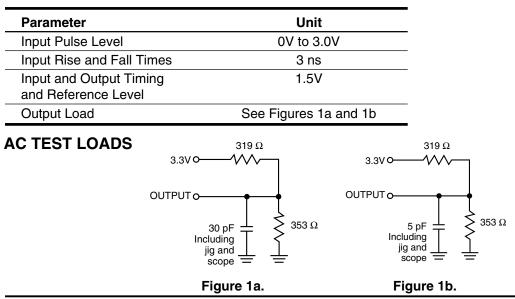
Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.

2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

3. Not 100% tested.

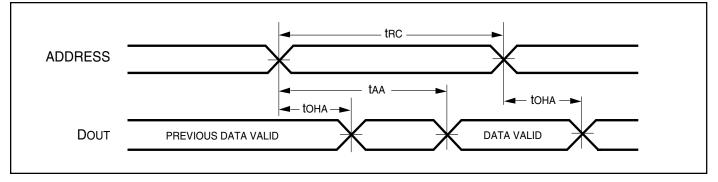
AC TEST CONDITIONS



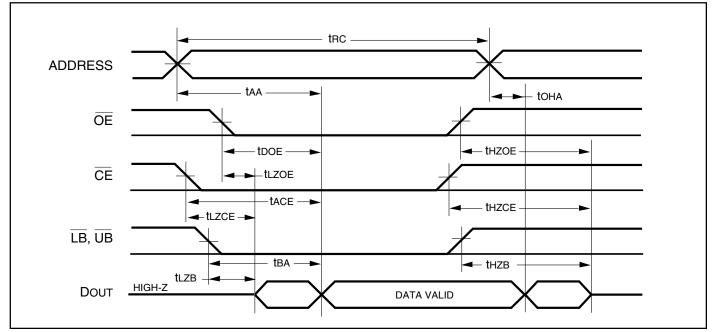
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AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$, \overline{UB} or $\overline{LB} = V_{IL}$)



READ CYCLE NO. 2^(1,3)



- **Notes:** 1. WE is HIGH for a Read Cycle.
- 2. The device is continuously selected. \overline{OE} , \overline{CE} , \overline{UB} , or $\overline{LB} = V_{IL}$.
- 3. Address is valid prior to or coincident with \overline{CE} LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

		-1	0	-1	2	-1	5	-2	0	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
twc	Write Cycle Time	10	_	12	_	15	_	20	_	ns
t SCE	CE to Write End	9	_	10	_	11	_	12	_	ns
taw	Address Setup Time to Write End	9	_	10	_	11	_	12	_	ns
tна	Address Hold from Write End	0	_	0	_	0	_	0	_	ns
t sa	Address Setup Time	0	_	0	_	0	_	0	_	ns
tрwв	$\overline{\text{LB}}$, $\overline{\text{UB}}$ Valid to End of Write	9	_	10	_	11	_	12	_	ns
t PWE	WE Pulse Width	7	_	8	_	10	—	11	_	ns
tsp	Data Setup to Write End	5	_	6	_	7	_	_	8	ns
t HD	Data Hold from Write End	0	_	0	_	0	_	0	_	ns
thzwe ⁽²⁾	WE LOW to High-Z Output	_	5	_	6		7	_	8	ns
tlzwe ⁽²⁾	WE HIGH to Low-Z Output	1	_	1	_	1	_	1	_	ns

Notes:

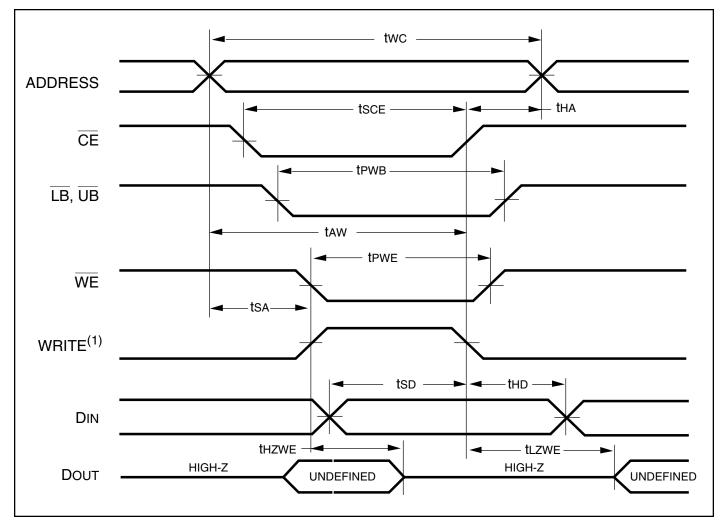
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.

2. Tested with the load in Figure 1b. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

3. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{UB} or \overline{LB} , and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

WRITE CYCLE NO. 1 (WE Controlled)^(1,2)



Notes:

- 1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the \overline{CE} and \overline{WE} inputs and at least one of the LB and UB inputs being in the LOW state.
- 2. WRITE = $(\overline{CE}) [(\overline{LB}) = (\overline{UB})] (\overline{WE}).$

ORDERING INFORMATION Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
10	IS61LV3216-10T	Plastic TSOP (Type 2)
10	IS61LV3216-10K	400-mil Plastic SOJ
12	IS61LV3216-12T	Plastic TSOP (Type 2)
12	IS61LV3216-12K	400-mil Plastic SOJ
15	IS61LV3216-15T	Plastic TSOP (Type 2)
15	IS61LV3216-15K	400-mil Plastic SOJ
20	IS61LV3216-20T	Plastic TSOP (Type 2)
20	IS61LV3216-20K	400-mil Plastic SOJ

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
12	IS61LV3216-12TI	Plastic TSOP (Type 2)
12	IS61LV3216-12KI	400-mil Plastic SOJ
15	IS61LV3216-15TI	Plastic TSOP (Type 2)
15	IS61LV3216-15KI	400-mil Plastic SOJ
20	IS61LV3216-20TI	Plastic TSOP (Type 2)
20	IS61LV3216-20KI	400-mil Plastic SOJ

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