

LR38581

Timing Generator IC for 270 k/320 k-pixel Color CCDs with Dual-power-supply Operation

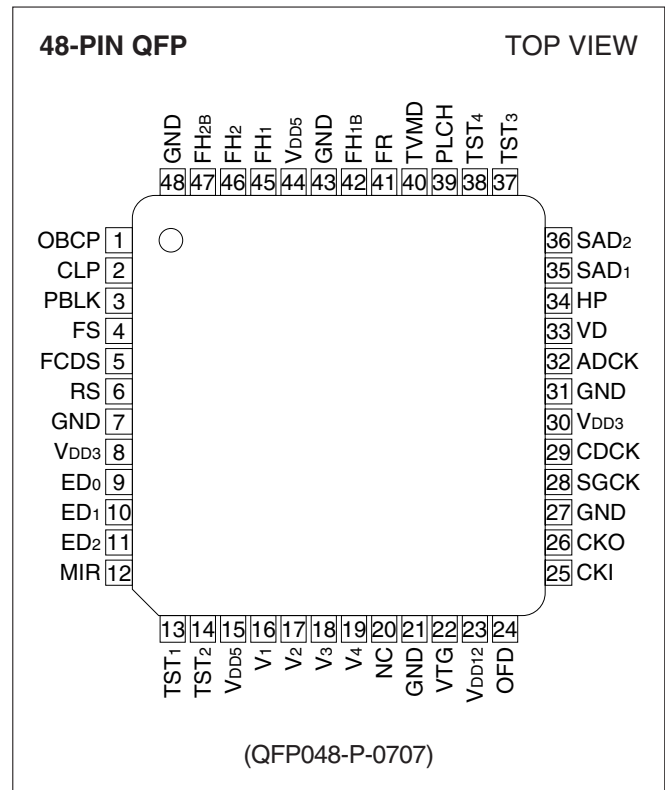
DESCRIPTION

The LR38581 is a CMOS timing generator IC which generates timing pulses for driving 270 k/320 k-pixel color CCD area sensors with a dual-power-supply operation and processing pulses for color video signals.

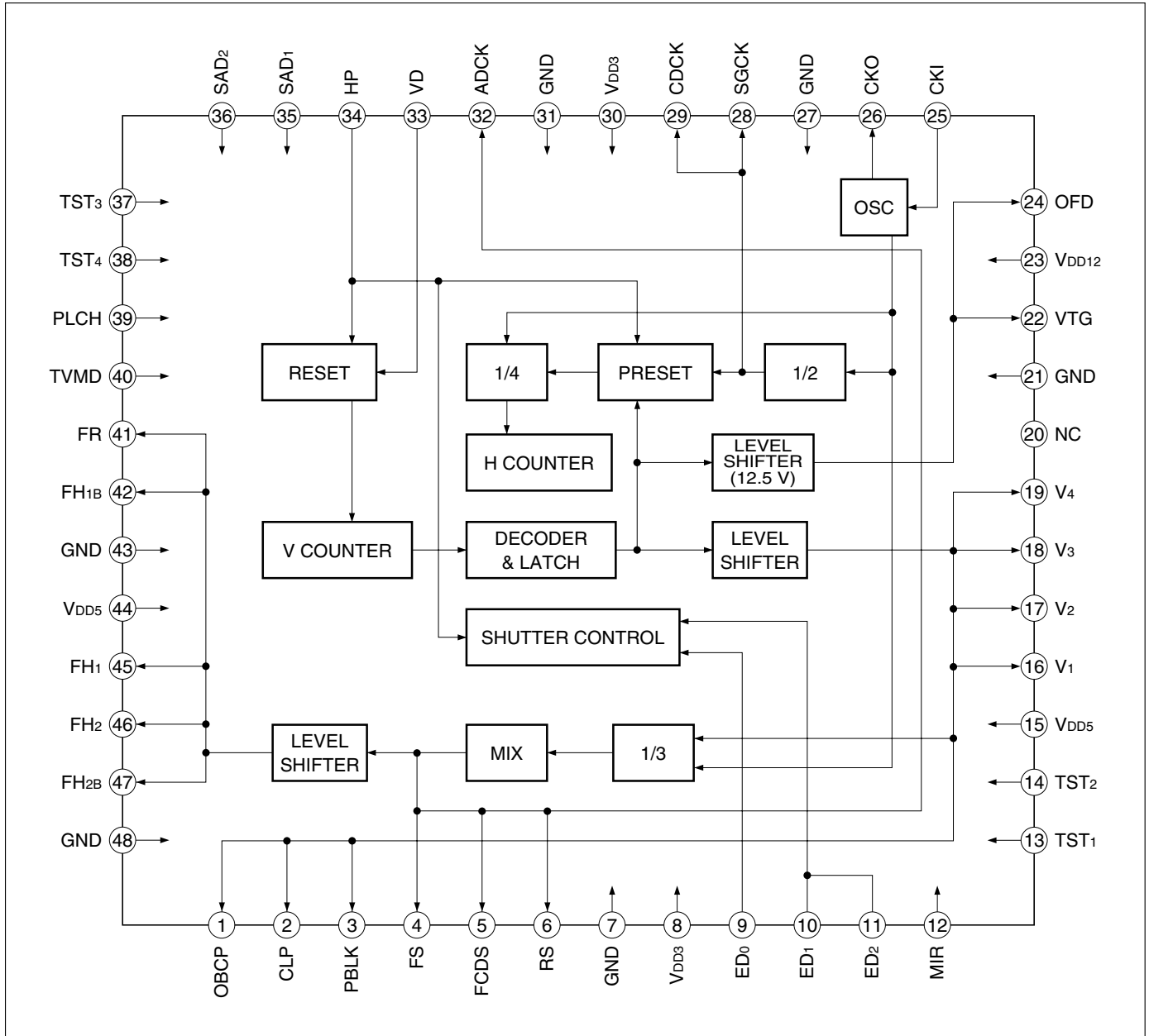
FEATURES

- Designed for 270 k/320 k-pixel color CCD area sensors with a dual-power-supply-operation
- Switchable between NTSC and PAL modes
- Switchable between normal and mirror images
- Level shifter for readout and shutter pulses included
- +3.3 V, +5 V and +12.5 V power supplies
- Package :
48-pin QFP (QFP048-P-0707) 0.5 mm pin-pitch

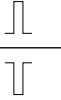








PIN CONNECTIONS
















BLOCK DIAGRAM



PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	DESCRIPTION									
1	OBCP	O4MA3		Optical black clamp pulse output	A pulse to clamp the optical black signal. This pulse stays low during the absence of effective pixels within the vertical blanking. The polarity can be changed by PLCH (pin 39).									
2	CLP	O4MA3		AD input signal clamp pulse output	A pulse to clamp the AD input signal. The polarity can be changed by PLCH (pin 39).									
3	PBLK	O4MA3		Pre-blanking pulse output	A pulse that corresponds to the cease period of the horizontal transfer pulse.									
4	FS	O4MA32		CDS pulse output 1	A pulse to sample-hold the signal from CCD. The polarity can be changed by PLCH (pin 39). The output phase of FS is selected by serial data.									
5	FCDS	O4MA32		CDS pulse output 2	A pulse to clamp the feed-through level from CCD. The polarity can be changed by PLCH (pin 39). The output phase of FCDS is selected by serial data.									
6	RS	O4MA32		S/H pulse output	A pulse to sample-hold the signal from CDS circuit. The polarity can be changed by PLCH (pin 39). The output phase of RS is selected by serial data.									
7	GND	–	–	Ground	A grounding pin.									
8	VDD3	–	–	Power supply	Supply of +3.3 V power.									
9	ED0	ICSU3	–	Shift register clock input	An input pin for the clock of the shift register, to control the functions of LR38581. For details, see " Serial Data Control ."									
10	ED1	ICSU3	–	Shift register data input	An input pin for the data of the shift register, to control the functions of LR38581. For details, see " Serial Data Control ."									
11	ED2	ICSU3	–	Strobe pulse input	An input pin for the strobe pulse, to control the functions of LR38581. For details, see " Serial Data Control ."									
12	MIR	ICU3	–	Mirror mode selection	An input pin to select mirror or normal image mode L level : Normal image mode H level or open : Mirror image mode <table border="1" data-bbox="841 1411 1453 1533"> <thead> <tr> <th>MIR</th> <th>L (Normal mode)</th> <th>H or open (Mirror mode)</th> </tr> </thead> <tbody> <tr> <td>FH1B</td> <td>≡ FH1</td> <td>≡ FH2</td> </tr> <tr> <td>FH2B</td> <td>≡ FH2</td> <td>≡ FH1</td> </tr> </tbody> </table>	MIR	L (Normal mode)	H or open (Mirror mode)	FH1B	≡ FH1	≡ FH2	FH2B	≡ FH2	≡ FH1
MIR	L (Normal mode)	H or open (Mirror mode)												
FH1B	≡ FH1	≡ FH2												
FH2B	≡ FH2	≡ FH1												
13	TST1	ICD5	–	Test pin 1	A test pin. Set open or to L level in the normal mode.									
14	TST2	ICD5	–	Test pin 2	A test pin. Set open or to L level in the normal mode.									
15	VDD5	–	–	Power supply	Supply of +5 V power.									
16	V1	O4MA52		Vertical transfer pulse output 1	A pulse to drive vertical CCD shift register. Connect to ϕv_1 pin of CCD.									
17	V2	O4MA52		Vertical transfer pulse output 2	A pulse to drive vertical CCD shift register. Connect to ϕv_2 pin of CCD.									
18	V3	O4MA52		Vertical transfer pulse output 3	A pulse to drive vertical CCD shift register. Connect to ϕv_3 pin of CCD.									

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	DESCRIPTION						
19	V ₄	O4MA52		Vertical transfer pulse output 4	A pulse to drive vertical CCD shift register. Connect to ϕ V ₄ pin of CCD.						
20	NC	–	–	No connection	No connection						
21	GND	–	–	Ground	A grounding pin.						
22	VTG	O12MHV		Readout pulse output	A pulse that transfers the charge of the photo-diode to the vertical shift register. Connect to VTG pin of CCD.						
23	V _{DD12}	–	–	Power supply	Supply of +12.5 V power.						
24	OFD	O12MHV		OFD pulse output	A pulse that sweeps the charge of the photo-diode for electronic shutter. Connect to OFD pin of CCD. Held at L level at normal mode.						
25	CKI	OSCI3	–	Clock input	An input pin for reference clock oscillation. Connect to CKO (pin 26) with R. The frequencies are as follows : <table border="1" data-bbox="846 762 1453 884"> <thead> <tr> <th>TVMD</th> <th>Frequency</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>28.63636 MHz (1820 fH)</td> </tr> <tr> <td>H</td> <td>28.37500 MHz (1816 fH)</td> </tr> </tbody> </table> <p style="text-align: right;">fH = Horizontal frequency</p>	TVMD	Frequency	L	28.63636 MHz (1820 fH)	H	28.37500 MHz (1816 fH)
TVMD	Frequency										
L	28.63636 MHz (1820 fH)										
H	28.37500 MHz (1816 fH)										
26	CKO	OSCO3	–	Clock output	An output pin for reference clock oscillation. The output is the inverse of CKI (pin 25).						
27	GND	–	–	Ground	A grounding pin.						
28	SGCK	O4MA32		SSG clock output	An output pin to generate HP and VD pulses. The frequencies are as follows : <table border="1" data-bbox="846 1129 1453 1251"> <thead> <tr> <th>TVMD</th> <th>Frequency</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>14.31818 MHz (910 fH)</td> </tr> <tr> <td>H</td> <td>14.18750 MHz (908 fH)</td> </tr> </tbody> </table>	TVMD	Frequency	L	14.31818 MHz (910 fH)	H	14.18750 MHz (908 fH)
TVMD	Frequency										
L	14.31818 MHz (910 fH)										
H	14.18750 MHz (908 fH)										
29	CDCK	O4MA32		DSP clock output	An output pin for DSP IC. The frequencies are as follows : <table border="1" data-bbox="846 1350 1453 1472"> <thead> <tr> <th>TVMD</th> <th>Frequency</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>9.5035 MHz (1820/3 fH)</td> </tr> <tr> <td>H</td> <td>9.4375 MHz (1816/3 fH)</td> </tr> </tbody> </table>	TVMD	Frequency	L	9.5035 MHz (1820/3 fH)	H	9.4375 MHz (1816/3 fH)
TVMD	Frequency										
L	9.5035 MHz (1820/3 fH)										
H	9.4375 MHz (1816/3 fH)										
30	V _{DD3}	–	–	Power supply	Supply of +3.3 V power.						
31	GND	–	–	Ground	A grounding pin.						
32	ADCK	O4MA32		AD clock output	An output pin for AD converter. The frequencies are as follows : <table border="1" data-bbox="846 1654 1453 1776"> <thead> <tr> <th>TVMD</th> <th>Frequency</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>9.5035 MHz (1820/3 fH)</td> </tr> <tr> <td>H</td> <td>9.4375 MHz (1816/3 fH)</td> </tr> </tbody> </table> <p>The output phase of ADCK is selected by SAD₁ (pin 35) and SAD₂ (pin 36).</p>	TVMD	Frequency	L	9.5035 MHz (1820/3 fH)	H	9.4375 MHz (1816/3 fH)
TVMD	Frequency										
L	9.5035 MHz (1820/3 fH)										
H	9.4375 MHz (1816/3 fH)										

PIN NO.	SYMBOL	I/O	POLARITY	PIN NAME	DESCRIPTION															
33	VD	IC3		Vertical reference pulse input	An input pin for reference of vertical pulse. Connect to VD pin of DSP IC.															
34	HP	IC3		Horizontal reference pulse input	An input pin for reference of horizontal pulse. Connect to HD pin of DSP IC.															
35	SAD ₁	ICU3	–	ADCK phase control input 1	An input pin to select the phase of ADCK. <table border="1" data-bbox="844 388 1429 514"> <tr> <td>SAD₁</td> <td>L</td> <td>H or open</td> <td>L</td> <td>H or open</td> </tr> <tr> <td>SAD₂</td> <td>L</td> <td>L</td> <td>H or open</td> <td>H or open</td> </tr> <tr> <td>Phase</td> <td>0°</td> <td>60° delay</td> <td>180° delay</td> <td>240° delay</td> </tr> </table>	SAD ₁	L	H or open	L	H or open	SAD ₂	L	L	H or open	H or open	Phase	0°	60° delay	180° delay	240° delay
SAD ₁	L	H or open	L	H or open																
SAD ₂	L	L	H or open	H or open																
Phase	0°	60° delay	180° delay	240° delay																
36	SAD ₂	ICU3	–	ADCK phase control input 2																
37	TST ₃	ICD5	–	Test pin 3	A test pin. Set open or to L level in the normal mode.															
38	TST ₄	ICD5	–	Test pin 4	A test pin. Set open or to L level in the normal mode.															
39	PLCH	ICU5	–	Polarity selection input	An input pin to select the polarity of OBCP (pin 1), CLP (pin 2), FS (pin 4), FCDS (pin 5) and RS (pin 6).															
40	TVMD	ICU5	–	TV mode selection input	An input pin to select TV standards. L level : NTSC mode H level or open : PAL mode															
41	FR	O4MA53		Reset pulse output	A pulse to reset the charge of output circuit. Connect to ϕ_R pin of CCD through the DC offset circuit. The output phase of FR is selected by serial data.															
42	FH _{1B}	O4MA52		Horizontal transfer pulse output 1B	A pulse to drive horizontal CCD shift register. Connect to ϕ_{H1B} pin of CCD.															
43	GND	–	–	Ground	A grounding pin.															
44	VDD5	–	–	Power supply	Supply of +5 V power.															
45	FH ₁	O4MA53		Horizontal transfer pulse output 1	A pulse to drive horizontal CCD shift register. Connect to ϕ_{H1} pin of CCD.															
46	FH ₂	O4MA53		Horizontal transfer pulse output 2	A pulse to drive horizontal CCD shift register. Connect to ϕ_{H2} pin of CCD.															
47	FH _{2B}	O4MA52		Horizontal transfer pulse output 2B	A pulse to drive horizontal CCD shift register. Connect to ϕ_{H2B} pin of CCD.															
48	GND	–	–	Ground	A grounding pin.															

IC3 : Input pin (CMOS level)

ICU3 : Input pin (CMOS level with pull-up resistor)

ICSU3 : Input pin (CMOS schmitt-trigger level with pull-up resistor)

ICU5 : Input pin (CMOS level with pull-up resistor)

ICD5 : Input pin (CMOS level with pull-up resistor)

O4MA3 : Output pin (V_{DD} = 3.3 V)

O4MA32 : Output pin (V_{DD} = 3.3 V)

O4MA52 : Output pin (V_{DD} = 5 V)

O4MA53 : Output pin (V_{DD} = 5 V)

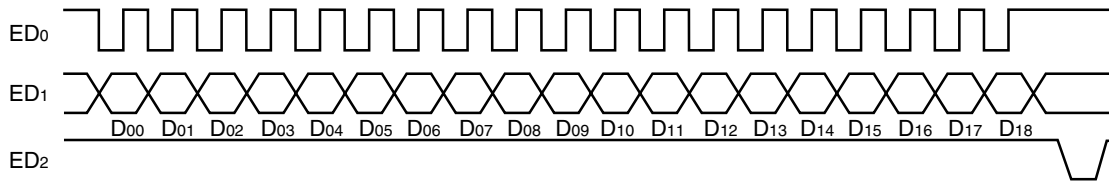
O12MHV : Output pin (V_{DD} = 12.5 V)

OSCI3 : Input pin for oscillation

OSCO3 : Output pin for oscillation

Serial Data Control

SERIAL DATA INPUT TIMING



The serial data ED1 is shifted by ED0 and is latched at the rising edge of ED2.

The shutter mode data SMD1 and SMD2 of serial data are latched at the rising edge of the horizontal

line in which VTG is active, the shutter speed data SD0 to SD8 are latched at the rising edge of the next horizontal line in which VTG is active.

SERIAL DATA INPUTS

DATA	NAME	FUNCTIONS
D00	SD0	Electronic shutter speed control
D01	SD1	
D02	SD2	
D03	SD3	
D04	SD4	
D05	SD5	
D06	SD6	
D07	SD7	
D08	SD8	

DATA	NAME	FUNCTIONS
D09	SMD1	Electronic shutter mode control
D10	SMD2	
D11	MR1	Phase control
D12	MR2	
D13	MC1	
D14	MC2	
D15	MS1	
D16	MS2	
D17	MF1	
D18	MF2	

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	VDD3, VDD5	-0.3 to +6.0	V
	VDD12	-0.3 to +15.0	V
Input voltage	VI3	-0.3 to VDD3 + 0.3	V
	VI5	-0.3 to VDD5 + 0.3	V
Output voltage	VO3	-0.3 to VDD3 + 0.3	V
	VO5	-0.3 to VDD5 + 0.3	V
	VO12	-0.3 to VDD12 + 0.3	V
Operating temperature	TOPR	-20 to +70	°C
Storage temperature	TSTG	-55 to +150	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics ($V_{DD3} = 3.3 \pm 0.33$ V, $V_{DD5} = 5.0 \pm 0.5$ V, $V_{DD12} = 12.5 \pm 0.5$ V, $T_{OPR} = -20$ to $+70$ °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL3}				$0.3V_{DD3}$	V	1, 2
Input "High" voltage	V_{IH3}		$0.7V_{DD3}$			V	
Input "Low" voltage	V_{IL5}				1.5	V	4, 5
Input "High" voltage	V_{IH5}		3.5			V	
Input "Low" voltage	V_{T+}				$0.75V_{DD3}$	V	3
Input "High" voltage	V_{T-}		$0.02V_{DD3}$			V	
Hysteresis voltage	$V_{T+} - V_{T-}$		$0.045V_{DD3}$			V	
Input "Low" current	$ I_{IL3-1} $	$V_I = 0$ V			1.0	μ A	1
Input "High" current	$ I_{IH3-1} $	$V_I = V_{DD3}$			1.0	μ A	
Input "Low" current	$ I_{IL3-2} $	$V_I = 0$ V	3.0		30	μ A	2, 3
Input "High" current	$ I_{IH3-2} $	$V_I = V_{DD3}$			2.0	μ A	
Input "Low" current	$ I_{IL5-1} $	$V_I = 0$ V	8.0		60	μ A	4
Input "High" current	$ I_{IH5-1} $	$V_I = V_{DD5}$			2.0	μ A	
Input "Low" current	$ I_{IL5-2} $	$V_I = 0$ V			2.0	μ A	5
Input "High" current	$ I_{IH5-2} $	$V_I = V_{DD5}$	8.0		60	μ A	
Output "Low" voltage	V_{OL3-1}	$I_{OL} = 1.5$ mA			0.4	V	6
Output "High" voltage	V_{OH3-1}	$I_{OH} = -1.5$ mA	$V_{DD3} - 0.5$			V	
Output "Low" voltage	V_{OL3-2}	$I_{OL} = 2$ mA			0.4	V	7
Output "High" voltage	V_{OH3-2}	$I_{OH} = -1.5$ mA	$V_{DD3} - 0.5$			V	
Output "Low" voltage	V_{OL3-3}	$I_{OL} = 4$ mA			0.4	V	8
Output "High" voltage	V_{OH3-3}	$I_{OH} = -3$ mA	$V_{DD3} - 0.5$			V	
Output "Low" voltage	V_{OL5-1}	$I_{OL} = 9$ mA			0.4	V	9
Output "High" voltage	V_{OH5-1}	$I_{OH} = -6$ mA	$V_{DD5} - 0.5$			V	
Output "Low" voltage	V_{OL5-2}	$I_{OL} = 12$ mA			0.4	V	10
Output "High" voltage	V_{OH5-2}	$I_{OH} = -9$ mA	$V_{DD5} - 0.5$			V	
Output "Low" voltage	V_{OL12}	$I_{OL} = 12$ mA			0.4	V	11
Output "High" voltage	V_{OH12}	$I_{OH} = -12$ mA	$V_{DD12} - 0.5$			V	

NOTES :

1. Applied to inputs (IC3, OSCI3).
2. Applied to input (ICU3).
3. Applied to input (ICSU3).
4. Applied to input (ICU5).
5. Applied to input (ICD5).
6. Applied to output (OSCO3). (Output (OSCO3) measures on condition that input (OSCI3) level is 0 V or V_{DD3} .)
7. Applied to output (O4MA3).
8. Applied to output (O4MA32).
9. Applied to output (O4MA52).
10. Applied to output (O4MA53).
11. Applied to output (O12MHV).

PACKAGE

(Unit : mm)

48 QFP (QFP048-P-0707)

